



STFI10NK60Z

N-channel 600 V, 0.65 Ω , 10 A, Zener-protected SuperMESH™ Power MOSFET in I²PAKFP package

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _{TOT}
STFI10NK60Z	600 V	< 0.75 Ω	10 A	35 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Switching applications

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well-established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

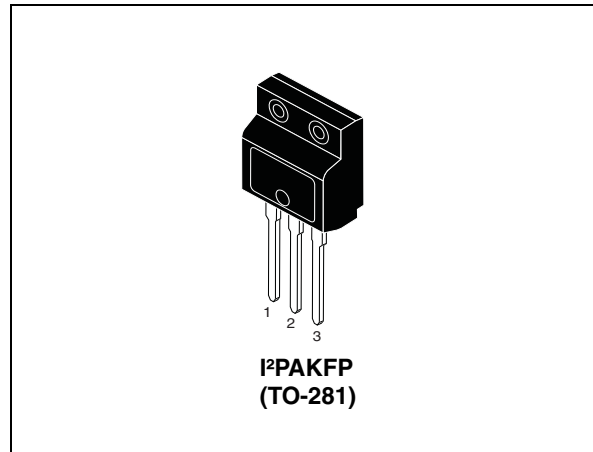


Figure 1. Internal schematic diagram

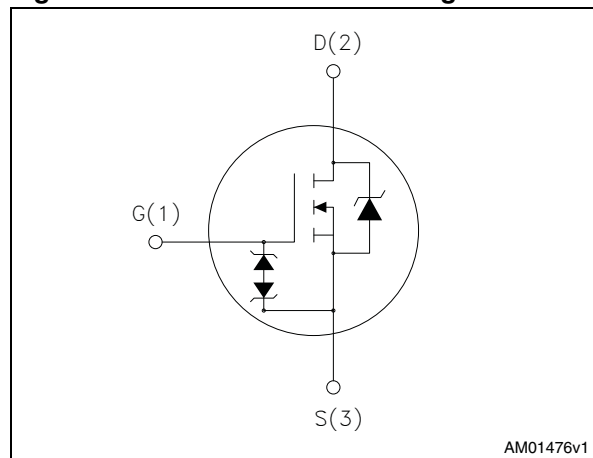


Table 1. Device summary

Order code	Marking	Package	Packaging
STFI10NK60Z	10NK60Z	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.7 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	36 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
ESD	Gate-source human body model (R=1,5 k Ω C=100 pF)	4	kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^\circ\text{C}$)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

- Limited by maximum junction temperature
- Pulse width limited by safe operating area
- $I_{SD} < 10\text{A}$, $di/dt < 200\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb Max	62.5	$^\circ\text{C}/\text{W}$

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Repetitive or non repetitive avalanche current	g ⁽¹⁾	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}= 50\text{ V}$)	300	mJ

- Limited by maximum junction temperature

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified).

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage, (V _{GS} = 0)	I _D = 250 μA	600			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 600 V V _{DS} = 600 V, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 4.5 A		0.65	0.75	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V, I _D = 4.5 A	-	7.8		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	1370 156 37		pF pF pF
C _{oss eq} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V	-	90		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 480 V, I _D = 8 A V _{GS} = 10 V (see Figure 16)	-	50 10 25	70	nC nC nC

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%

2. C_{oss eq} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t _{d(on)} t _r	Turn-on delay time Rise time	V _{DD} = 300 V, I _D = 4 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 15)	-	20 20	-	ns ns
t _{d(off)} t _f	Turn-off delay time Fall time	V _{DD} = 300 V, I _D = 4 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 15)	-	55 30	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10\text{ A}, V_{GS}=0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD}=40\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	570		ns
Q_{rr}	Reverse recovery charge		-	4.3		μC
I_{RRM}	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage ($I_D=0$)	$I_{GS} = \pm 1\text{ mA}$	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

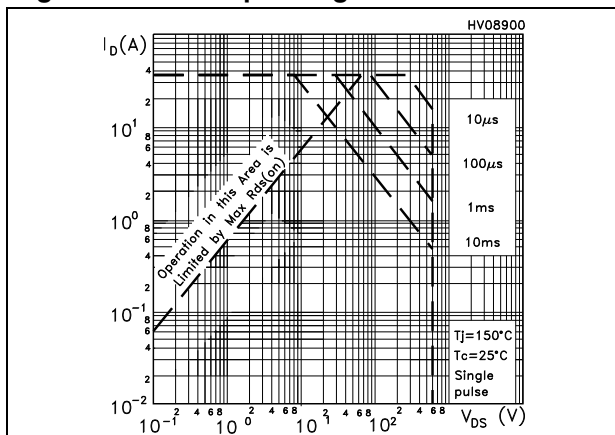


Figure 3. Thermal impedance

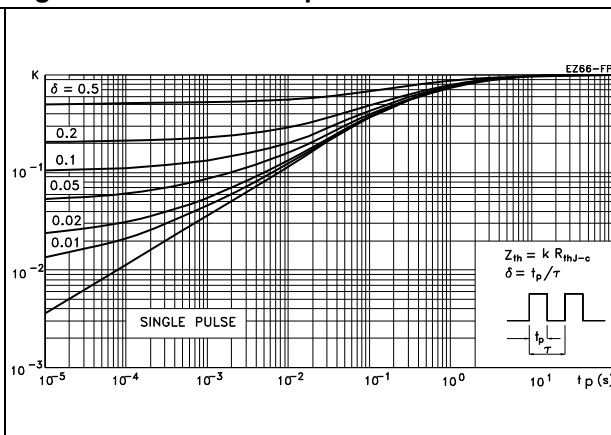


Figure 4. Output characteristics

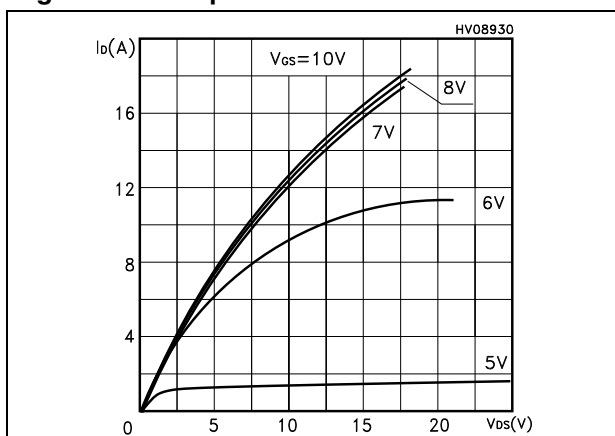


Figure 5. Transfer characteristics

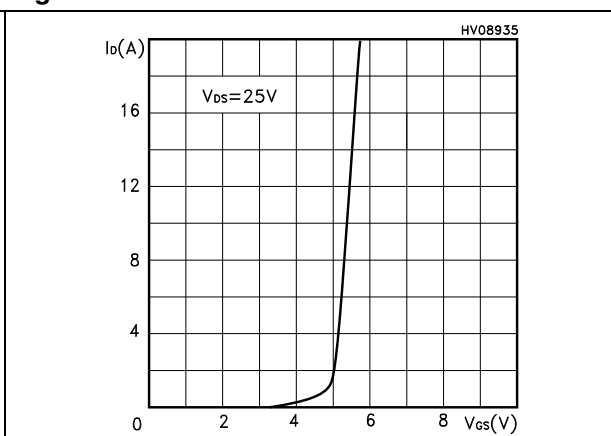


Figure 6. Transconductance

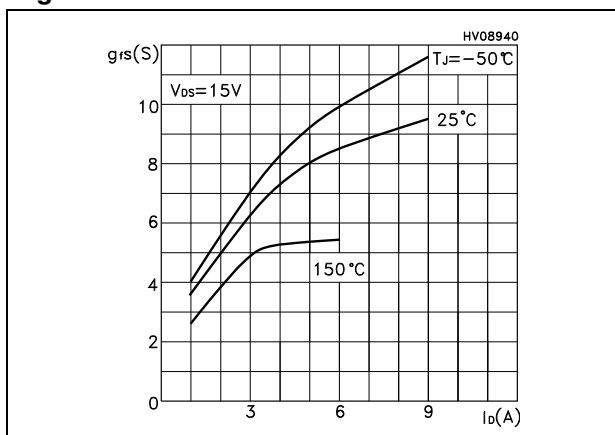


Figure 7. Static drain-source on resistance

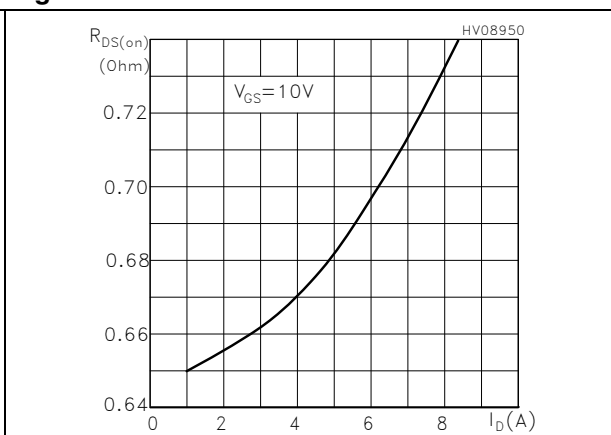


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

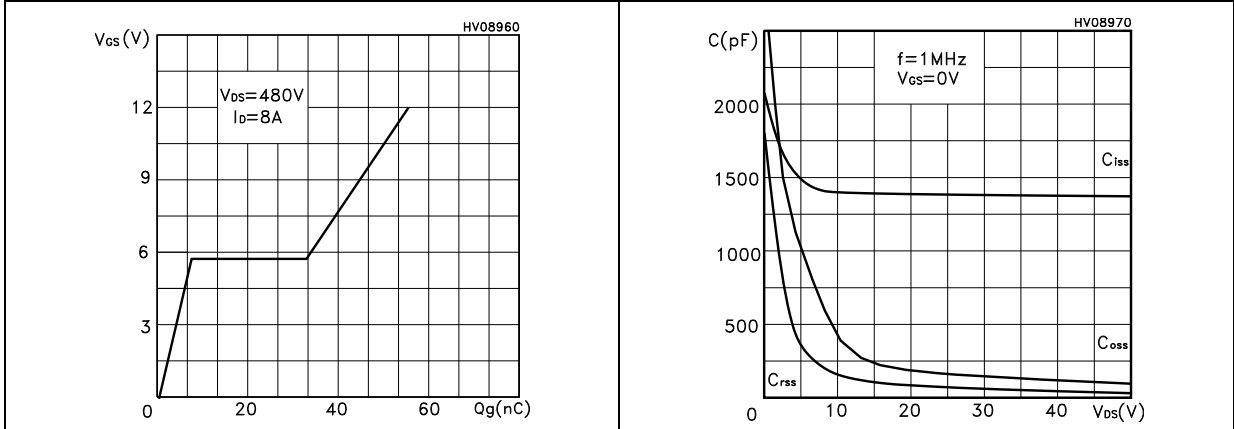


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

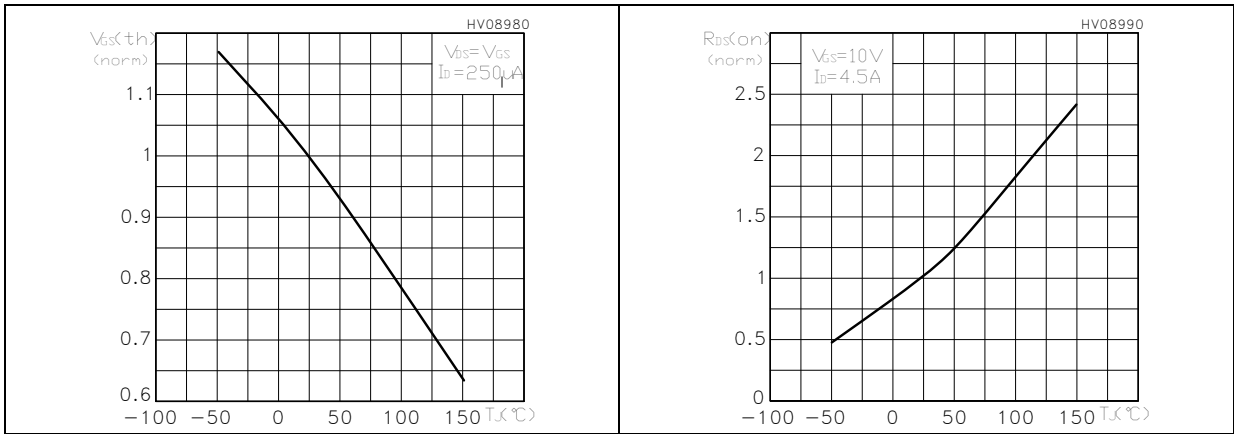


Figure 12. Source-drain diode forward characteristics Figure 13. Maximum avalanche energy vs temperature

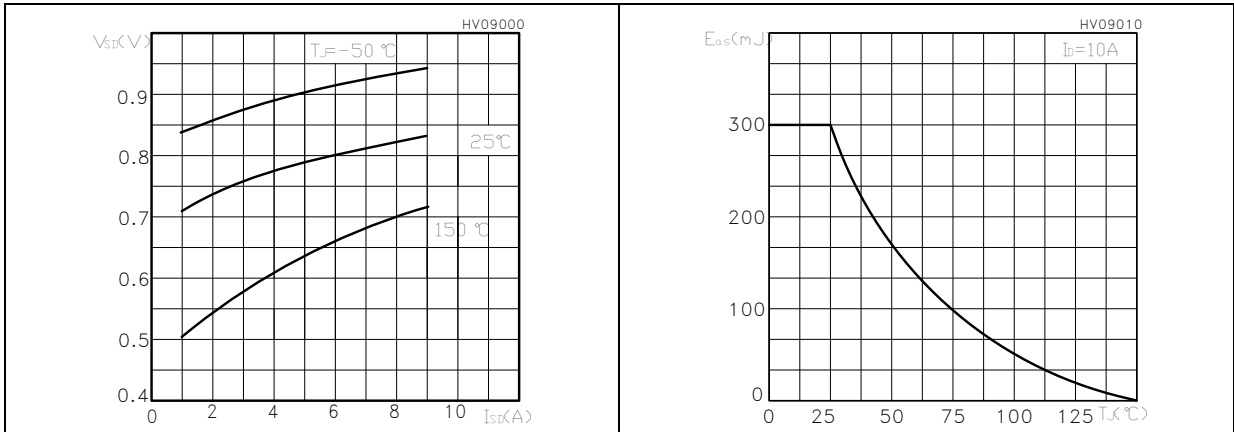
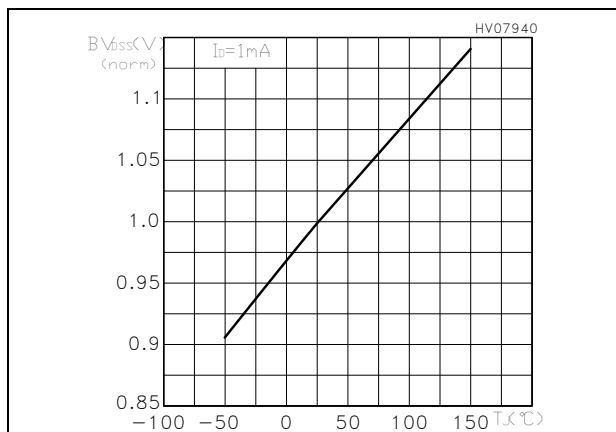


Figure 14. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit

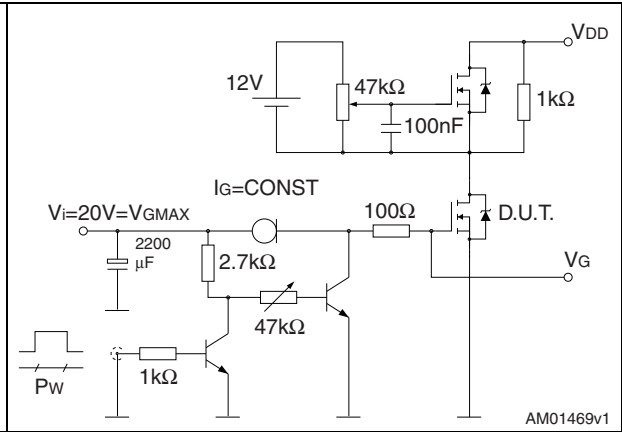


Figure 17. Test circuit for inductive load switching and diode recovery times

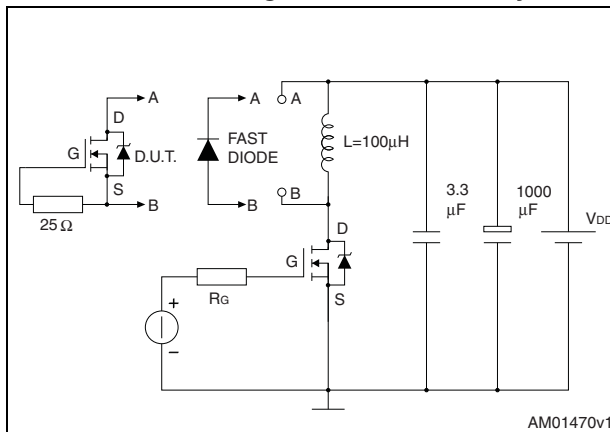


Figure 18. Unclamped inductive load test circuit

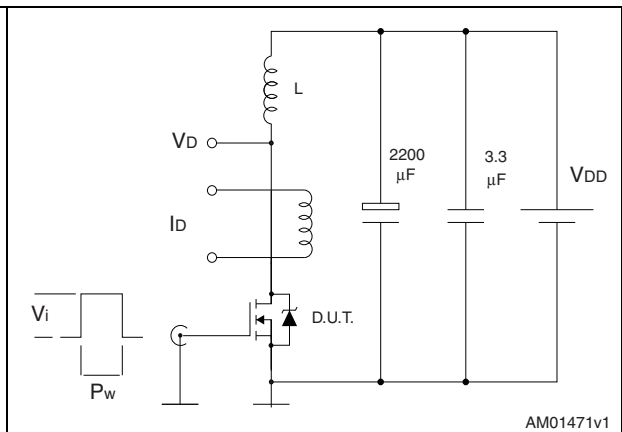


Figure 19. Unclamped inductive waveform

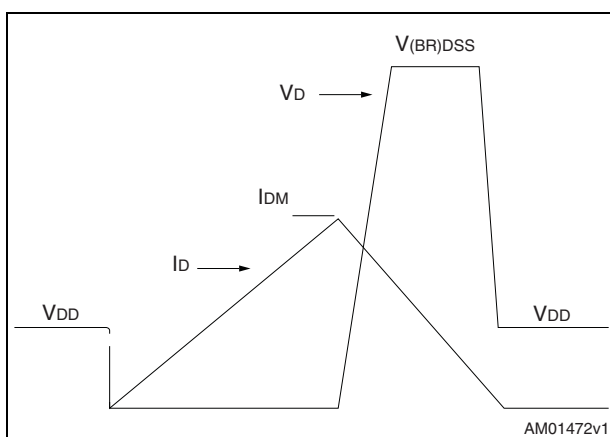
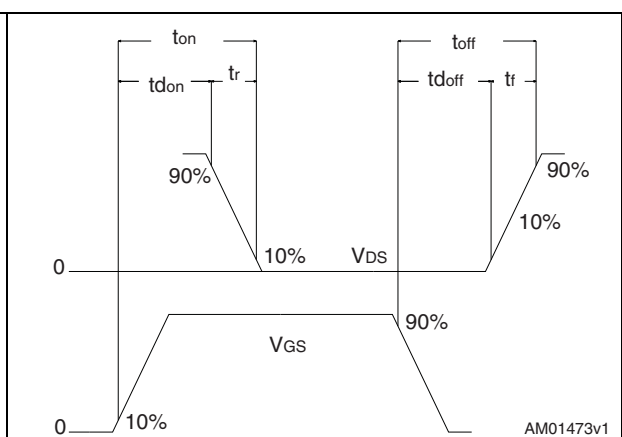


Figure 20. Switching time waveform



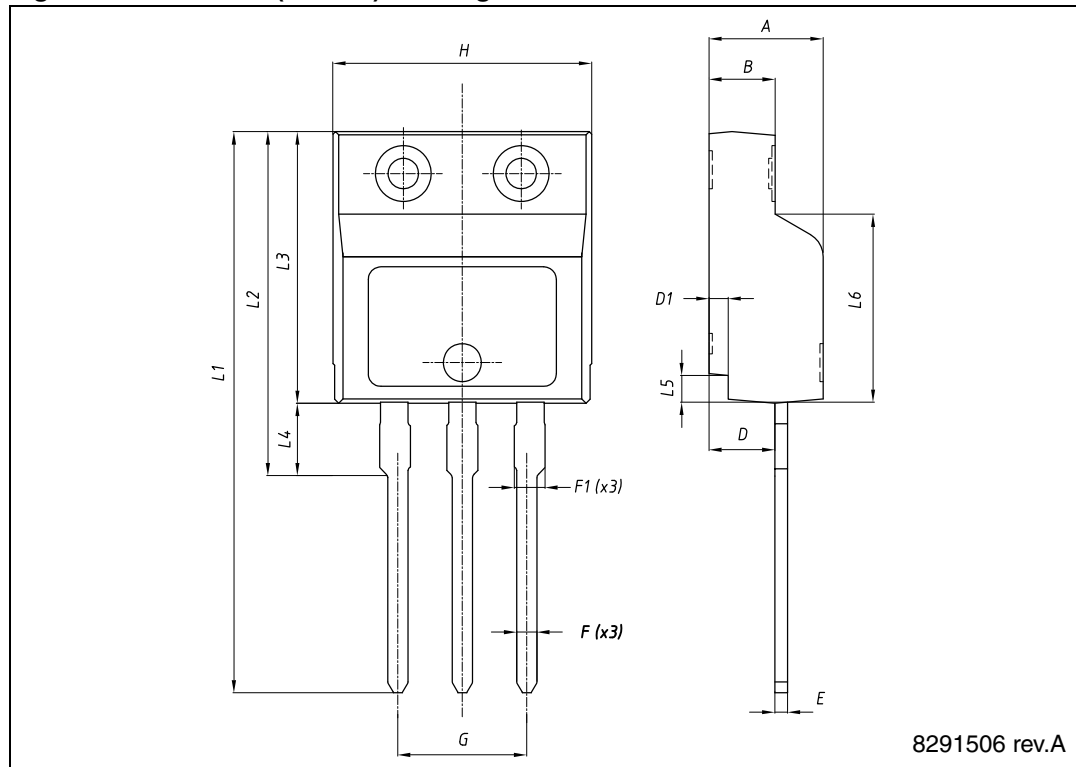
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 10. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 21. I²PAKFP (TO-281) drawing



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Jun-2011	1	First release
03-Nov-2011	2	<i>Figure 2: Safe operating area</i> and <i>Figure 3: Thermal impedance</i> have been added.
19-Mar-2012	3	Document status promoted from preliminary data to production data. Package name has been updated.

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