19-2740; Rev 1; 6/09

EVALUATION KIT AVAILABLE

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

General Description

The MAX1960/MAX1961/MAX1962 high-current, high-efficiency voltage-mode step-down DC-DC controllers operate from a 2.35V to 5.5V input and generate output voltages down to 0.8V at up to 20A. An on-chip charge pump generates a regulated 5V for MOSFET drive. Additionally, adaptive dead-time drivers allow a wide variety of MOSFETs to be used without risking shoot-through.

Fixed-frequency PWM operation and external synchronization make these controllers suitable for telecom and datacom applications. The operating frequency is programmable to either 500kHz or 1MHz, or from 450kHz to 1.2MHz with an external clock. A clock output is provided to synchronize another converter for 180° out-of-phase operation. A high closed-loop bandwidth provides excellent transient response for applications with dynamic loads.

Lossless current sensing in the MAX1960 and MAX1961 is achieved by monitoring the drain-to-source voltage of the low-side external FET. The current limit is scalable to accommodate a wide variety of MOSFETs and load currents. The MAX1962 has 10% accurate sense-resistor-based current limiting.

The MAX1960 and MAX1962 have an adjustable output voltage from 0.8V to 4.95V. The MAX1961 and MAX1962 have four preset output voltages (1.5V, 1.8V, 2.5V, and 3.3V) and feature 0.5% voltage accuracy over temperature, line, and load variations. The MAX1960 and MAX1961 also feature voltage-margining control inputs that shift the output voltage up or down by 4% for system testing.

Applications

ASIC, FPGA, DSP, and CPU Core and I/O Voltages

Cellular Base Stations

Telecom and Network Equipment

Server and Storage Systems

Pin Configurations and Selector Guide appear at the end of the data sheet.

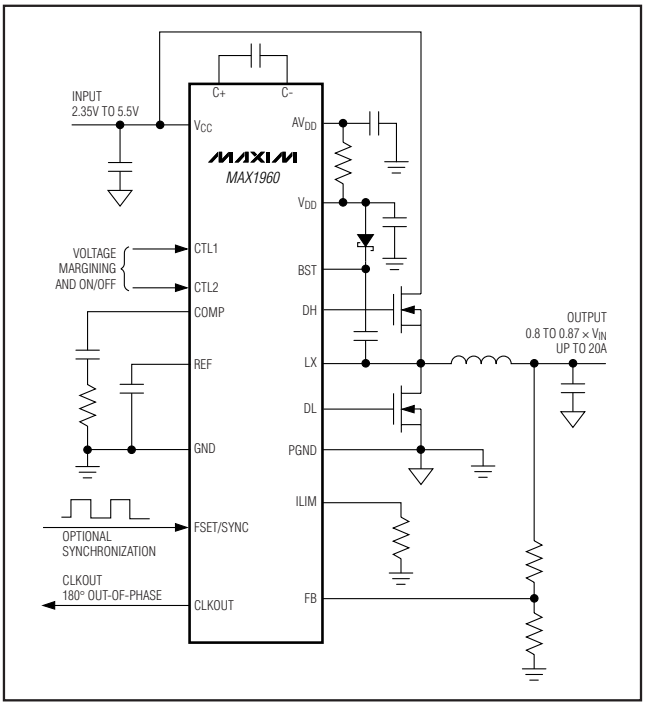
Features

- ♦ **0.5% Accurate Output**
- ♦ **Operates from 2.35V to 5.5V Supply**
- ♦ **Generates Low Output Voltage Down to 0.8V**
- ♦ **On-Chip Charge Pump Provides 5V Gate Drive**
- ♦ **Ceramic or Electrolytic Capacitors**
- ♦ **94% Efficiency**
- ♦ **External Synchronization from 450kHz to 1.2MHz**
- ♦ **500kHz/1MHz Fixed-Frequency PWM Operation**
- ♦ **Fast Transient Response**
- ♦ **Two Converters Can Operate 180° Out-of-Phase**
- ♦ **±4% Voltage Margining for System Test**
- ♦ **10% Accurate Current Sensing (MAX1962)**
- ♦ **Adaptive Dead Time Prevents Shoot-Through**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1960EEP	-40°C to +85°C	20 QSOP
MAX1961EEP	-40°C to +85°C	20 QSOP
MAX1962EEP	-40°C to +85°C	20 QSOP

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V_{CC}, CTL_, CS, FSET/SYNC, SEL, EN, OUT to GND ..... -0.3V to +6V
ILIM, COMP, REF, FB, CLKOUT, C- to GND ..... -0.3V to V_{AVDD} + 0.3V
C+ to GND ..... -0.3V to higher of V_{VCC} + 1V or V_{VDD} + 0.3V
V_{DD}, AV_{DD} to GND ..... -0.3V to higher of V_{VCC} - 0.3V or 6V
DL to PGND ..... -0.3V to V_{VDD} + 0.3V
BST to GND ..... -0.3V to +12V
DH to LX ..... -0.3V to +6V
LX to BST ..... -6V to +0.3V
PGND to GND, or V_{DD} to AV_{DD} ..... -0.3V to +0.3V

Continuous Power Dissipation (T_A = +70°C)
20-Pin QSOP (derate up to +70°C) 727mW
20-Pin QSOP (derate above +70°C) ..... 9.1mW/°C
Operating Temperature Range (Extended) ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VCC} = 3.3V, Circuits of Figures 9–12, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Input Voltage Range			2.35		5.5	V
V_{CC} Input Voltage UVLO	Rising or falling, hysteresis = 33mV (typ)		1.95		2.3	V
V_{DD} Input Voltage UVLO	Rising or falling, hysteresis = 44mV (typ)		3.9		4.45	V
Output Voltage			0.8			V
DC Output Accuracy	MAX1960/MAX1962 (measured at FB)		0.796	0.800	0.804	V
	MAX1961/ MAX1962 (FB = V_{DD}), measured at output	SEL = GND	1.492	1.500	1.508	
		SEL = REF	1.791	1.800	1.809	
		SEL not connected	2.487	2.500	2.514	
		SEL = V_{DD}	3.272	3.300	3.336	
Positive Voltage-Margining Shift	MAX1960/MAX1961		+3.8	+4	+4.2	%
Negative Voltage-Margining Shift	MAX1960/MAX1961		-3.8	-4	-4.2	%
Load Regulation Error	0V to full load			0.08		%
Line Regulation Error	V_{VCC} = 2.7V to 5.5V			0.1		%
FB Input Bias Current			-0.2		+0.2	µA
Feedback Transconductance			1	2	3	mS
COMP Discharge Resistance	In shutdown			10	100	Ω
DC-DC Soft-Start Time				1280		cycles
Switching Frequency	FSET/SYNC = GND		450	500	550	kHz
	FSET/SYNC = V_{CC}		880	1000	1120	
SYNC Frequency Range			450		1200	kHz
Maximum Duty Cycle	f = 1MHz		80	83		%
Maximum Duty Cycle	f = 500kHz		90	92		%
Quiescent Supply Current				11	15	mA
Shutdown Supply Current					15	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 3.3V, Circuits of Figures 9–12, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Output Voltage	2.7V ≤ V_{VCC} ≤ 5.5V, I_{LOAD} = 1mA to 50mA		4.75		5.25	V
	2.35V ≤ V_{VCC} ≤ 2.7V, I_{LOAD} = 1mA to 35mA, C1 = 4.7µF, C6 = 22µF (Note 1)		4.45		5.25	V
	2.35V ≤ V_{VCC} ≤ 3.6V with tripler, I_{LOAD} = 1 to 50mA (circuit of Figure 12) (Note 1)		4.75		5.25	V
Reference Voltage (No Load)			1.269	1.280	1.291	V
Reference Load Regulation	-50µA to +50µA			3		mV
Positive Current-Limit Threshold (V_{PGND} - V_{LX})	MAX1962	V_{OUT} = 0.8V	44	53	62	mV
		V_{OUT} = 2.0V	45	50	55	
		V_{OUT} = 3.3V	38	48	58	
Negative Current-Limit Threshold (V_{LX} - V_{PGND})	MAX1962, V_{OUT} = 0.8V to 3.3V		38	50	68	mV
CS Bias Current	MAX1962, V_{CS} = 3.3V			20	50	µA
OUT Bias Current	MAX1961/MAX1962, V_{OUT} = 3.3V			30	50	µA
Current-Limit Threshold (Positive Direction, Fixed, V_{PGND} - V_{LX})	MAX1960/MAX1961, ILIM = V_{DD}		58	74	90	mV
Current-Limit Threshold (Negative Direction, Fixed, V_{LX} - V_{PGND})	MAX1960/MAX1961, ILIM = V_{DD}		50	67	85	mV
Current-Limit Threshold (Positive Direction, Adjustable, V_{PGND} - V_{LX})	MAX1960/MAX1961, R_{ILIM} = 160kΩ		100	114	135	mV
	R_{ILIM} = 400kΩ		250	279	306	
Current-Limit Threshold (Negative Direction, Adjustable, V_{LX} - V_{PGND})	MAX1960/MAX1961, R_{ILIM} = 160kΩ		90	107	125	mV
	R_{ILIM} = 400kΩ		245	271	296	
Thermal-Shutdown Threshold	15°C hysteresis			+160		°C
DH Gate-Driver On-Resistance	V_{BST} - V_{LX} = 5V, pulling up or down			1.8	3.5	Ω
DL Gate-Driver On-Resistance (Pullup)	DL high state			1.8	3.5	Ω
DL Gate-Driver On-Resistance (Pulldown)	DL low state			0.5	1.6	Ω
Minimum Adaptive Dead Time	DH falling to DL rising			35		ns
	DH rising to DL falling			26		
FSET/SYNC Pulse Width	Minimum high time (Note 1)		200			ns
	Minimum low time (Note 1)		200			
FSET/SYNC Rise/Fall Time	(Note 1)				100	ns
CTL_, FSET/SYNC, EN Input High Voltage	V_{VCC} = 2.35V to 5.5V		2.0			V
CTL_, FSET/SYNC, EN Input Low Voltage	V_{VCC} = 2.35V to 5.5V				0.8	V
CTL_, FSET/SYNC, EN Input Current			-1		+1	µA
CLKOUT V_{OL}	Sinking 1mA			0.01	0.1	V
CLKOUT V_{OH}	Sourcing 1mA		V_{VCC} - 0.2V	V_{VCC} - 0.01V		V
CLKOUT Rise/Fall Time	C_{LOAD} = 100pF (Note 1)				40	ns

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

ELECTRICAL CHARACTERISTICS

(V_{VCC} = 3.3V, Circuits of Figures 9–12, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Input Voltage Range			2.35		5.50	V
V_{CC} Input Voltage UVLO	Rising or falling		1.95		2.3	V
V_{DD} Input Voltage UVLO	Rising or falling		3.90		4.45	V
Output Voltage			0.8			V
DC Output Accuracy	MAX1960/MAX1962 (measured at FB)		0.795		0.805	V
	MAX1961/MAX1962 ($FB = V_{DD}$), measured at output	SEL = GND	1.492		1.508	
		SEL = REF	1.789		1.809	
		SEL not connected	2.482		2.517	
		SEL = V_{DD}	3.272		3.339	
Positive Voltage-Margining Shift	MAX1960/MAX1961		3.8		4.2	%
Negative Voltage-Margining Shift	MAX1960/MAX1961		-3.8		-4.2	%
FB Input Bias Current			-0.2		+0.2	µA
Feedback Transconductance			1		3	mS
COMP Discharge Resistance	In shutdown				100	Ω
Switching Frequency	FSET/SYNC = GND		450		550	kHz
	FSET/SYNC = V_{CC}		880		1120	
SYNC Frequency Range			450		1200	kHz
Maximum Duty Cycle	f = 1MHz		80			%
Maximum Duty Cycle	f = 500kHz		90			%
Quiescent Supply Current					15	mA
Shutdown Supply Current					15	µA
V_{DD} Output Voltage	2.7V ≤ V_{VCC} ≤ 5.5V, I_{LOAD} = 1mA to 50mA		4.75		5.25	V
	2.35V ≤ V_{VCC} ≤ 2.7V, I_{LOAD} = 1mA to 35mA, C1 = 4.7µF, C6 = 22µF		4.45		5.25	
	2.35V ≤ V_{VCC} ≤ 3.6V with tripler, I_{LOAD} = 1mA to 50mA (circuit of Figure 12)		4.75		5.25	
Reference Voltage (No Load)			1.267		1.291	V
Positive Current-Limit Threshold (V_{CS} - V_{OUT})	MAX1962, V_{OUT} = 2V		45		56	mV
Negative Current-Limit Threshold (V_{OUT} - V_{CS})	MAX1962, V_{OUT} = 2V		42		64	mV
CS Bias Current	MAX1962, V_{CS} = 3.3V				50	µA
OUT Bias Current	MAX1961/MAX1962, V_{OUT} = 3.3V				50	µA
Current-Limit Threshold (Positive Direction, Fixed, V_{PGND} - V_{LX})	MAX1960/MAX1961, ILIM = V_{DD}		58		90	mV
Current-Limit Threshold (Negative Direction, Fixed, V_{LX} - V_{PGND})	MAX1960/MAX1961, ILIM = V_{DD}		50		85	mV
Current-Limit Threshold (Positive Direction, Adjustable, V_{PGND} - V_{LX})	MAX1960/MAX1961, R_{ILIM} = 160kΩ		100		135	mV
	R_{ILIM} = 400kΩ		250		306	

ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = 3.3V, Circuits of Figures 9–12, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Threshold (Negative Direction, Adjustable, V_{LX} - V_{PGND})	MAX1960/MAX1961, R_{ILIM} = 160kΩ	90		125	mV
	R_{ILIM} = 400kΩ	245		296	
DH Gate-Driver On-Resistance	V_{BST} - V_{LX} = 5V, pulling up or down			3.5	Ω
DL Gate-Driver On-Resistance (Pullup)	DL high state			3.5	Ω
DL Gate-Driver On-Resistance (Pulldown)	DL low state			1.6	Ω
FSET/SYNC Pulse Width	Minimum high time	200			ns
	Minimum low time	200			
FSET/SYNC Rise/Fall Time				100	ns
CTL_, FSET/SYNC, EN Input High Voltage	V_{VCC} = 2.35V to 5.5V	2.0			V
CTL_, FSET/SYNC, EN Input Low Voltage	V_{VCC} = 2.35V to 5.5V			0.8	V
CTL_, FSET/SYNC, EN Input Current		-1		+1	µA
CLKOUT V_{OL}	Sinking 1mA			0.1	V
CLKOUT V_{OH}	Sourcing 1mA	V_{VCC} - 0.2V			V
CLKOUT Rise/Fall Time	C_{LOAD} = 100pF			40	ns

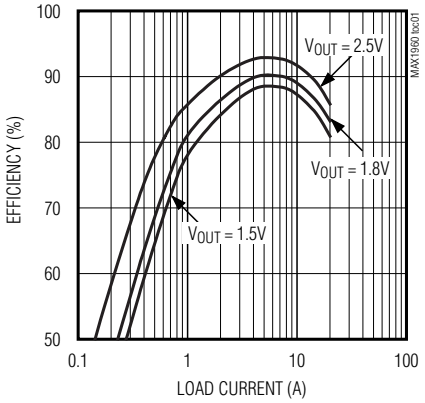
Note 1: Guaranteed by design.
Note 2: Specifications at -40°C are guaranteed by design, and not production tested.

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

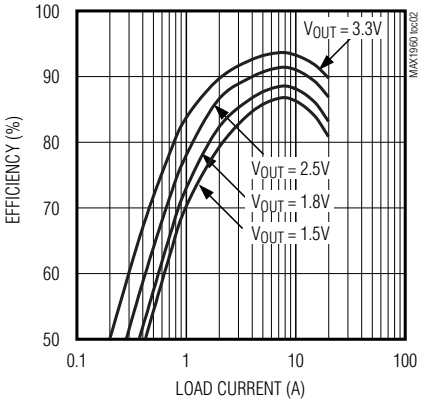
Typical Operating Characteristics

(Circuit of Figure 9, T_A = +25°C, unless otherwise noted.)

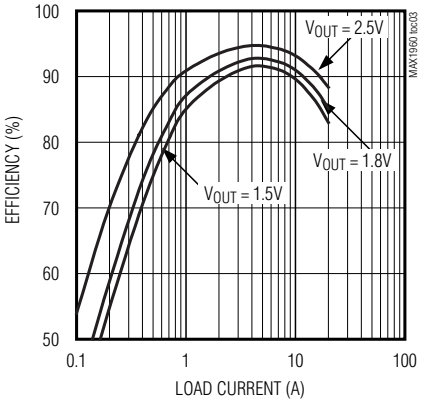
EFFICIENCY vs. LOAD CURRENT WITH 15A 1MHz CIRCUIT, 3.3V INPUT



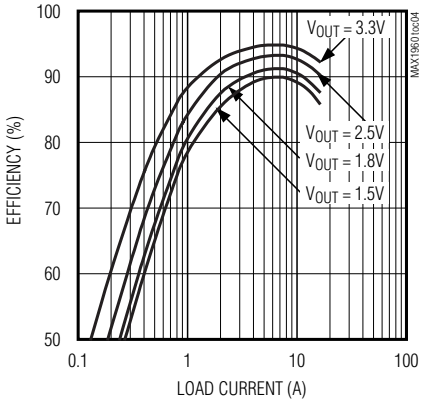
EFFICIENCY vs. LOAD CURRENT WITH 15A 1MHz CIRCUIT, 5V INPUT



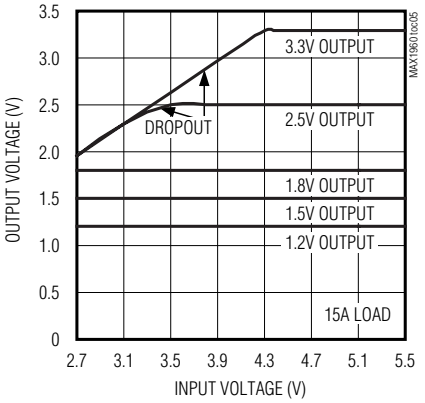
EFFICIENCY vs. LOAD CURRENT WITH 15A 500kHz CIRCUIT, 3.3V INPUT



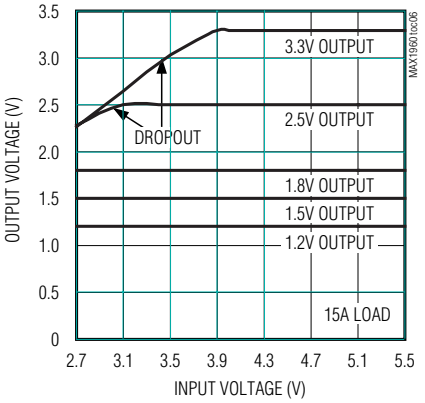
EFFICIENCY vs. LOAD CURRENT WITH 15A 500kHz CIRCUIT, 5V INPUT



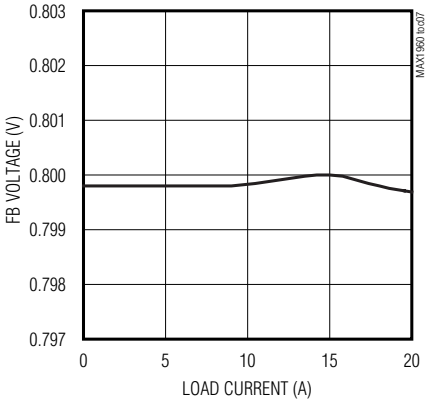
OUTPUT VOLTAGE vs. INPUT VOLTAGE, 1MHz



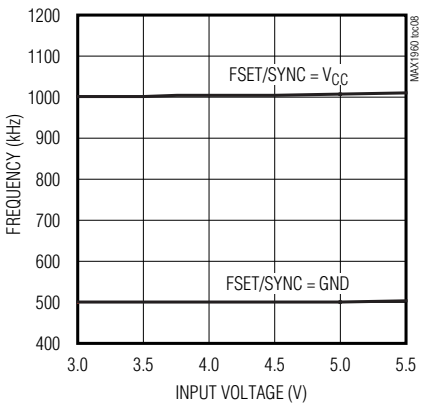
OUTPUT VOLTAGE vs. INPUT VOLTAGE, 500kHz



FB REGULATION VOLTAGE vs. LOAD CURRENT



FREQUENCY vs. INPUT VOLTAGE

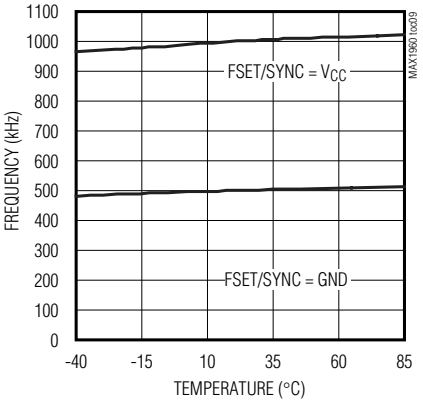


2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

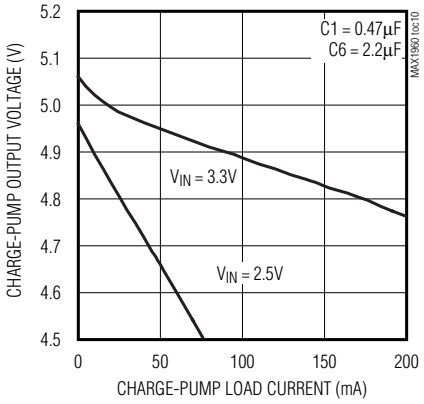
Typical Operating Characteristics (continued)

(Circuit of Figure 9, T_A = +25°C, unless otherwise noted.)

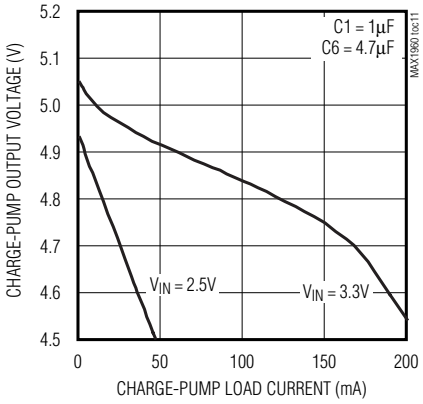
FREQUENCY vs. TEMPERATURE



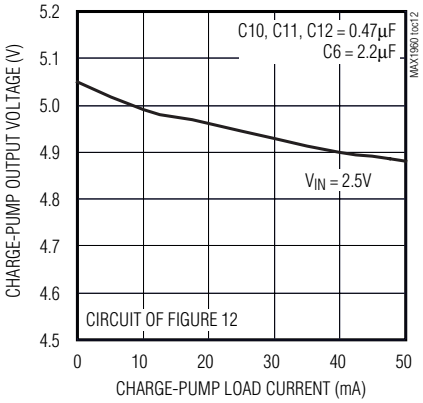
CHARGE-PUMP OUTPUT VOLTAGE vs. CHARGE-PUMP LOAD CURRENT, 1MHz



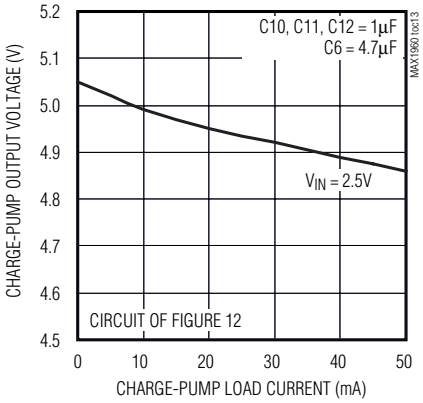
CHARGE-PUMP OUTPUT VOLTAGE vs. CHARGE-PUMP LOAD CURRENT, 500kHz



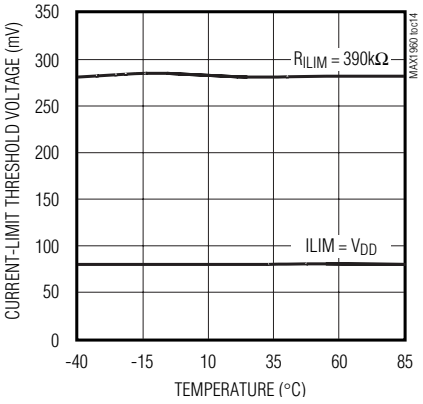
TRIPLER CHARGE-PUMP OUTPUT VOLTAGE vs. CHARGE-PUMP LOAD CURRENT, 1MHz



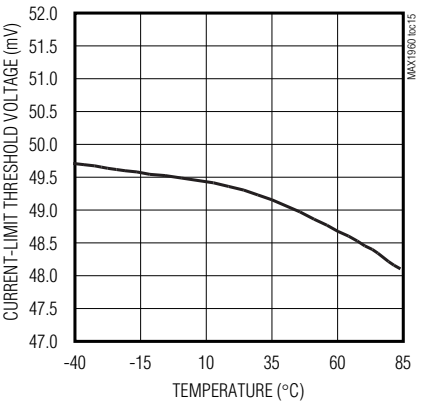
TRIPLER CHARGE-PUMP OUTPUT VOLTAGE vs. CHARGE-PUMP LOAD CURRENT, 500kHz



MAX1960/MAX1961 CURRENT-LIMIT THRESHOLD VOLTAGE vs. TEMPERATURE



MAX1962 CURRENT-LIMIT THRESHOLD VOLTAGE vs. TEMPERATURE

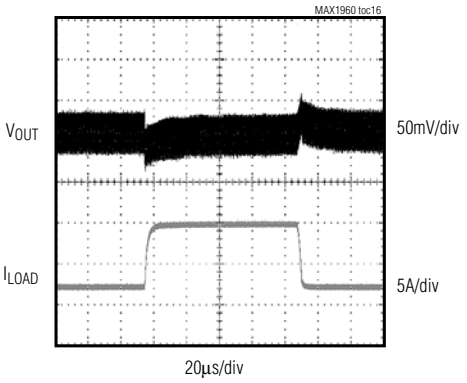


2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

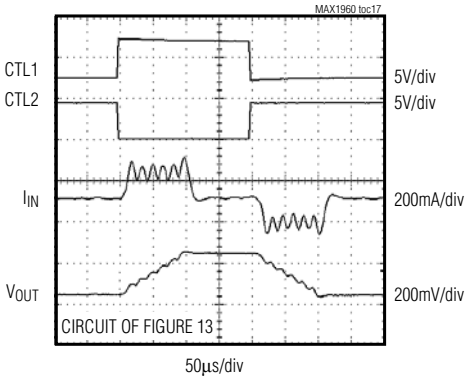
Typical Operating Characteristics (continued)

(Circuit of Figure 9, T_A = +25°C, unless otherwise noted.)

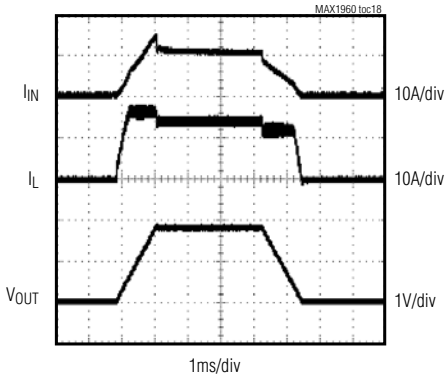
7.5A TO 15A TO 7.5A LOAD TRANSIENT



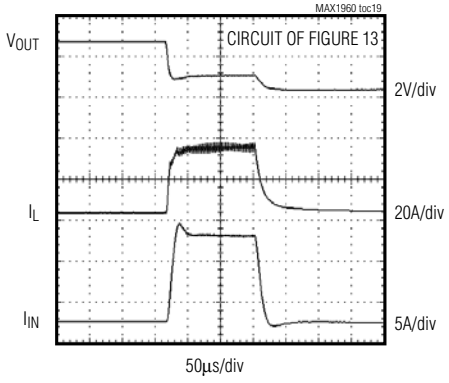
VOLTAGE-MARGINING STEP RESPONSE



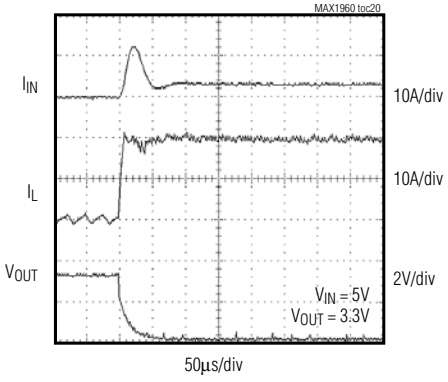
STARTUP/SHUTDOWN WAVEFORMS



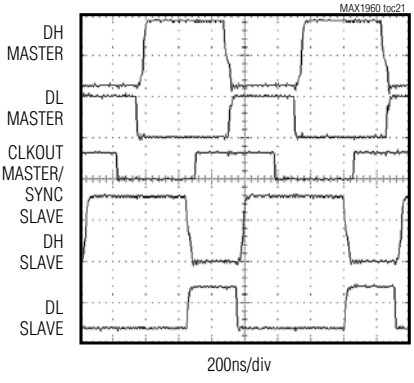
MAX1960/MAX1961 SHORT-CIRCUIT WAVEFORMS



MAX1962 SHORT-CIRCUIT WAVEFORMS



SYNC TIMING WAVEFORMS



Pin Description

PIN			NAME	FUNCTION
MAX1960	MAX1961	MAX1962		
1	1	1	CLKOUT	Clock Output. Connect to FSET/SYNC of a second converter to operate 180° out-of-phase. CLKOUT swings from V_{CC} to GND. CLKOUT is low in shutdown (see the *Operating Frequency and Synchronization* section).
2	2	2	FSET/SYNC	Frequency Set and Synchronization. Connect to GND for 500kHz operation, connect to V_{CC} for 1MHz operation, or drive with clock signal to synchronize (between 450kHz and 1200kHz).
3	3	—	ILIM	Current Limit. Connect a resistor from ILIM to GND to set the current-sense threshold voltage. Connect ILIM to V_{DD} to select the default threshold of 75mV.
—	—	3	EN	Enable. Drive high for normal operation. Drive low or connect to GND for shutdown mode.
—	4	4	SEL	Preset Output Voltage Select. Allows the output to be set to one of four preset voltages (1.5V, 1.8V, 2.5V, and 3.3V). For the MAX1962, FB must be connected to V_{DD} if SEL is to be used (see the *Setting the Output Voltage* section).
4	—	—	N.C.	No Connection. Not internally connected.
—	8	5	OUT	Output. Connect to the output. Used to sense the output voltage for internal feedback and current sense.
5	5	—	CTL1	Control Pins. Controls voltage margining and shutdown. Connect both CTL1 and CTL2 high for normal operation. Connect both CTL1 and CTL2 low for shutdown. Connect CTL1 high and CTL2 low for +4% voltage margining. Connect CTL1 low and CTL2 high for -4% voltage margining. If voltage margining is not to be used, connect CTL1 and CTL2 together and use to enable/shutdown the device.
6	6	—	CTL2	
—	—	6	CS	Current-Sense Input. Connect to the junction of the current-sense resistor and the inductor. The MAX1962 current-sense threshold is 50mV measured from CS to OUT.
7	7	7	AV_{DD}	Filtered Supply from V_{DD}. Connect a 1µF bypass capacitor. AV_{DD} is forced to V_{CC} in shutdown. **Do not apply an external load to AV_{DD}.**
8	—	8	FB	Feedback Input. The feedback threshold is 0.8V. Connect to the center of a resistive voltage-divider from the output to GND to set the output voltage to 0.8V or greater. On the MAX1962, connect FB to V_{DD} to select preset output voltages (see SEL).
9	9	9	COMP	Compensation Pin. COMP is forced to GND in shutdown, UVLO, or thermal fault.
10	10	10	REF	Reference Output. V_{REF} = 1.28V. Bypass with a 0.22µF capacitor to GND.
11	11	11	GND	Analog Ground. Connect to the PC board analog ground plane. Connect the PC board analog ground plane and power ground planes with a single connection.
12	12	12	V_{DD}	Charge-Pump Output. Provides regulated 5V to power the IC and gate drivers. Bypass with a 4.7µF ceramic capacitor for operating frequencies between 450kHz and 950kHz. Bypass with a 2.2µF ceramic capacitor for 1MHz operation. V_{DD} is internally forced to V_{CC} in shutdown. Do not apply an external load to V_{DD}.
13	13	13	DL	Low-Side MOSFET Synchronous Rectifier Gate-Driver Output. DL is high in shutdown.
14	14	14	PGND	Power Ground. Connect to the PC board power ground plane.

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1960	MAX1961	MAX1962		
15	15	15	C-	Charge-Pump Flying Capacitor Negative Connection. Use a 0.47µF ceramic capacitor at 1MHz, and 1µF between 450kHz and 950kHz.
16	16	16	C+	Charge-Pump Flying Capacitor Positive Connection. Use a 0.47µF ceramic capacitor at 1MHz and 1µF between 450kHz and 950kHz.
17	17	17	V_{CC}	Input Supply to Charge Pump
18	18	18	BST	Boost Capacitor Connection. Connect a 0.1µF ceramic capacitor from BST to LX.
19	19	19	DH	High-Side MOSFET Gate-Driver Output. DH is low in shutdown.
20	20	20	LX	Inductor Connection

Detailed Description

The MAX1960/MAX1961/MAX1962 are high-current, high-efficiency voltage-mode step-down DC-DC controllers that operate from 2.35V to 5.5V input and generate adjustable voltages down to 0.8V at up to 20A. An on-chip charge pump generates a regulated 5V for driving a variety of external N-channel MOSFETs.

Constant frequency PWM operation and external synchronization make these controllers suitable for telecom and datacom applications. The operating frequency is programmed externally to either 500kHz or 1MHz, or from 450kHz to 1.2MHz with an external clock. A clock output is provided to synchronize another converter for 180° out-of-phase operation.

A high closed-loop bandwidth provides excellent transient response for applications with dynamic loads.

Internal Charge Pump

An on-chip regulated charge pump develops 5V at 50mA (max) with input voltages as low as 2.35V. The output of this charge pump provides power for the internal circuitry, bias for the low-side driver (DL), and the bias for the boost diode, which supplies the high-side MOSFET gate driver (DH). The charge pump is synchronized with the DL driver signal and operates at 1/2 the PWM frequency.

The external MOSFET gate charge is the dominant load for the charge pump and is proportional to the PWM switching frequency. The charge pump must supply chip-operating current plus adequate gate current for both MOSFETs at the selected operating frequency. The required charge-pump output current is given by the formula:

$$I_{TOTAL} = I_{AVDD} + f_{OSC} (Q_{G1} + Q_{G2})$$

where I_{AVDD} is the current supplied to the IC through AV_{DD} (typically 2mA), f_{OSC} is the PWM switching frequency, Q_{G1} is the gate charge of the high-side MOSFET, and Q_{G2} is the gate charge of the low-side MOSFET. The MOSFETs must be chosen such that I_{TOTAL} does not exceed 50mA. For example, with 1MHz operation, $Q_{G1} + Q_{G2}$ should be less than 48nC.

Voltage Margining and Shutdown

The voltage-margining feature on the MAX1960/MAX1961 shifts the output voltage up or down by 4%. This is useful for the automatic testing of systems at high and low supply conditions to find potential hardware failures. CTL1 and CTL2 control voltage margining as outlined in Table 1.

A shutdown feature is included on all three parts, which stops switching the output drivers and the charge pump, reducing the supply current to less than 15µA. For the MAX1962, drive EN high for normal operation, or low for shutdown. For the MAX1960/MAX1961, drive both CTL1 and CTL2 high for normal operation, or drive CTL1 and CTL2 low for shutdown. For a simple enable/shutdown function with no voltage margining, connect CTL1 and CTL2 together and drive as one input.

Table 1. Voltage Margining Truth Table

CTL1	CTL2	FUNCTION
High	High	Normal operation
High	Low	+4% output-voltage shift
Low	High	-4% output-voltage shift
Low	Low	Shutdown

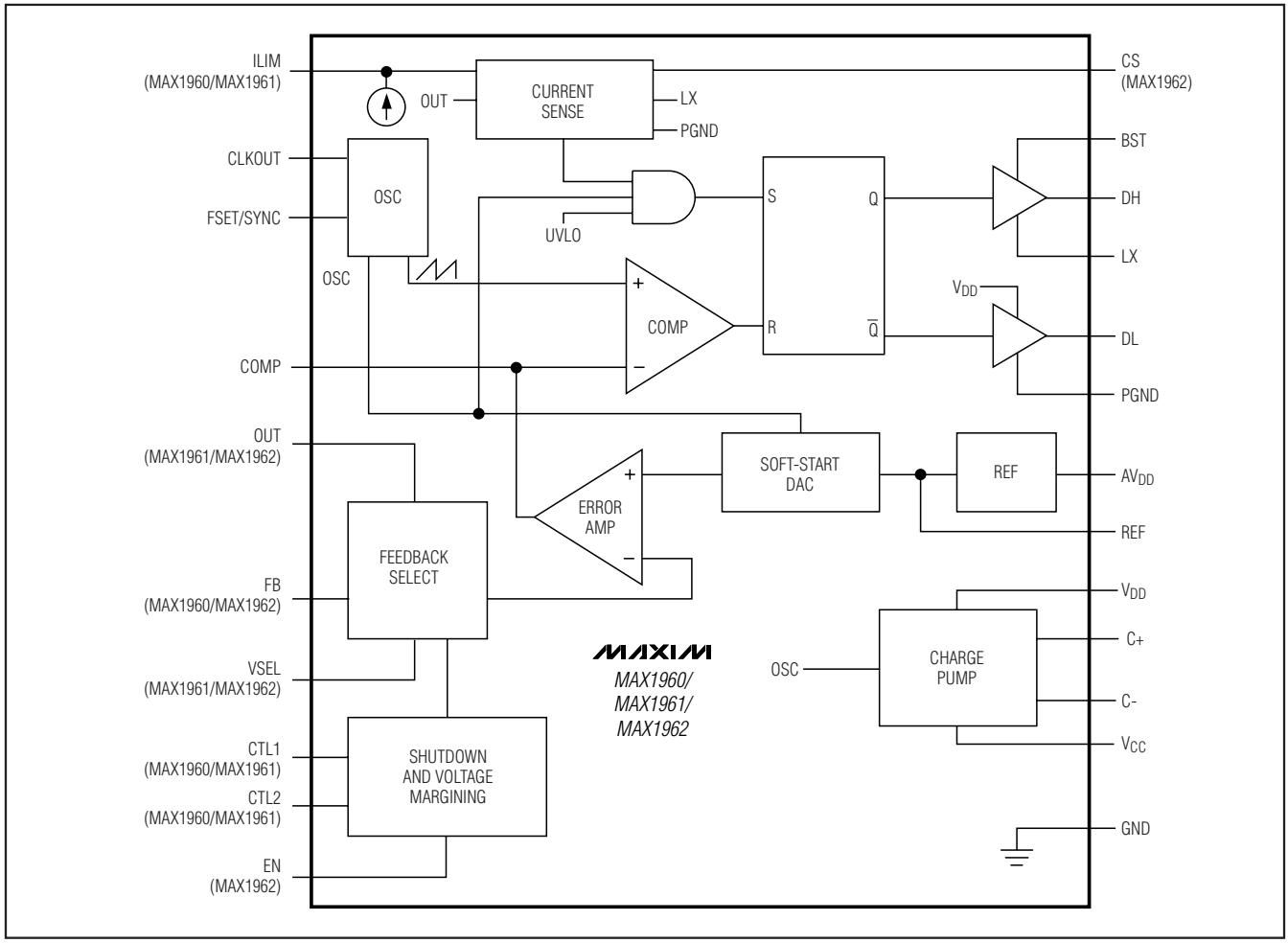


Figure 1. Functional Diagram

MOSFET Gate Drivers

The DH and DL drivers are designed to drive logic-level N-channel MOSFETs to optimize system cost and efficiency. MOSFETs with R_{DSON} rated at V_{GS} 4.5V are recommended. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate for the adaptive dead-time circuit to work properly. Otherwise, the internal sense circuitry could interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring no more than 20 squares (50mils to 100mils wide if the MOSFET is 1in from the IC).

Undervoltage Lockout and Soft-Start

There are two undervoltage lockout (UVLO) circuits on the MAX1960/MAX1961/MAX1962. The first UVLO circuit monitors V_{CC}, which must be above 2.15V (typ) in order for the charge pump to operate. The second UVLO circuit monitors the output of the charge pump. The charge-pump output, V_{DD}, must be above 4.2V (typ) in order for the PWM converter to operate. Both UVLO circuits inhibit switching and force DL high and DH low when either V_{CC} or V_{DD} are below their threshold. When the monitored voltages are above their thresholds, an internal soft-start timer ramps up the error-amplifier reference voltage. The ramp occurs in eighty 10mV steps. Full output voltage is reached 1.28ms after activation with a 1MHz operating frequency.

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Operating Frequency and Synchronization

The MAX1960/MAX1961/MAX1962 operating frequency is set externally to either 500kHz or 1MHz. For 500kHz operation, connect FSET/SYNC to GND, or for 1MHz operation, connect FSET/SYNC to V_{DD}. Alternately, an external clock from 450kHz to 1.2MHz can be applied to SYNC.

A clock output (CLKOUT) that is 180° out-of-phase with the internal clock is also provided. This allows a second converter to be synchronized, and operate 180° out-of-phase with the first. To do this, simply connect CLKOUT of the first converter to FSET/SYNC of the second converter. The first converter can be set internally to 500kHz or 1MHz for this mode of operation. When the first converter is synchronized to an external clock, CLKOUT is the inverse of external clock. See the SYNC Timing Waveform in the *Typical Operating Characteristics*.

Lossless Current Limit (MAX1960/MAX1961)

To prevent damage in the case of excessive load current or a short circuit, the MAX1960/MAX1961 use the low-side MOSFET's on-resistance ($R_{DS(ON)}$) for current sensing. The current is monitored during the on-time of the low-side MOSFET. If the current-sense voltage (V_{PGND} - V_{LX}) rises above the current-limit threshold for more than 128 clock cycles, the controller turns off. The controller remains off until the input voltage is removed or the device is re-enabled with CTL1 and CTL2 (see the *Setting the Current Limit* section).

Current-Sense Resistor (MAX1962)

The MAX1962 uses a standard current-sense resistor in series with the inductor for a 10% accurate current-limit measurement. The current-sense threshold is 50mV. This provides accurate current sensing at all duty cycles without relying on MOSFET on-resistance. CS connects to the high-side (inductor side) of the current-sense resistor and OUT connects to the low-side (output side) of the current-sense resistor.

The current-sense resistor for the MAX1962 may also be replaced with a series RC network across the inductor. This method uses the parasitic resistance of the inductor for current sensing. This method is less accurate than using a current-sense resistor, but is lower cost and provides slightly higher efficiency. See the *Design Procedure* section for instructions on using this method.

Dropout Performance

The MAX1960/MAX1961/MAX1962 enter dropout when the input voltage is not sufficiently high to maintain output regulation. As input voltage is lowered, the duty cycle increases until it reaches its maximum value, where the part enters dropout. With a switching frequency of 1MHz, the maximum duty cycle is about 83%. At 500kHz, the duty cycle can increase to about 92%, resulting in a lower dropout voltage. The duty cycle is dependent on the input voltage (V_{IN}), the output voltage (V_{OUT}), and the parasitic voltage drops in the MOSFETs and the inductor ($V_{DROP(N1)}$, $V_{DROP(N2)}$, $V_{DROP(L)}$). Note that $V_{DROP(L)}$ includes the voltage drop due to the inductor's resistance, the drop across the current-sense resistor (if used), and any other resistive voltage drop from the LX switching node to the point where the output voltage is sensed. The duty cycle is found from:

$$D = \frac{V_{OUT} + V_{DROP(L)}}{V_{IN} - V_{DROP(N1)} - V_{DROP(N2)}}$$

Adaptive Dead Time

The MAX1960/MAX1961/MAX1962 DL and DH MOSFET drivers have an adaptive dead-time circuit to prevent shoot-through current caused by high- and low-side MOSFET overlap. This allows a wide variety of MOSFETs to be used without matching FET dynamic characteristics. The DL driver will not go high until DH drives the high-side MOSFET gate to within 1V of its source (LX). The DH output will not go high until DL drives the low-side MOSFET gate to within 1V of ground.

Design Procedure

Component selection is primarily dictated by the following criteria:

Input voltage range. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high input voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and selector switches are considered.

Maximum load current. There are two values to consider: The *peak load current* ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and is key in determining output capacitor requirements. $I_{LOAD(MAX)}$ also determines the inductor saturation rating and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and is key in determining input capacitor requirements, MOSFET requirements, as well as those of other critical heat-contributing components.

Inductor operating point. This choice provides tradeoffs between size, transient response, and efficiency. Choosing higher inductance values results in lower inductor ripple current, lower peak current, lower switching losses, and, therefore, higher efficiency at the cost of slower transient response and larger size. Choosing lower inductance values results in large ripple currents, smaller size, and poorer efficiency, but have faster transient response.

Setting the Output Voltage

The MAX1961 has four output voltage presets selected by SEL. Table 2 shows how each of the preset voltages are selected. The MAX1962 also has four preset output voltages, but also is adjustable down to 0.8V. To use the preset voltages on the MAX1962, FB must be connected to V_{DD}. SEL then selects the output voltage as shown in Table 2.

Both the MAX1960/MAX1962 feature an adjustable output that can be set down to 0.8V. To set voltages greater than 0.8V, Connect FB to a resistor-divider from the output (Figures 9 and 11). Use a resistor up to 10kΩ for R2 and select R1 according to the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where the feedback threshold, V_{FB} = 0.8V, and V_{OUT} is the output voltage.

Input Voltage Range

The MAX1960/MAX1961/MAX1962 have an input voltage range of 2.35V to 5.5V but cannot operate at both extremes with one application circuit. The standard charge-pump doubler application circuit operates with an input range of 2.7V to 5.5V (Figures 9, 10, and 11). In order to operate down to 2.35V, the charge pump must be configured as a tripler. This circuit, however, limits the maximum input voltage to 3.6V. The schematic for the tripler charge pump is shown in Figure 2. Note that the flying capacitor between C+ and C- has been removed and C+ is not connected.

Inductor Selection

Determine an appropriate inductor value with the following equation:

$$L = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{V_{IN} \times f_{OSC} \times LIR \times I_{LOAD(MAX)}}$$

The inductor current ripple, LIR, is the ratio of peak-to-peak inductor ripple current to the average continuous inductor current. An LIR between 20% and 40% provides a good compromise between efficiency and economy. Choose a low-loss inductor having the lowest possible DC resistance. Ferrite core type inductors are often the best choice for performance. The inductor saturation current rating must exceed I_{PEAK}:

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{LIR}{2} \right) \times I_{LOAD(MAX)}$$

Table 2. Preset Voltages—MAX1961/MAX1962

PRESET OUTPUT VOLTAGE	SEL
1.5V	GND
1.8V	REF
2.5V	No connection
3.3V	V_{DD}

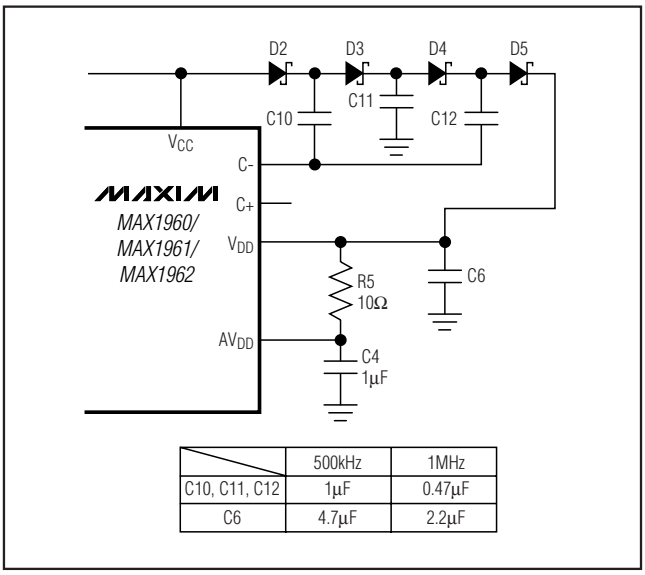

Figure 2. Tripler Charge-Pump Configuration.

Setting the Current Limit

Lossless Current Limit (MAX1960/MAX1961)

The MAX1960/MAX1961 use the low-side MOSFET's on-resistance ($R_{DS(ON)}$) for current sensing. This method of current limit sets the maximum value of the inductor's "valley" current (Figure 3). If the inductor current is higher than the valley current-limit setting at the end of the clock period, the controller skips the DH pulse. When the first current-limit event is detected, the controller initi-

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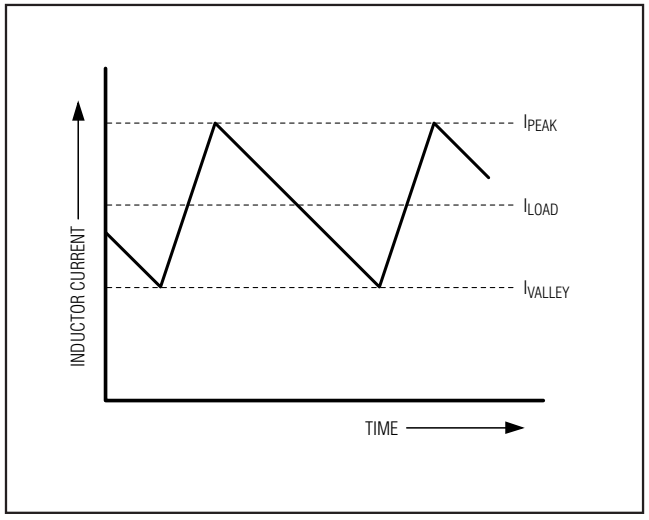

Figure 3. Inductor Current Waveform

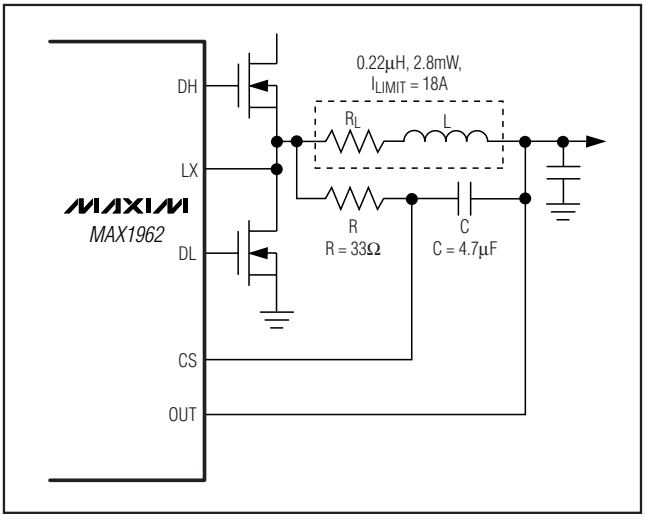

Figure 4. Using the Inductor Resistance as a Current-Sense Resistor with the MAX1962

ates a 128 clock cycle counter. If the current limit is present at the end of this count, the controller remains off until the input voltage is removed and re-applied, or the device is re-enabled with CTL1 and CTL2. The 128-cycle counter is reset when four successive DH pulses are observed, without activating the current limit.

At maximum load, the low excursion of inductor current, $I_{VALLEY(MAX)}$, is:

$$I_{VALLEY(MAX)} = I_{LOAD(MAX)} - \left(\frac{LIR}{2}\right) \times I_{LOAD(MAX)}$$

The current-limit threshold (V_{CLT}) is set by connecting a resistor (R_{ILIM}) from ILIM to GND. The range for this resistor is 100kΩ to 400kΩ. Set current-limit threshold as follows:

$$V_{CLT} = R_{ILIM} \times 0.714\mu A$$

Connecting ILIM to V_{DD} sets the threshold to a default value of 75mV.

To prevent the current limit from falsely triggering, V_{CLT} divided by the low-side MOSFET $R_{DS(ON)}$ must exceed the maximum value of I_{VALLEY}. The maximum value of low-side MOSFET $R_{DS(ON)}$ should be used:

$$V_{CLT} > R_{DS(ON)MAX} \times I_{VALLEY(MAX)}$$

A limitation of sensing current across MOSFET on-resistance is that the MOSFET on-resistance varies significantly from MOSFET to MOSFET and over temperature. Consequently, this current-sensing method may not be suitable if a precise current limit is required. If better accuracy is needed, use the MAX1962 with a current-sense resistor.

Current-Sense Resistor (MAX1962)

The MAX1962 uses a current-sense resistor connected from the inductor to the output with Kelvin sense connections. The current-sense voltage is measured from CS to OUT, and has a fixed threshold of 50mV. The MAX1962 current limit is triggered when the peak voltage across the current-sense resistor, $I_{PEAK} \times R_{SENSE}$, exceeds 50mV. Once current sense is triggered, the controller does not turn off, but continues to operate at the current limit. This method of current sensing is more precise due to the accuracy of the current-sense resistor. The cost of this precision is that it requires an extra component and is slightly less efficient due to the loss in the current-sense resistance.

Inductor Resistance Current Sense (MAX1962)

Alternately, the inductor resistance can be used to sense current in place of a current-sense resistor. To do this, connect a series RC network in parallel with the inductor (Figure 4). Choose a resistor value less than 40Ω to avoid offsets due to CS input current. Calculate the capacitor value from the formula $C = 2L / (R_L \times R)$. The effective current-sense resistance (R_{SENSE}) equals R_L. Current-sense accuracy then depends on the accuracy of the inductor resistance. Note that the current-sense signal is delayed due to the RC filter time constant. Consequently, inductor current may overshoot (by as much as 2x) when a fast short occurs.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load transient requirements. In addition, the capacitance value must be high enough to absorb the inductor energy during load steps.

In applications where the output is subject to large load transients, low ESR is needed to prevent the output from dipping too low (V_{DIP}) during a load step:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOADSTEP(MAX)}}$$

In applications with less severe load steps, maximum ESR may be governed by what is needed to maintain acceptable output voltage ripple:

$$R_{ESR} \le \frac{V_{RIPPLE(P-P)}}{LIR \times I_{LOAD(MAX)}}$$

To satisfy both load step and ripple requirements, select the lowest value from the above two equations.

The capacitor is usually selected by physical size, ESR, and voltage rating, rather than by capacitance value. With current tantalum, electrolytic, and polymer capacitor technology, the bulk capacitance will also be sufficient once the ESR requirement is satisfied.

When using low-capacity filter capacitors such as ceramic, capacitor size is usually determined by the capacitance needed to prevent voltage undershoot and overshoot during load transients. The overshoot voltage (V_{SOAR}) is given by:

$$V_{SOAR} = \frac{L \times (I_{PEAK})^2}{2 \times V_{OUT} \times C_{OUT}}$$

Generally, once enough capacitance is in place to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection. The source impedance to the input supply largely determines the value of C_{IN}. High source impedance requires high input capacitance. The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents.

The RMS input ripple current is given by:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

Compensation and Stability

Compensation with Ceramic Output Capacitors

The high switching frequency range of the MAX1960/MAX1961/MAX1962 allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is very low typically, the frequency of the associated transfer function zero is higher than the unity-gain crossover frequency and the zero cannot be used to compensate for the double pole created by the output inductor and capacitor. The solution is Type 3 compensation (Figure 5), which takes advantage of local feedback to create two zeros and three poles (Figure 6). The frequency of the poles and zeros are described below:

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times C3}$$

$$f_{P3} = \frac{1}{2\pi \times R1 \times \frac{C1 \times C2}{C1 + C2}}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L_0 \times C_0}}$$

$$f_{Z1} = \frac{1}{2\pi \times R1 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times (R2+R3) \times C3}$$

$$f_{ZESR} = \frac{1}{2\pi \times R_{ESR} \times C_0}$$

Unity-gain crossover frequency:

$$f_0 = R1 \times C3 \times \frac{V_{IN(MAX)}}{V_{RAMP}} \times \frac{1}{2\pi \times L_0 \times C_0}$$

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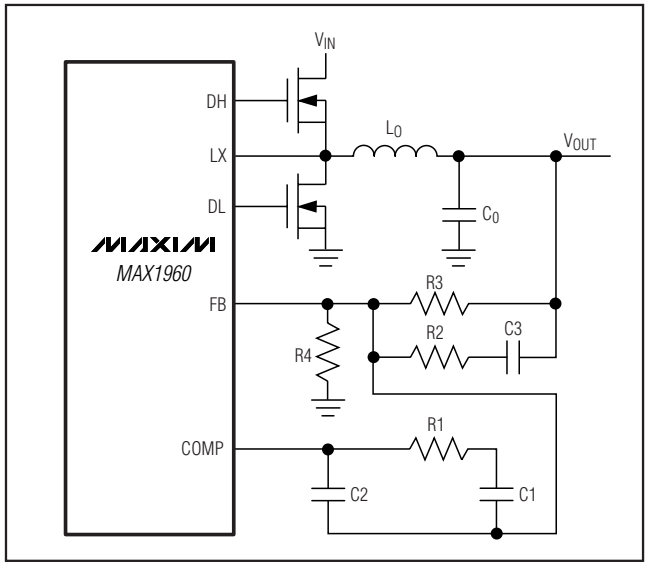


Figure 5. Type 3 Compensation Network

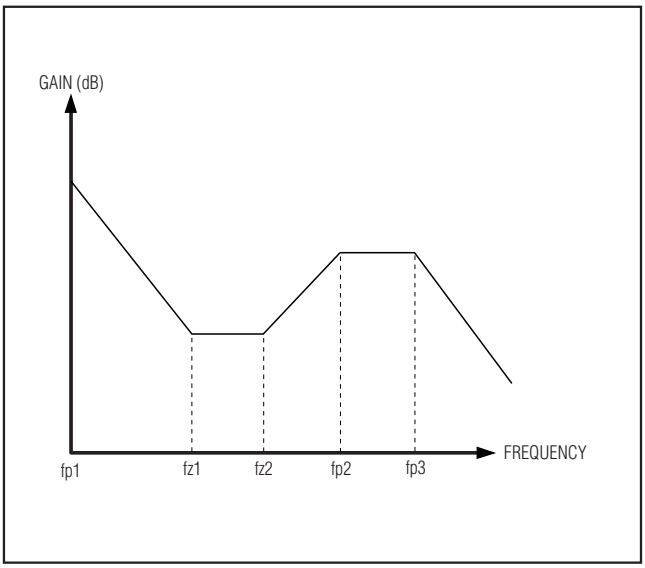


Figure 6. Transfer Function for Type 3 Compensation

where:

$V_{IN(MAX)}$ = Maximum input voltage

V_{RAMP} = Oscillator ramp voltage = $0.85 \times 10^6/f_S$, where f_S = switching frequency

L_O = Output inductance

C_O = Output capacitance

The goal is to place the two zeros below crossover and the two poles above crossover so that crossover occurs with a single-pole slope. The compensation procedure is as follows:

Select the crossover frequency such that:

$$f_0 < f_{ZESR} \text{ and } f_0 < 1/5 \times f_S$$

Select R1 such that:

$$R1 >> \frac{2}{g_{mEA}}$$

where g_{mEA} = 2mS.

Place the first zero before the double pole:

$$C1 \geq \frac{1}{2\pi \times 0.75 \times f_{LC} \times R1}$$

Place the third pole at half the switching frequency:

$$C2 \geq \frac{1}{2\pi \times 0.5 \times f_S \times R1}$$

If C2 < 10pF, it can be omitted.

$$C3 \leq \frac{2\pi \times f_0 \times L_0 \times C_0 \times V_{RAMP}}{R1 \times V_{IN}}$$

Place the second pole after the ESR zero:

$$R2 \leq \frac{1}{2\pi \times f_{ZESR} \times C3}$$

If:

$$R2 < \frac{1}{g_{mEA}},$$

where g_{mEA} = 2mS

increase R1 and recalculate C1, C2, and C3.

Place the second zero at the double-pole frequency:

$$R3 \geq \frac{1}{2\pi \times f_{LC} \times C3} - R2$$

Set the output voltage:

$$R4 = \frac{V_{FB}}{V_{OUT} - V_{FB}} \times R3, \; V_{FB} = 0.8V$$

Compensation with Electrolytic Output Capacitors

The MAX1960/MAX1961/MAX1962 use a voltage-mode control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with a fixed internal ramp to produce the required duty cycle. The inductor and output capacitor create a double pole at the resonant frequency, which has gain drop of 40dB per decade, and phase shift of 180°. The error amplifier must compensate for this gain drop and phase shift in order to achieve a stable high-bandwidth, closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider and an error amplifier. The power modulator has DC gain set by V_{IN}/V_{RAMP}, with a double pole set by the inductor and output capacitor, and a single zero set by the output capacitor (C_O) and its equivalent series resistance (ESR). Below are equations that define the power modulator:

The DC gain of the power modulator is:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

where $V_{RAMP} = 0.85 \times 10^6 / f_S$. The pole frequency due to the inductor and output capacitor is:

$$f_{PMOD} = \frac{1}{2\pi\sqrt{L_O C_O}}$$

The zero frequency due to the output capacitor's ESR is:

$$f_{ZESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

The output capacitor is usually comprised of several same value capacitors connected in parallel. With n capacitors in parallel, the output capacitance is:

$$C_O = n \times C_{EACH}$$

The total ESR is:

$$R_{ESR} = \frac{R_{ESR(EACH)}}{n}$$

The ESR zero (f_{ZESR}) for a parallel combination of capacitors is the same as for an individual capacitor.

The feedback divider has a gain of $G_{FB} = V_{FB}/V_{OUT}$, where V_{FB} is 0.8V.

The transconductance error amplifier has DC gain GEA(dc) of 80dB. A dominant pole is set by the compensation capacitor (C_C), the amplifier output resistance (R_O), and the compensation resistor (R_C):

$$f_{PEA} = \frac{1}{2\pi \times C_C \times (R_0 + R_C)}$$

A zero is set by the compensation resistor and the compensation capacitor:

$$f_{ZEA} = \frac{1}{2\pi \times C_C \times R_C}$$

The total closed-loop gain must equal to unity at the crossover frequency, where the crossover frequency should be higher than f_{ZESR}, so that the -1 slope is used to cross over at unity gain. Also, the crossover frequency should be less than or equal to 1/5 the switching frequency.

$$f_{ZESR} < f_C \le \frac{f_S}{5}$$

The loop-gain equation at the crossover frequency is:

$$\frac{V_{FB}}{V_{OUT}} \times G_{EA(f_C)} \times G_{MOD(f_C)} = 1$$

where:

$$G_{EA(f_C)} = g_{mEA} \times R_C$$

and:

$$G_{MOD(f_C)} = G_{MOD(DC)} \times \frac{(f_{PMOD})2}{f_{ESR} \times f_C}$$

The compensation resistor, R_C, is calculated from:

$$R_C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(f_C)}}$$

where g_{mEA} = 2mS.

Due to the under-damped (Q > 1) nature of the output LC double pole, the error-amplifier compensation zero should be approximately $0.2f_{PMOD}$ to provide good phase boost. C_C is calculated from:

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

$$C_C = \frac{5}{2\pi \times R_C \times f_{PMOD}}$$

A small capacitor C_F, can also be added from COMP to GND to provide high-frequency decoupling. C_F will add another high-frequency pole (f_{PHF}) to the error-amplifier response. This pole should be greater than 100 times the error-amplifier zero frequency to have negligible impact on the phase margin. This pole should also be less than half the switching frequency for effective decoupling:

$$100f_{ZEA} < f_{PHF} < 0.5f_S$$

Select a value for f_{PHF} in the range given above, then solve for C_F using the following equation:

$$C_F = \frac{1}{2\pi \times R_C \times f_{PHF}}$$

Below is a numerical example to calculate compensation values:

V_{IN} = 3.3V

V_{RAMP} = 0.85V

V_{OUT} = 1.8V

V_{FB} = 0.8V

$I_{OUT(max)}$ = 15A

C_O = 2 x 680µF = 1360µF

ESR = 0.008Ω / 2 = 0.004Ω

L_O = 0.22µH

g_{mEA} = 2mS

f_S = 1MHz

$$f_{PMOD} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} = \frac{1}{2\pi \times \sqrt{0.22 \times 10^{-6} \times 1360 \times 10^{-6}}} = 9.201\text{kHz}$$

$$f_{ZESR} = \frac{1}{2\pi \times C_O \times R_{ESR}} = \frac{1}{2\pi \times 1360 \times 10^{-6} \times 0.004} = 29.3\text{kHz}$$

Choose the crossover frequency (f_C) in the range $f_{ZESR} < f_C < f_S/5$:

$$29.3\text{kHz} < f_C < 200\text{kHz}$$

Select f_C = 100kHz, this meets the criteria above, and the bandwidth is high enough for good transient response.

The power modulator gain at f_C is:

$$G_{MOD(fc)} = \frac{V_{IN}}{V_{RAMP}} \times \frac{(f_{PMOD})^2}{f_{ZESR} \times f_C} = \frac{3}{0.85} \times \frac{(9201)^2}{29.3\text{k}\Omega \times 100\text{k}\Omega} = 0.102$$

Choose R_1 = 8.06kΩ, then R_2 = 10kΩ (see the *Setting the Output Voltage* section):

$$C = \frac{V_{OUT}}{g_{mEA} \times V_{FB} \times G_{MOD(f_C)}} = \frac{1.8}{0.002 \times 0.8 \times 0.102} = 11\text{k}\Omega$$

$$C_C = \frac{5}{2\pi \times R_C \times f_{PMOD}} = \frac{5}{2\pi \times 11\text{k}\Omega \times 9201} = 7863\text{pF}$$

Select C_C = 8200pF (nearest standard capacitor value).

Select f_{PHF} in the range $100f_{ZEA} < f_{PHF} < 0.5f_S$.

$$184\text{kHz} < f_{PHF} < 500\text{kHz}$$

Select f_{PHF} = 250kHz, then solve for C_F:

$$C_F = \frac{1}{2\pi \times R_C \times f_{PHF}} = \frac{1}{2\pi \times 11\text{k}\Omega \times 250\text{kHz}} = 58\text{pF}$$

Select the nearest standard capacitor value C_F = 56pF.

Summary of feedback divider and compensation components:

R_1 = 8.06kΩ

R_2 = 10kΩ

R_C = 11kΩ

C_C = 8200pF

C_F = 56pF

Power MOSFET Selection

When selecting a MOSFET, essential parameters include:

(1) Total gate charge (Q_G)

(2) Reverse transfer capacitance (C_{RSS})

(3) On-resistance ($R_{DS(ON)}$)

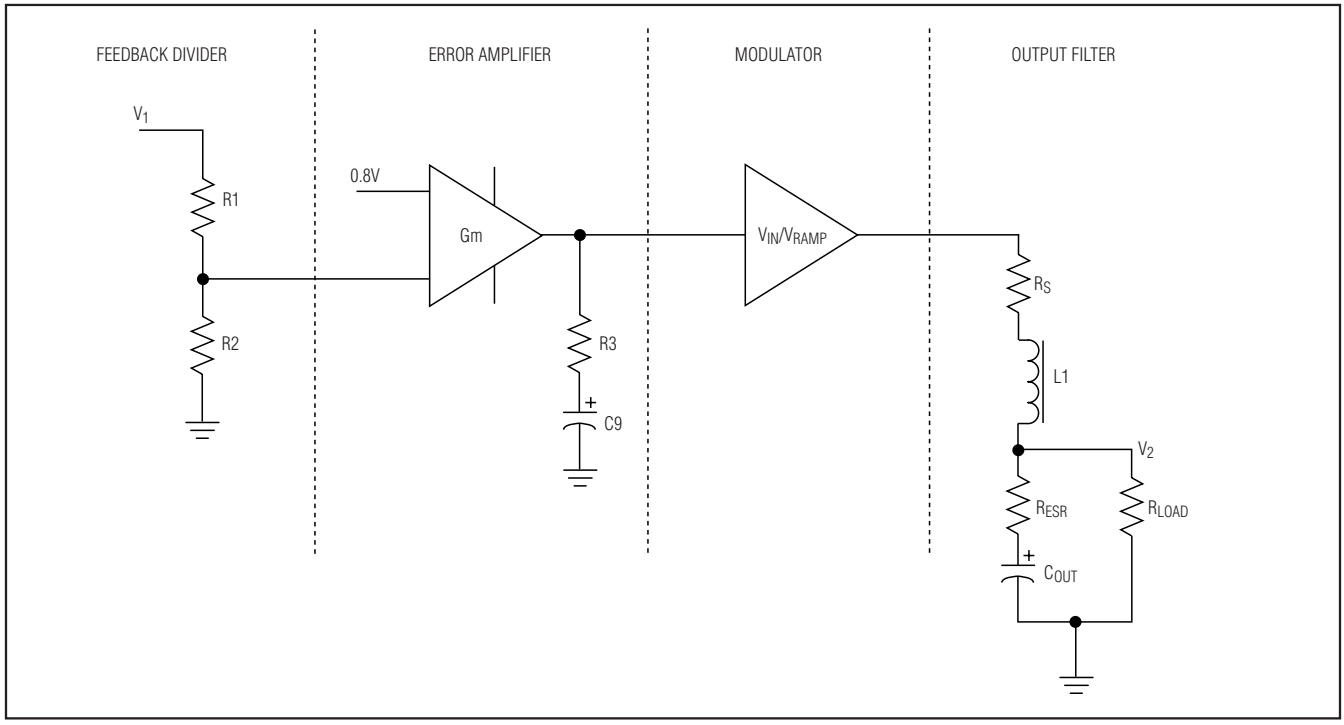


Figure 7. Open-Loop Transfer Model

(4) Gate threshold voltage ($V_{TH(MIN)}$)

(5) Turn-on/turn-off times

(6) Turn-on/turn-off delays

At high switching rates, dynamic characteristics (parameters 1, 2, 5, and 6) that predict switching losses may have more impact on efficiency than $R_{DS(ON)}$, which predicts DC losses. Q_G includes all capacitance associated with charging the gate, and best performance is achieved with a low total gate charge. Q_G also helps predict the current needed to drive the gate at the selected operating frequency. This is very important because the output current from the charge pump is finite (50mA, max) and is used to drive the gates of the MOSFETs as well as provide bias for the IC. $R_{DS(ON)}$ is important as well, as it is used for current sensing in the MAX1960/MAX1961. $R_{DS(ON)}$ also causes power dissipation during the on-time of the MOSFET.

Choose Q_G to be as low as possible. Ensure that:

$$Q_{G1} + Q_{G2} \le \frac{50mA}{f_S}$$

Choose $R_{DS(ON)}$ to provide the desired $I_{LOAD(MAX)}$ at the desired current-limit threshold voltage (see the *Setting the Current Limit* section).

MOSFET RC Snubber Circuit

Fast-switching transitions can cause ringing due to resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX rising and falling transitions, and may introduce current-sensing errors and generate EMI. To dampen this ringing, a series RC snubber circuit can be added across each MOSFET switch (Figure 8). Typical values for the snubber components are C_{SNUB} = 4700pF and R_{SNUB} = 1Ω, however, the ideal values for snubber components will depend on circuit parasitics. Below is the procedure for selecting the component values of the series RC snubber circuit:

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R.

2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

3) The circuit parasitic capacitance, C_{PAR}, at LX is then equal to 1/3 of the value of the added capacitance above.

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

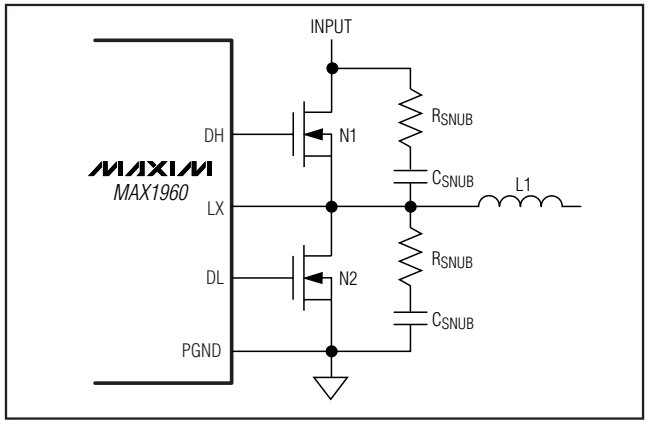


Figure 8. RC Snubber Circuit

4) The circuit parasitic inductance, L_{PAR}, is calculated by:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}}$$

5) The resistor for critical dampening, $R_{SNUB} = 2\pi \times f_R \times L_{PAR}$. The resistor value can be adjusted up or down to tailor the desired damping and the peak voltage excursion.

6) The capacitor, C_{SNUB}, should be at least 2 to 4 times the value of the C_{PAR} to be effective.

7) The snubber circuit power loss is dissipated in the resistor, P_{RSNUB}, and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_S$$

where V_{IN} is the input voltage, and f_S is the switching frequency. Choose R_{SNUB} power rating that exceeds the calculated power dissipation.

MOSFET Power Dissipation

Worst-case power dissipation occurs at duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum input voltage ($V_{IN(MIN)}$):

$$PD_{(N1RESISTIVE)} = \frac{V_{OUT}}{V_{IN(MIN)}} \times I_{LOAD}^2 \times R_{DS(ON)}$$

The following formula calculates switching losses for the high-side MOSFET, but is only an approximation and not a substitute for evaluation:

$$P_{D(N1SWITCHING)} =$$

$$\left(I_{L(PEAK)} \times t_{FALL} + I_{L(VALLEY)} \times t_{RISE}\right) \times \frac{V_{IN(MAX)}}{2} \times f_S$$

where $V_{IN(MAX)}$ is the maximum value of the input voltage, t_{FALL} and t_{RISE} are the fall and rise time of the MOSFET, $I_{L(PEAK)}$ and $I_{L(VALLEY)}$ are the maximum peak and valley inductor current, and f_S is the PWM switching frequency:

$$I_{L(PEAK)} = I_{OUT(MAX)} \times (1 + 0.5 \times LIR) \text{ and } I_{L(VALLEY)} = I_{OUT(MAX)} \times (1 - 0.5 \times LIR)$$

where LIR is the peak-to-peak inductor ripple current divided by the load current.

The total power dissipation in the high-side MOSFET is the sum of these two power losses:

$$P_{D(N1)} = P_{D(N1RESISTIVE)} + P_{D(N1SWITCHING)}$$

For the low-side MOSFET, the worst-case power dissipation occurs at maximum input voltage:

$$P_{D(N2RESISTIVE)} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Applications Information

PC Board Layout Guidelines

A properly designed PC board layout is important in any switching DC-DC converter circuit. If possible, mount the MOSFETs, inductor, input/output capacitors, and current-sense resistor on the top side. Connect the ground for these devices close together on a power-ground trace. Make all other ground connections to a separate analog ground plane. Connect the analog ground plane to power ground at a single point.

To help dissipate heat, place high-power components (MOSFETs, inductor, and current-sense resistor) on a large PC board area. Keep high-current traces short and wide to reduce the resistance in these traces. Also make the gate drive connections (DH and DL) short and wide, measuring 10 to 20 squares (50mils to 100mils wide if the MOSFET is 1in from the controller IC).

For the MAX1960/MAX1961, connect LX and PGND to the low-side MOSFET using Kelvin sense connections. For the MAX1962, connect CS and OUT to the current-sense resistor using Kelvin sense connections.

Place the REF capacitor, the BST diode and capacitor, and the charge-pump components as close as possible to the IC. If the IC is far from the input capacitors, bypass V_{CC} to GND with a 0.1µF or greater ceramic capacitor close to the V_{CC} pin.

For an example PC board layout, see the MAX1960 evaluation kit.

Table 3. Component List for Application Circuits

PART	APP. CIRCUIT	15A OUTPUT 1MHz	15A OUTPUT 500kHz
C1	1, 2, 3	0.47µF ceramic capacitor	1µF ceramic capacitor
C2	1, 2, 3, 4	5 × 10µF ceramic capacitors	5 × 10µF ceramic capacitors
C3	1, 2, 3, 4	2 x 680µF POSCAPs Sanyo 2R5TPD680M8	2 x 680µF POSCAPs Sanyo 2R5TPD680M8
C4	1, 2, 3, 4	1µF ceramic capacitor	1µF ceramic capacitor
C5	1, 2, 3, 4	0.1µF ceramic capacitor	0.1µF ceramic capacitor
C6	1, 2, 3, 4	2.2µF ceramic capacitor	4.7µF ceramic capacitor
C8	1, 2, 3, 4	0.22µF ceramic capacitor	0.22µF ceramic capacitor
C9	1, 2, 3, 4	(Table 4)	(Table 5)
C10, C11, C12	4	0.47µF ceramic capacitors	1µF ceramic capacitors
C13, C14	1, 2, 3, 4	4700pF ceramic capacitors	4700pF ceramic capacitors
D1	1, 2, 3, 4	Schottky diode Central CMSSH-3	Schottky diode Central CMSSH-3
D2–D5	4	Schottky diodes Central CMHSH5-2L	Schottky diodes Central CMHSH5-2L
L1	1, 2, 3, 4	0.22µH, 1.7mΩ inductor Sumida CDEP1040R2NC-50	0.45µH inductor Sumida CDEP1040R4MC-50
N1	1, 2, 3, 4	N-channel MOSFET International Rectifier IRLR7821	N-channel MOSFET International Rectifier IRLR7821
N2	1, 2, 3, 4	N-channel MOSFET International Rectifier IRLR7833	N-channel MOSFET International Rectifier IRLR7833
R1	1, 3	Sets output voltage	Sets output voltage
R2	1, 3	10kΩ ±1% resistor	10kΩ ±1% resistor
R3	1, 2, 3, 4	(Table 4)	(Table 5)
R4	1, 2	390kΩ ±5% resistor	390kΩ ±5% resistor
R5	1, 2, 3, 4	10Ω ±5% resistor	10Ω ±5% resistor
R6	3, 4	1.5mΩ ±5%, 1W resistor Panasonic ERJM1WTJ1M5U	1.5mΩ ±5%, 1W resistor Panasonic ERJM1WTJ1M5U
R7, R8	1, 2, 3, 4	1Ω ±5% resistors	1Ω ±5% resistors

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

Table 4. R1, R3, and C9 Component Values for 1MHz Operation

V_{IN}	V_{OUT} = 3.3V			V_{OUT} = 2.5V			V_{OUT} = 1.8V			V_{OUT} = 1.5V		
	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (Ω)	R3 (kΩ)	C9 (µF)
5V	3.12	1.2	0.0068	2.13	9.1	0.01	1.24	6.8	0.01	876	5.5	0.01
3.3V	—	—	—	—	—	—	1.24	2.7	0.01	876	2.4	0.01
2.5V	—	—	—	—	—	—	1.24	3.9	0.01	876	3.3	0.01

Table 5. R1, R3, and C9 Component Values for 500kHz Operation

V_{IN}	V_{OUT} = 3.3V			V_{OUT} = 2.5V			V_{OUT} = 1.8V			V_{OUT} = 1.5V		
	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (kΩ)	R3 (kΩ)	C9 (µF)	R1 (Ω)	R3 (kΩ)	C9 (µF)
5V	3.12	36	0.0033	2.13	27	0.0047	1.24	20	0.0068	876	16	0.0068
3.3V	—	—	—	2.13	47	0.0033	1.24	30	0.0047	876	27	0.0047
2.5V	—	—	—	—	—	—	1.24	39	0.0033	876	33	0.0033

Table 6. Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor	631-435-1110	www.centralsemi.com
International Rectifier	310-322-3331	www.irf.com
Kamaya	260-489-1533	www.kamaya.com
Murata	814-237-1431	www.murata.com
Panasonic	714-373-7939	www.panasonic.com
Sanyo	619-661-6835	www.sanyo.com
Sumida	847-956-0666	www.sumida.com
Taiyo Yuden	408-573-4150	www.t-yuden.com

Selector Guide

PART	VOLTAGE MARGINING	CURRENT LIMIT	OUTPUT VOLTAGE
MAX1960	±4%	FET V_{DS} Sensing	Adjustable
MAX1961			4 Presets
MAX1962	No	±10% with R_{SENSE}	4 Presets or Adjustable

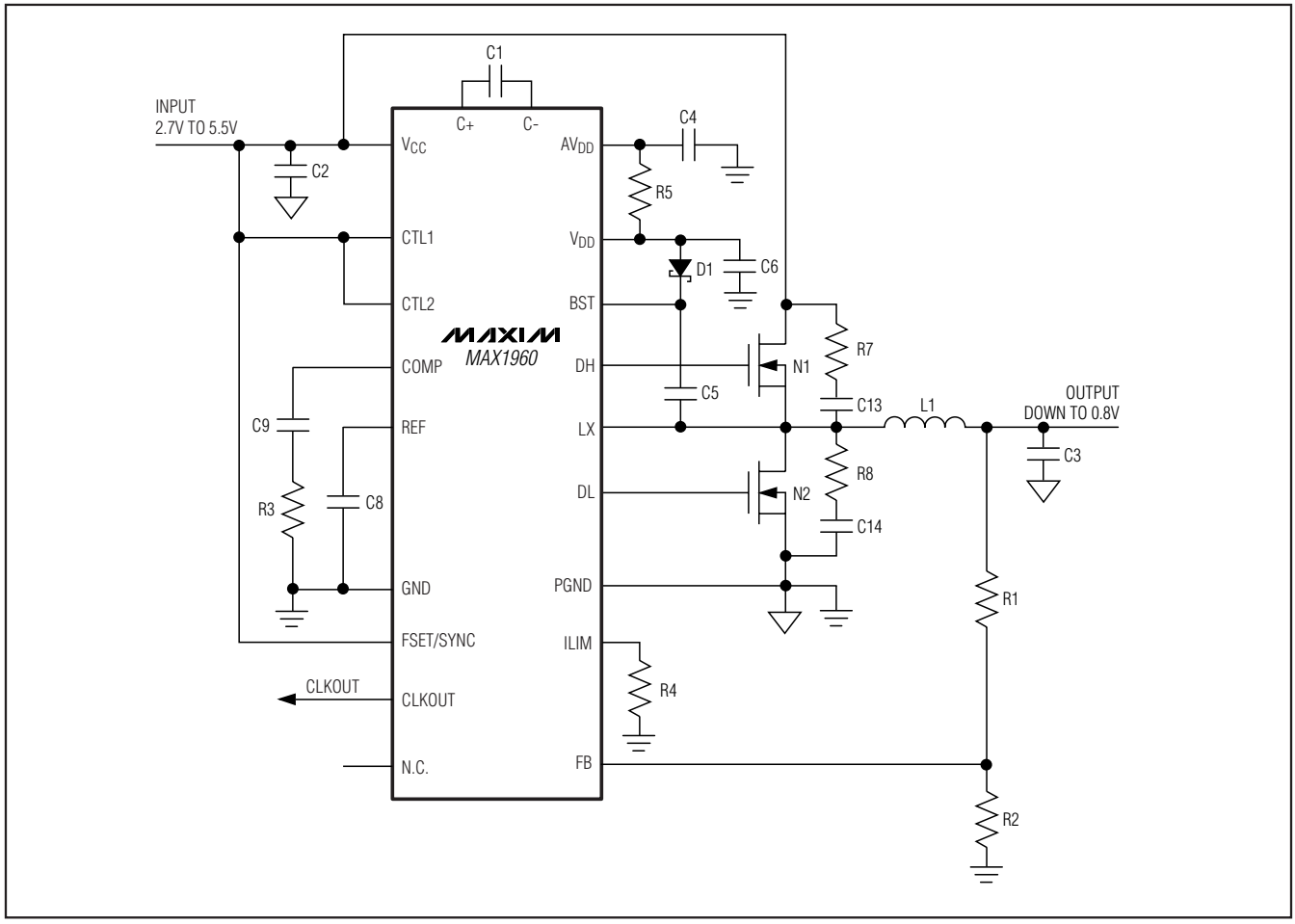


Figure 9. Application Circuit 1—MAX1960 Adjustable Output Voltage

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

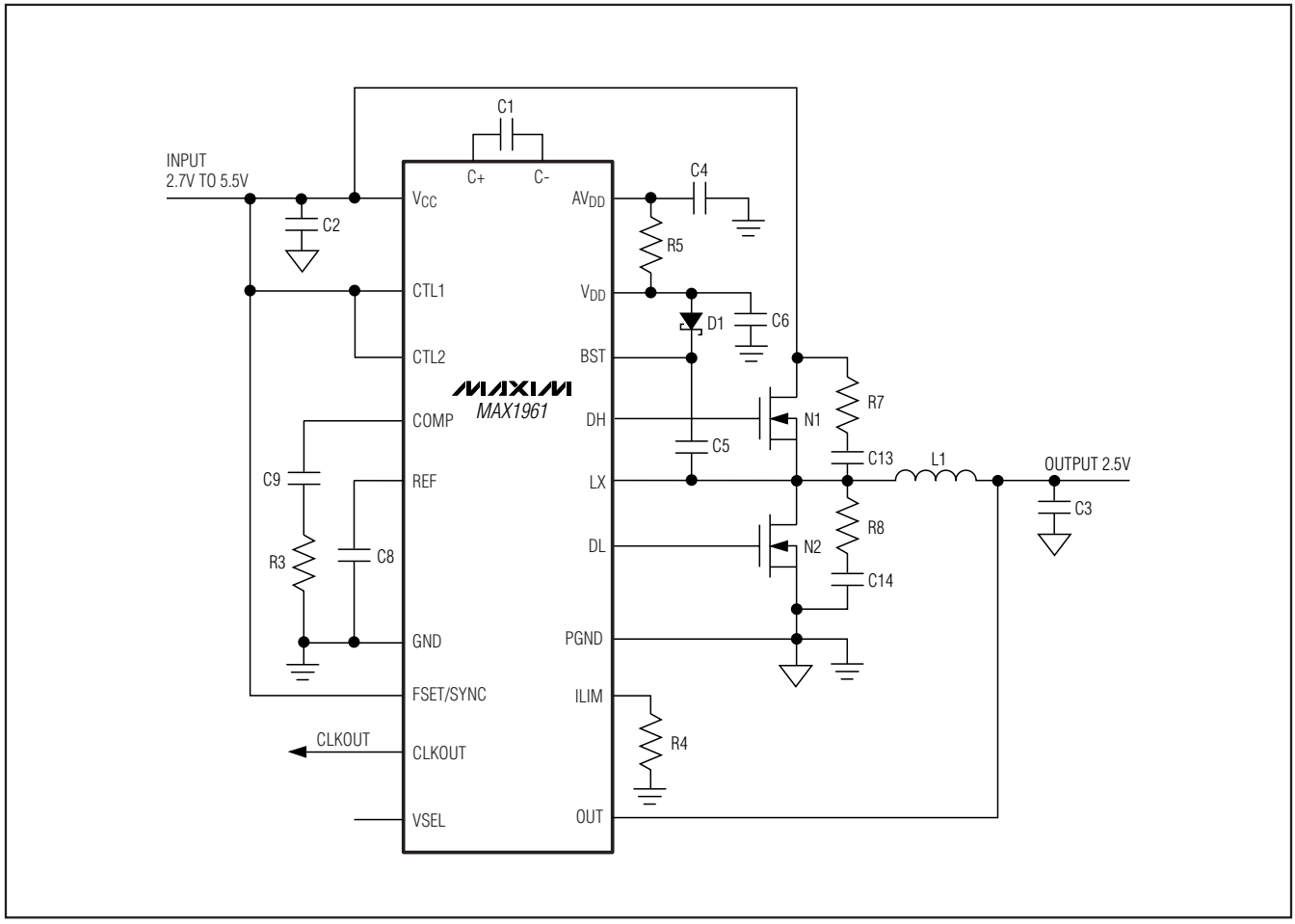


Figure 10. Application Circuit 2—MAX1961 Preset Output Voltage

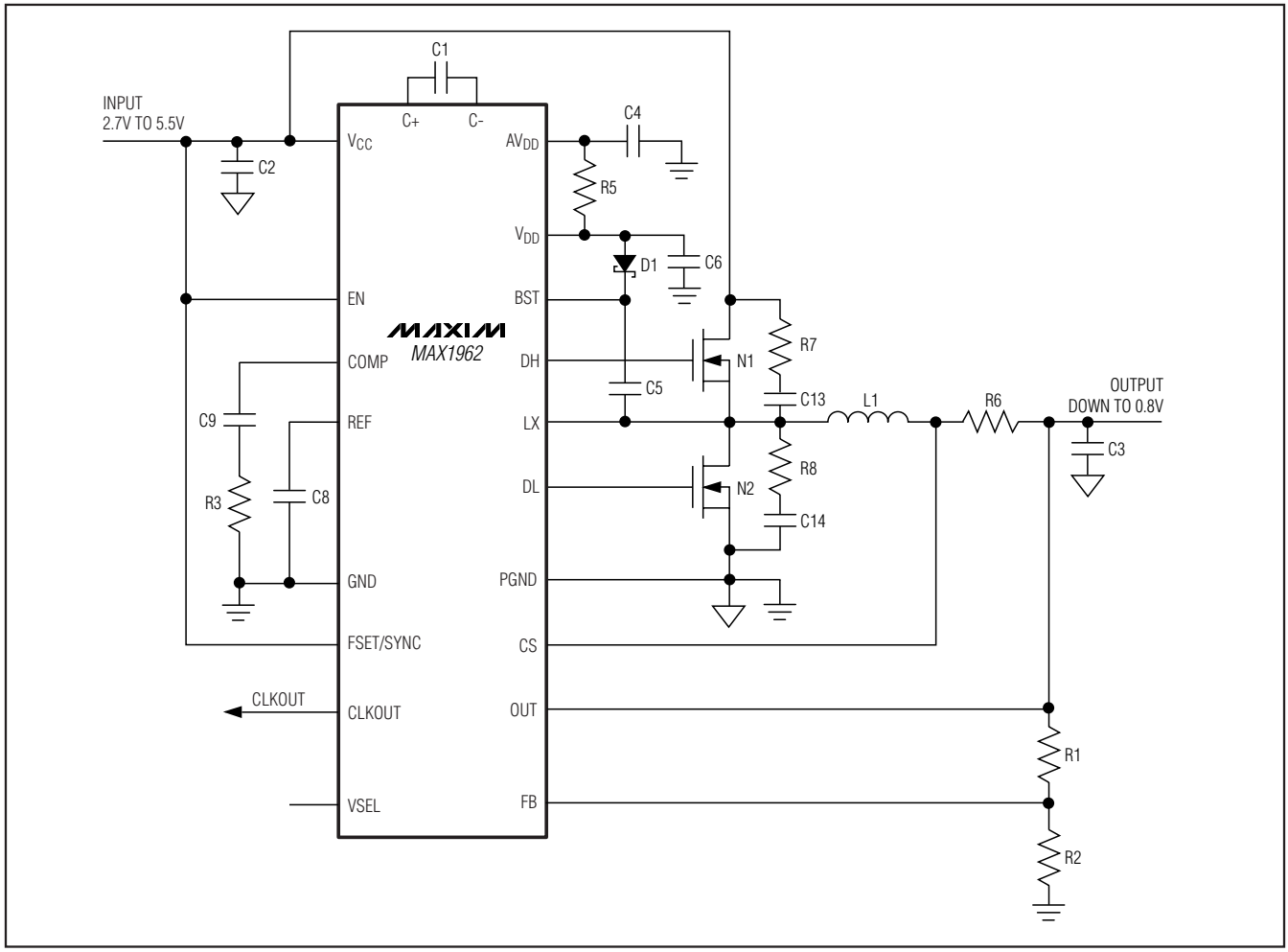


Figure 11. Application Circuit 3—MAX1962 Adjustable Output Voltage

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

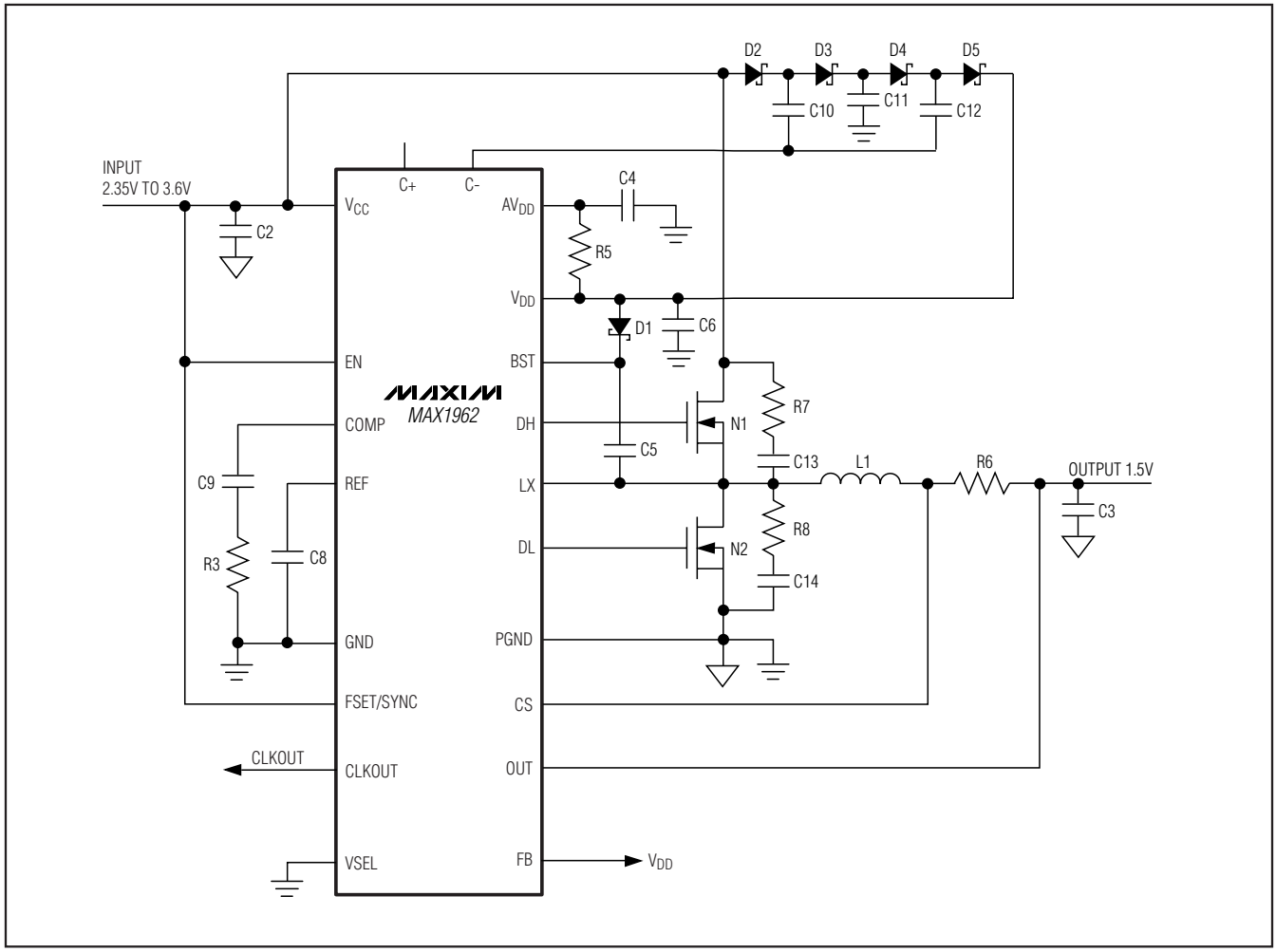


Figure 12. Application Circuit 4—MAX1962 Tripler Configuration, Preset Output

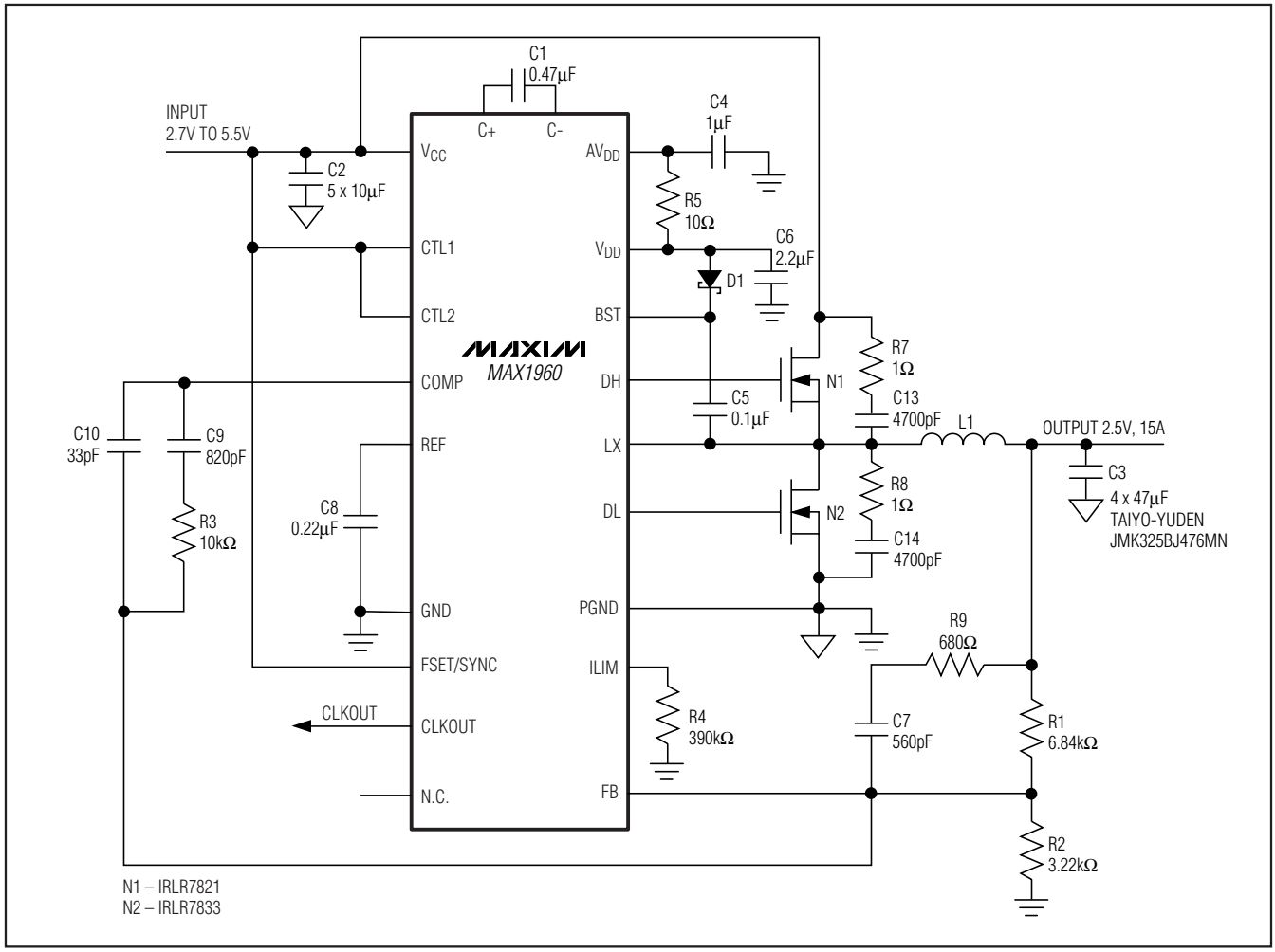
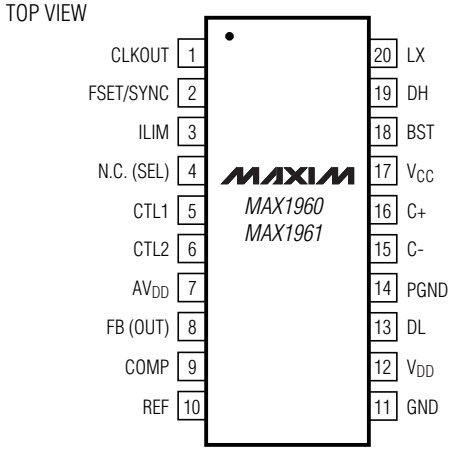


Figure 13. Application Circuit—Ceramic Output Capacitors with Type 3 Compensation

2.35V to 5.5V, 0.5% Accurate, 1MHz PWM Step-Down Controllers with Voltage Margining

Pin Configurations

TOP VIEW



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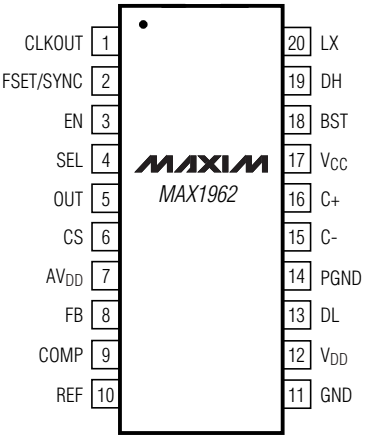
TOP VIEW



QSOP

Chip Information

TRANSISTOR COUNT: 4476

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 QSOP	E20-1	21-0055

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/03	Initial release	—
1	6/09	Updated *Electrical Characteristics* and *Compensation with Ceramic Output Capacitors* sections.	4, 16