Datasheet Brief

MCDP28x0
DisplayPort1.2a to HDMI2.0b
Level Shifter/Protocol Converter
[LSPCON]

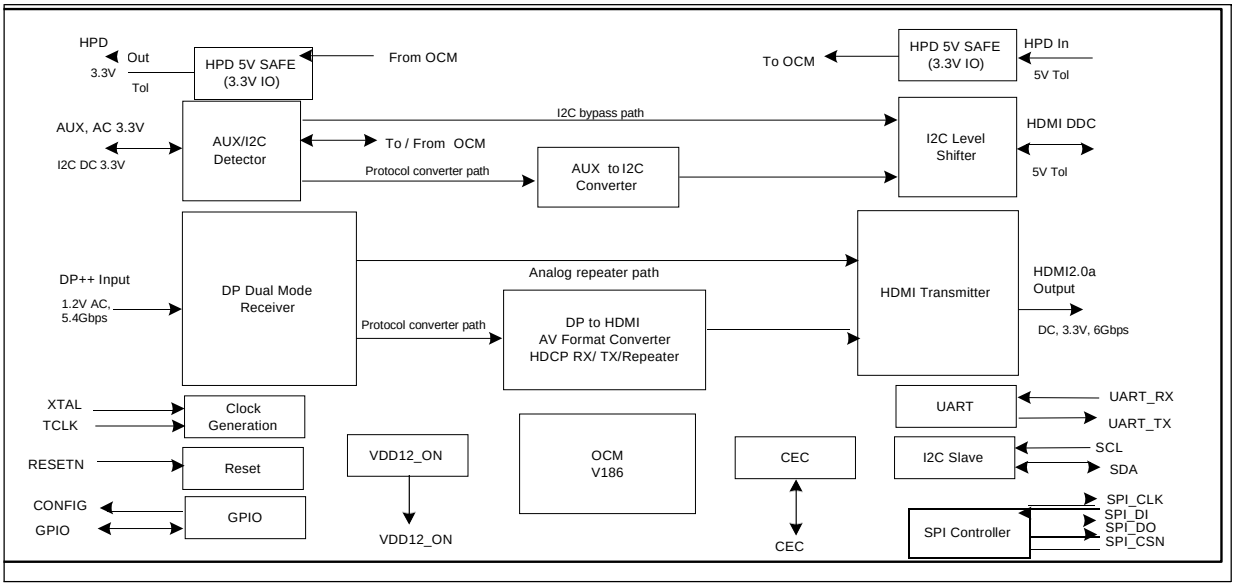
Features

- DisplayPort™ (DP1.2a) receiver
  - Link rate HBR2/HBR/RBR
  - 1, 2, or 4 lanes configuration
  - AUX CH 1 Mbps, HPD out
  - Supports eDP ASSR scrambler operation
- HDMI2.0b transmitter
  - Max data rate up to 6.0 Gbps/ch
  - Deep color up to 16 bits per color
  - 3D video timings, CEC, HPD in
  - Supports High Dynamic Range (HDR)
  - Supports scrambling for the higher data rate
- Level shifter operation (up to 3.4Gbps/ch)
  - AC-coupled HDMI1.4b to DC-coupled HDMI1.4b
  - PHY analog repeater (re-driver or re-timer)
  - 3.3 V DDC/AUX CH signaling support with auto detect
  - 3.3 V DDC to 5V DDC buffering
  - I2C-over-AUX to 5V DDC translation
  - DP HPD_OUT matched to HDMI HPD_IN
- Protocol converter operation (up to 6.0 Gbps/ch)
  - DP SST-to-HDMI format conversion
  - Video and audio forwarding
  - Pixel encoding format conversion from YCbCr444 to YCbCr420
  - Horizontal expansion of VESA CVT to CEA-861 timings
  - Meta data handing
- Level shifter – Protocol converter mode switching
  - Via sideband communication (AUX CH/ DDC)
- Max video resolution and color depth
  - 4Kp60Hz, RGB/YCbCr444, 8bpc
  - 4Kp60Hz, YCbCr420, up to 16bpc
  - 4Kp30Hz, RGB/YCbCr444, up to 16bpc
- YCbCr420 support
  - YCbCr444-to-420 conversion, up to 16 bpc
  - YCbCr420 pass through, up to 16 bpc
- Stereoscopic 3D forwarding
  - Conversion from frame sequential over DP to stacked top-bottom 3D over HDMI
  - All other 3D formats forwarded as is
- Audio forwarding
  - 2-ch, 768 kHz 24bps HBR audio
  - Up to 8-ch, 192 kHz, 24bps LPCM audio, AC3, DTS
- Secure communication
  - Intel secure communication protocol compliant with LSPCON spec
- HDCP content protection
  - Embedded HDCP keys
  - HDCP2.2 transmitter
  - HDCP1.x repeater
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 channel status overwrite
  - CEA861F INFOFRAME generation
  - CEA861-3 HDR and Mastering InfoFrame
- SCDC read request handling
  - Polling enabled for HDMI sinks not supporting read request
- AUX to I2C bridge for EDID/MCCS pass through
- CEC tunneling over AUX CH
- Device configuration options
  - SPI flash for firmware binary image storage required
  - AUX CH, I2C host interface (optional)
- EMI reduction support
  - Spread spectrum for DP input
  - Scrambler for DP input and HDMI2.0b output
- Low power operation
  - 412 mW in protocol converter mode
  - 100 mW in Level shifter mode
  - 0.1 mW in connected standby mode
- ESD specification
  - 6.5 kV HBM, 500 V CDM
- Package
  - 64 LFBGA (7 x 7 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- PC notebook/ tablet motherboard
- DP/USB Type-C docking station, dongle

Figure 1. MCDP28x0 internal block diagram



1. Description

The MCDP28x0 is a power-optimized DisplayPort1.2a-to-HDMI2.0b converter device targeted for desktop/mobile PC motherboard-down applications and for DP or USB type-C adaptor (dongle, docking station) applications. This device functions as a level shifter as well as an active protocol converter.

In level shifter mode, the device functions as a PHY repeater with optional jitter removal capability. This operating mode provides a low-power means of using an AC-coupled TMDS signal from a dual mode DP (DP++) source to be repeated to the HDMI output. The maximum TMDS character clock frequency in this mode is limited to 340 Mchar/s (per HDMI1.4b specification).

In Protocol Converter (PCON) mode, MCDP28x0 functions as a DP branch device receiving AC coupled DisplayPort stream and converting it to HDMI output. The maximum TMDS character clock frequency supported in this mode is up to 600 Mchar/s (as per the HDMI2.0b specification).

The MCDP28x0 operates with two power supply voltages: 1.2 V and 3.3 V. It consumes:

- 100 mW in PHY analog repeater mode
- 412 mW in protocol converter mode
- 0.1 mW in connected standby mode (1.2 V power rail disabled)

The MCDP28x0 has a DisplayPort1.2a dual-mode receiver and HDMI2.0b transmitter. The upstream main link can receive DP input at HBR2 rate over 4 lanes and AC-coupled TMDS signal up to 340Mchar/s. It supports DP SST stream on its main link and Manchester-coded AUX signaling or native 3.3 I2C signaling as the side band channel with the DP++ source. The downstream HDMI TX port is HDMI2.0b specification compliant.

The MCDP28x0 is capable of supporting Ultra High-Definition video formats, resolutions as high as 4096 x 2160@60 Hz. It supports RGB/YCbCr video color formats with a color depth of 16 bpc (or 48 bits per pixel) as long as it fits within the DP1.2a and HDMI2.0b link rate. In addition, this device also supports pixel encoding conversion from YCbCr444 to YCbCr420 and YcbCr420 pass-through from a DP input to an HDMI output. High Dynamic Range (HDR) with deep color up to 12bpc at 4Kp60Hz is supported through the conversion of YCbCr444 CVT timing over DP link with horizontal expansion to YCbCr420 CEA timing on the HDMI TX output.

This device offers secure reception and transmission of high bandwidth digital audio and video content with HDCP 1.x content protection for the upstream DP interface and HDCP2.2 for the downstream HDMI interface. It also operates as an HDCP1.x repeater between the source and the sink. In addition, it conforms to the secure communication protocol specified in the Intel “LSPCON Security Requirements

Architecture Specification" document. The MCDP28x0 comes with embedded HDCP keys that are stored in encrypted form.

The MCDP28x0 uses an external crystal of 27 MHz as a reference clock for its operation and it has a reset input which provides the chip reset during system power up. The device has an on-chip microcontroller with SPI, UART, and I2C interfaces for system level communication and debug. It requires an external SPI flash memory for storing device configuration firmware. The firmware update is done through the DP AUX channel or through UART interface. An 8 Mbit SPI flash memory is recommended for storing the firmware with a backup option as fail-safe during in-system-programming.

2. Application overview

Two important target applications of MCDP28x0 are:

- Mobile PC motherboard application. This is referred as motherboard-down topology and the part number that supports this topology is MCDP2800.
- Accessory application (dongle, docking station etc.). This is referred as adaptor topology and the part number for this topology is MCDP2850.

3. Ordering information

Table 1. Ordering Information

Part Number	Operating Temperature	Package
MCDP2800-BC	0°C to +70°C	64 LFBGA (7 x 7 x 1.4 mm) for motherboard-down application. Mass production parts. Delivered in trays. (Rev BC silicon)
MCDP2800-BCT	0°C to +70°C	64 LFBGA (7 x 7 x 1.4 mm) for motherboard-down application. Mass production parts. Delivered in tape and reel. (Rev BC silicon)
MCDP2850-BC	0°C to +70°C	64 LFBGA (7 x 7 x 1.4 mm) for dongle application. Delivered in trays. (Rev BC silicon)