

## MM54HC03/MM74HC03 Quad 2-Input Open Drain NAND Gate

### General Description

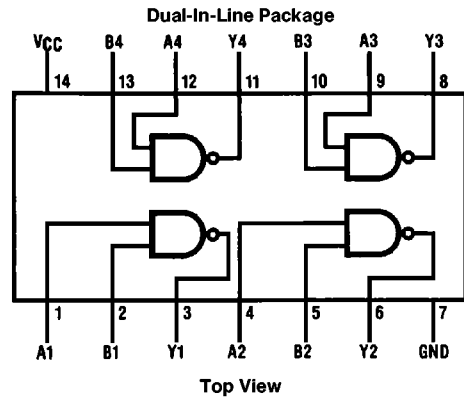
These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

As with standard 54HC/74HC push-pull outputs there are diodes to both  $V_{CC}$  and ground. Therefore the output should not be pulled above  $V_{CC}$  as it would be clamped to one diode voltage above  $V_{CC}$ . This diode is added to enhance electrostatic protection.

### Features

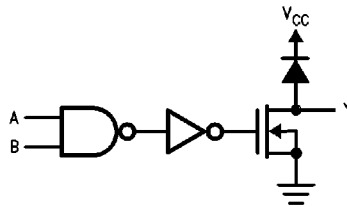
- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20  $\mu$ A maximum (74HC Series)
- Low input current: 1  $\mu$ A maximum
- Fanout of 10 LS-TTL loads

### Connection and Logic Diagrams



TL/F/5295-1

Order Number MM54HC03 or MM74HC03



TL/F/5295-2

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$		Units	
				Typ	Guaranteed Limits						
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5		V		
			4.5V		3.15	3.15	3.15		V		
			6.0V		4.2	4.2	4.2		V		
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5		V		
			4.5V		1.35	1.35	1.35		V		
			6.0V		1.8	1.8	1.8		V		
$V_{OL}$	Minimum Low Level Output Voltage	$V_{IN} = V_{IH}$ $ I_{OUT}  \leq 20 \mu A$ $R_L = \infty$	2.0V	0	0.1	0.1	0.1		V		
			4.5V	0	0.1	0.1	0.1		V		
			6.0V	0	0.1	0.1	0.1		V		
		$V_{IN} = V_{IH}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4		V		
			6.0V	0.2	0.26	0.33	0.4		V		
$I_{LKG}$	Maximum High Level Output Leakage Current	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$	6.0V		0.5	5	10		$\mu A$		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$		$\mu A$		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		2.0	20	40		$\mu A$		

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

**AC Electrical Characteristics**  $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{pZL}, t_{pLZ}$	Maximum Propagation Delay	$R_L = 1\text{ K}\Omega$	10	20	ns

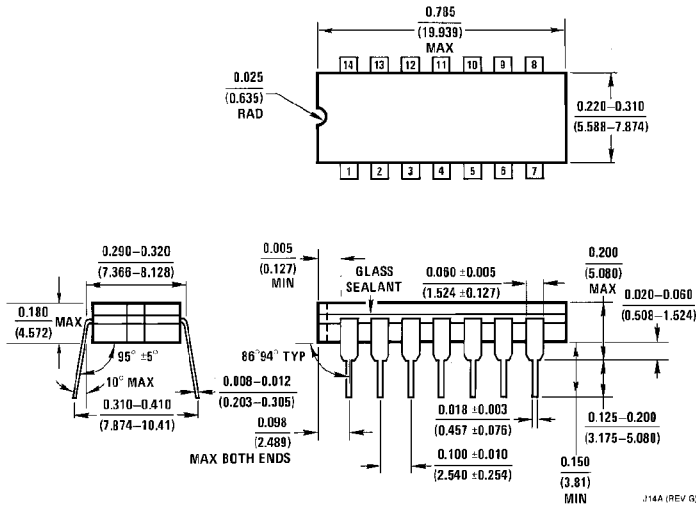
**AC Electrical Characteristics**

$V_{CC}=2.0V\text{ to }6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$  (unless otherwise specified)

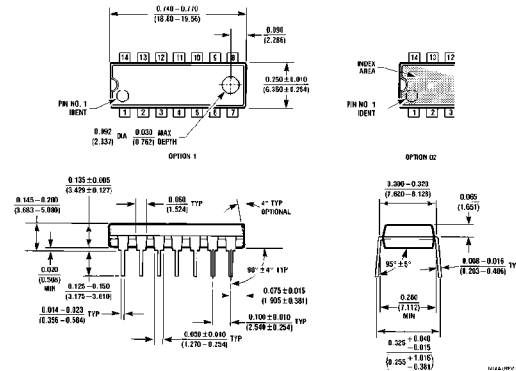
Symbol	Parameter	Conditions	$V_{CC}$	$T_A=25^{\circ}C$		74HC	54HC	Units
						$T_A=-40\text{ to }85^{\circ}C$	$T_A=-55\text{ to }125^{\circ}C$	
				Typ	Guaranteed Limits			
$t_{pLZ}, t_{pZL}$	Maximum Propagation Delay	$R_L = 1\text{ K}\Omega$	2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
$t_{THL}$	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ . The power dissipated by  $R_L$  is not included.

**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54HC03J or MM74HC03J**  
**NS Package Number J14A**



**Molded Dual-In-Line Package (N)**  
**Order Number MM74HC03N**  
**NS Package Number N14A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: onjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
 Tel: 81-043-299-2309  
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.