HDMI Switch ICs

BU16006KV, BU16018KV, BU16024KV, BU16027KV

No.10063EET01

●Description

These devices control are simple. It requires only 3.3V source and a few GPIO controls.
Termination resistors (50Ω) are integrated at all TMDS input port. When channel is not selected, TMDS input termination resistors are turned off and TMDS inputs are high impedance. These devices are also integrated equalizer circuit to adapt long cable and DDC active buffer function to isolate capacitance.

●Features

1) Supports 2.25 Gbps signaling rate for 480i/p, 720p, and 1080i/p resolution to 12-bit color depth
2) Compatible with HDMI 1.3a
3) 5V tolerance to all DDC and HPD_SINK inputs
4) Integrated active DDC buffer
5) Integrated switchable 50Ω termination resistors
6) Integrated equalizer circuit to adapt long cable
7) HBM ESD protection exceeds 10kV
8) 3.3V fixed supply
9) RoHS compatible

●Applications

Digital TV, Audio Video Receiver, Digital Projector, DVI or HDMI Switch Box

●Line up matrix

Part No.	Power Supply (V)	ESD (KV)	Input and Output	Data rate (Gbps)	Hot Plug Control	Termination Resistor switch Control	Switching Method	DDC Buffer type	Equalizer	High speed mode	Package	RoHS
BU16018KV	3 to 3.6	10	3 input 1 output	2.25	Yes	Sync HPD	GPIO	Active	Fixed	Yes	VQFP80	Yes
BU16027KV	3 to 3.6	10	3 input 1 output	2.25	Yes	Sync S1/S2	GPIO	Active	Fixed	Yes (Always ON)	VQFP64	Yes
BU16006KV	3 to 3.6	10	2 input 1 output	2.25	Yes	Sync HPD	GPIO	Active	Fixed	Yes (Always ON)	VQFP64	Yes
BU16024KV	3 to 3.6	10	1 input 1 output	2.25	Yes	Sync HPD	-	Active	Fixed	Yes	VQFP48C	Yes

●Other Line up

HDMI Switch adapted “Repeater” and “Source” Equipment

Part No.	Power Supply (V)	ESD (KV)	Input and Output	Data rate (Gbps)	Hot Plug Control	Termination Resistor switch Control	Switching Method	DDC Buffer type	Equalizer	High speed mode	Package	RoHS
BU16025MUV	3 to 3.6	10	1 input 1 output	2.70	Yes	Sync OE	-	Active	Selectable	Yes	VQFN48AV7070	Yes

●Absolute Maximum Rating

Over operating free-air temperature range (unless otherwise noted)

Item	Limits				Unit
	BU16006KV	BU16018KV	BU16024KV	BU16027KV	
Power supply voltage(Vcc)	-0.3～+4.5	-0.3～+4.5	-0.3～+4.5	-0.3～+4.5	V
DDC, HPD_SINK input voltage	-0.3～+5.6	-0.3～+5.6	-0.3～+5.6	-0.3～+5.6	V
Differential input voltage	+2.5～+4.0	+2.5～+4.0	+2.5～+4.0	+2.5～+4.0	V
Control pin input voltage	-0.3～+4.0	-0.3～+4.0	-0.3～+4.0	-0.3～+4.0	V
Power dissipation	1000(*1)	1200(*2)	950(*3)	1000(*1)	mW
Strage temperture range	-55～+125	-55～+125	-55～+125	-55～+125	℃

(*1-3) 70mm×70mm×1.6mm glass epoxy board mount.（Reverse Cu occupation rate：15mm×15mm）

(*1) When it's used by than Ta=25℃, it's reduced by 10.0mW/℃.

(*2) When it's used by than Ta=25℃, it's reduced by 12.5mW/℃.

(*3) When it's used by than Ta=25℃, it's reduced by 9.5mW/℃.

●Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Free-air temperature	0	-	70	℃
TMDS Differential Pins					
V_{IC}	Input common mode voltage, see Figure 2.	V_{CC}–0.6	-	V_{CC}+0.01	V
$V_{ID(pp)}$	Receiver peak-to-peak differential input voltage, see Figure 2.	150	-	1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	4.60	4.64	4.68	k Ω
AV_{CC}	TMDS Output termination voltage, see Figure 1.	3	3.3	3.6	V
R_T	Termination resistance, see Figure 1.	45	50	55	Ω
Signaling rate		-	-	2.25	Gbps
Control Pins					
V_{IH}	LVTTL High-level input voltage	2	-	V_{CC}	V
V_{IL}	LVTTL Low-level input voltage	GND	-	0.8	V
HPD_SINK					
V_{IH}	High-level input voltage	2.4	-	5.5	V
V_{IL}	Low-level input voltage	GND	-	0.8	V
RX (SDA[n],SCL[n])					
V_{IH}	High-level input voltage	2.4	-	5.5	V
V_{IL}	Low-level input voltage	GND	-	0.8	V
TX (SCL_SINK, SDA_SINK)					
V_{IH}	High-level input voltage	1.5	-	5.5	V
V_{IL}	Low-level input voltage	GND	-	0.35	V

●Electrical Specifications

Over recommended operating conditions (unless otherwise noted)

Symbol	Parameter		Test Condition	Limit			Unit
				Min.	Typ.(1)	Max.	
Icc	Supply current	BU16006KV, BU16018KV BU16027KV	V_{ID} = 400mV, R_{VSADJ} = 4.64kΩ R_T = 50Ω, AVcc = Vcc, Am/Bm = 2.25 Gbps HDMI data pattern, A1,/B1 = 225 MHz clock See Figure 2	-	120	150	mA
		BU16024KV		-	140	170	mA
P_D	Power Consumption	BU16006KV, BU16018KV BU16027KV	V_{ID} = 400mV, R_{VSADJ} = 4.64kΩ R_T = 50Ω, AVcc = Vcc, Am/Bm = 2.25 Gbps HDMI data pattern, A1,/B1 = 225 MHz clock See Figure 2	-	450	600	mW
		BU16024KV		-	480	700	mW
TMDS Differential Pins (A/B;Y/Z)							
V_{OH}	Single-ended high-level output voltage	BU16006KV, BU16027KV	AVcc = Vcc, R_T = 50Ω	AVcc-200	-	Avcc-50	mV
		BU16018KV, BU16024KV	AVcc = Vcc, PRE = Vcc, R_T = 50Ω	AVcc-200	-	AVcc - 50	mV
		BU16018KV, BU16024KV	AVcc = Vcc, PRE = 0.0V, R_T = 50Ω	AVcc-10	-	AVcc +10	mV
V_{OL}	Single-ended low-level output voltage		AVcc = Vcc, R_T = 50Ω	AVcc-600	-	Avcc-400	mV
V_{SWING}	Single-ended low-level swing voltage	BU16006KV, BU16027KV	AVcc = Vcc, R_T = 50Ω, See Figure 2,	300	-	460	mV
		BU16018KV, BU16024KV	AVcc = Vcc, PRE = Vcc, R_T = 50Ω, See Figure 2,	300	-	460	mV
		BU16018KV, BU16024KV	AVcc = Vcc, PRE = 0.0V, R_T = 50Ω, See Figure 2,	400	-	600	mV
$Vod_{(O)}$	Overshoot of output differential voltage		See Figure 2	-	6%	15%	$2xV_{swing}$
$Vod_{(U)}$	Undershoot of output differential voltage		See Figure 2	-	12%	25%	$2xV_{swing}$
R_{INT}	Input termination resistance		AVcc = Vcc = 3.3V, V_A = V_B = Vcc-400mV, See Figure 2	45	50	55	Ω

Symbol	Parameter		Test Conditions		Limits			Unit
					Min.	Typ.(1)	Max.	
DDC Input and output								
Tx								
I_{IKT1}	Input leak current		VI=5.5V		-10	-	10	µA
I_{IKT2}	Input leak current		VI=Vcc		-10	-	10	µA
I_{OHT}	High-level output current		VO=3.6V		-10	-	10	µA
I_{ILT}	Low-level input current		VI=GND		-10	-	10	µA
V_{OLT}	Low-level output voltage	BU16006KV BU16018KV BU16027KV	RL=4.7kΩ		0.43	0.5	0.57	V
		BU16024KV	RL=4.7kΩ	SELREF = NC	0.43	-	0.57	V
				SELREF = GND	0.58	-	0.72	
				SELREF =Vcc	0.73	-	0.87	
V_{OLT}-V_{IL}	Low-level input voltage below output low-level voltage	BU16006KV BU16018KV BU16027KV	RL=4.7kΩ		20	100	190	mV
		BU16024KV	RL=4.7kΩ	SELREF = NC	-	100	-	mV
				SELREF= GND	-	250	-	
				SELREF = Vcc	-	400	-	
Rx								
I_{IKR1}	Input leak current		VI=5.5V		-10	-	10	µA
I_{IKR2}	Input leak current		VI=Vcc		-10	-	10	µA
I_{OHR}	High-level output current		VO=3.6V		-10	-	10	µA
I_{ILR}	Low-level input current		VIL=GND		-10	-	10	µA
V_{OLR}	Low-level output voltage		Iout = 4mA		-	-	0.2	V
HPD 1, HPD 2, HPD 3								
$V_{OH(TTL)}$	High level output voltage		I_{OH} = -8mA		2.4	-	Vcc	V
$V_{OL(TTL)}$	Low level output voltage		I_{OL} = 8mA		0	-	0.4	V
CONTROL PINS								
I_{IH}	High level input current		V_{IH} = Vcc		-10	-	10	µA
I_{IL}	Low level input current		V_{IL} = GND		-10	-	10	µA
CONTROL PINS (I^2CEN, SELREF,)								
I_{IH}	High level input current		V_{IH} = Vcc		-45	-	45	µA
I_{IL}	Low level input current		V_{IL} = GND		-45	-	45	µA
HPD_SINK								
I_{IH}	High level input current		V_{IH} = 5.5V		10	50	100	µA
			V_{IH} = Vcc		5	30	80	µA
I_{IL}	Low –level input current		V_{IL} = GND		-10	-	10	µA

Symbol	Parameter		Test Condition	Limits			Unit
				Min.	Typ.(1)	Max.	
TMDS Differential Pins (Y/Z)							
t_{PLH}	Propagation delay time low to high level output	BU16006KV, BU16018KV, BU16027KV	AV_{CC} = 3.3V, R_T = 50Ω	-	480	-	ps
		BU16024KV		-	320	-	
t_{PHL}	Propagation delay time low to high level output	BU16006KV, BU16018KV, BU16027KV		-	500	-	ps
		BU16024KV		-	335	-	
t_r	Differential output signal rise time (20%-80%)	BU16006KV, BU16027KV, BU16018KV		-	160	-	ps
		BU16024KV		-	120	-	
t_f	Differential output signal fall time (20%-80%)	BU16006KV, BU16018KV, BU16027KV		-	160	-	ps
		BU16024KV		-	120	-	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	BU16006KV, BU16018KV, BU16027KV		-	20	-	ps
		BU16024KV		-	15	-	
$t_{sk(D)}$	Intra-pair differential skew, see Figure 3.	BU16006KV, BU16018KV, BU16027KV		-	35	-	ps
		BU16024KV		-	25	-	
DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK) See Figure 4							
$t_{pdLHTR(DDC)}$	Propagation delay time, low to high level output Tx to Rx		R_L = 4.7kΩ, C_L = 100pF, see Figure 5	-	650	-	ns
$t_{pdHLTR(DDC)}$	Propagation delay time, high to low level output Tx to Rx			-	200	-	ns
$t_{pdLHRT(DDC)}$	Propagation delay time, low to high level output Rx to Tx		R_L = 1.67kΩ, C_L = 400pF, see Figure 5	-	500	-	ns
$t_{pdHLRT(DDC)}$	Propagation delay time, high to low level output Rx to Tx			-	350	-	ns
tr $Tx_{(DDC)}$	Tx output Rise time		R_L = 4.7kΩ, C_L = 100pF, see Figure 5	-	800	-	ns
tf $Tx_{(DDC)}$	Tx output Fall time			-	150	-	ns
tr $Rx_{(DDC)}$	Rx output Rise time		R_L = 1.67kΩ C_L = 400pF	-	950	-	ns
tf $Rx_{(DDC)}$	Rx output Fall time			-	50	-	ns
t_{sx}	Select to switch output		see Figure 4	-	8	-	ns
t_{dis}	Disable time		see Figure 4	-	5	-	ns
t_{en}	Enable time		see Figure 4	-	7	-	ns
$t_{sx(DDC)}$	Switch time from SCLn to SCL_SINK		C_L=10pF	-	800	-	ns
C_{IO}	Input/output capacitance		V_I=0V	-	15	-	pF
Hot Plug Detect Pins							
$t_{pdLH(HPD)}$	Propagation delay time, low to high level output from HPD_SINK to HPDn(n=1,2,3)		C_L=10pF	-	5	-	ns
$t_{pdHL(HPD)}$	Propagation delay time, high to low level output from HPD_SINK to HPDn(n=1,2,3)		C_L=10pF	-	5	-	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD		C_L=10pF	-	8	-	ns

Note: (1). All typical values are at 25℃ and with a 3.3V supply.

●Measurement Symbol And Circuit

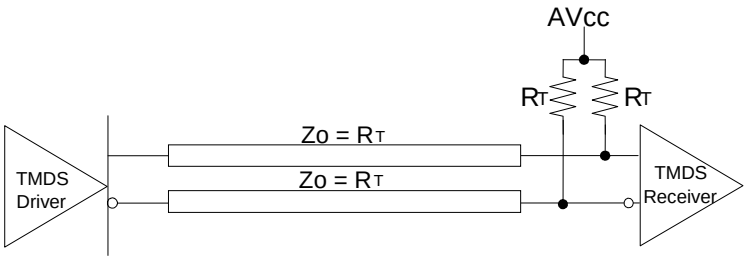


Figure 1 TMDS Output Driver

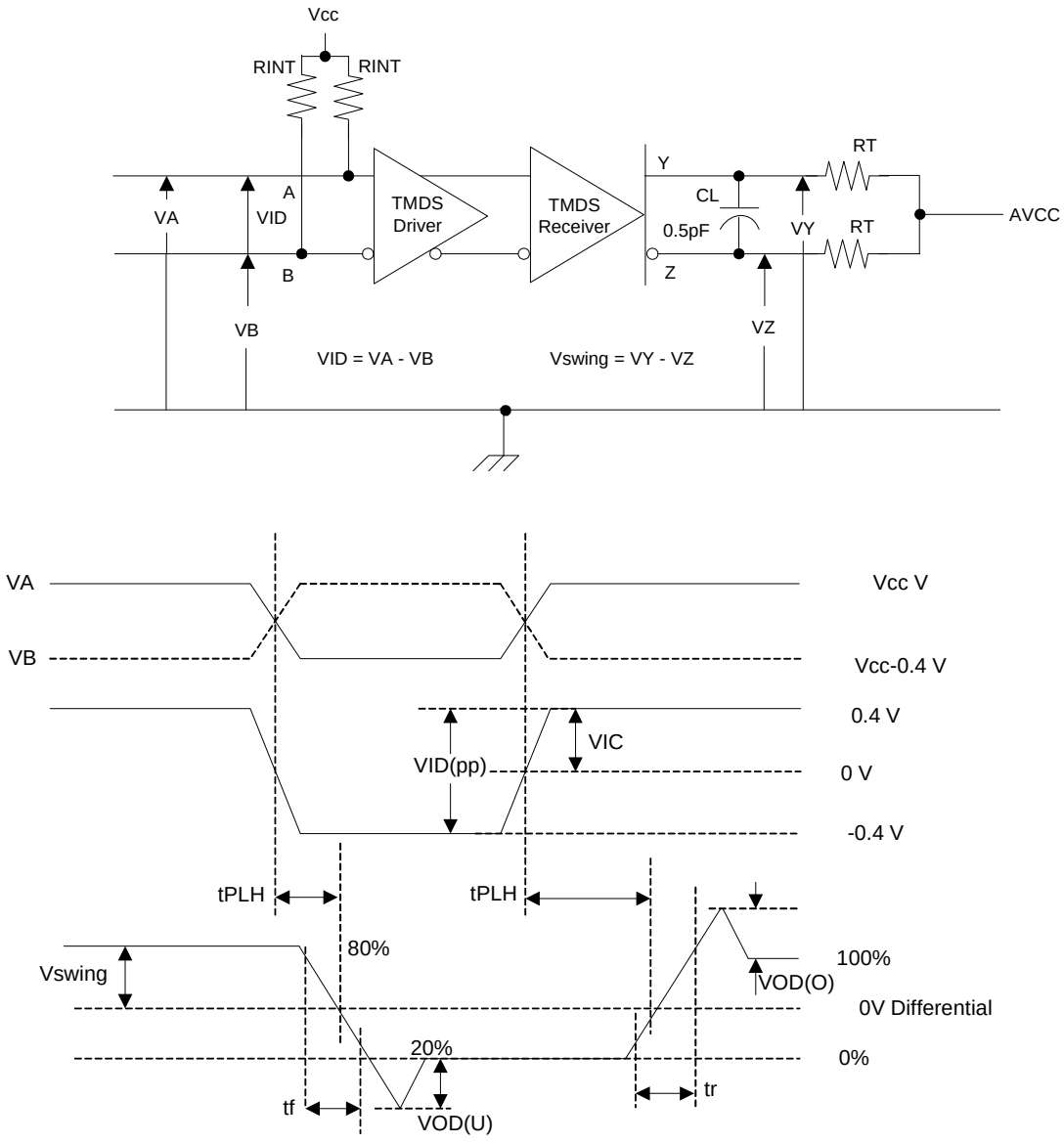


Figure 2 Test Circuit and Definitions

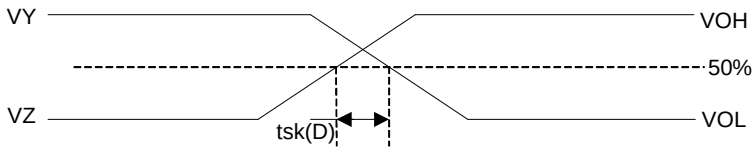


Figure 3 Definition of Intra-Pair Differential Skew

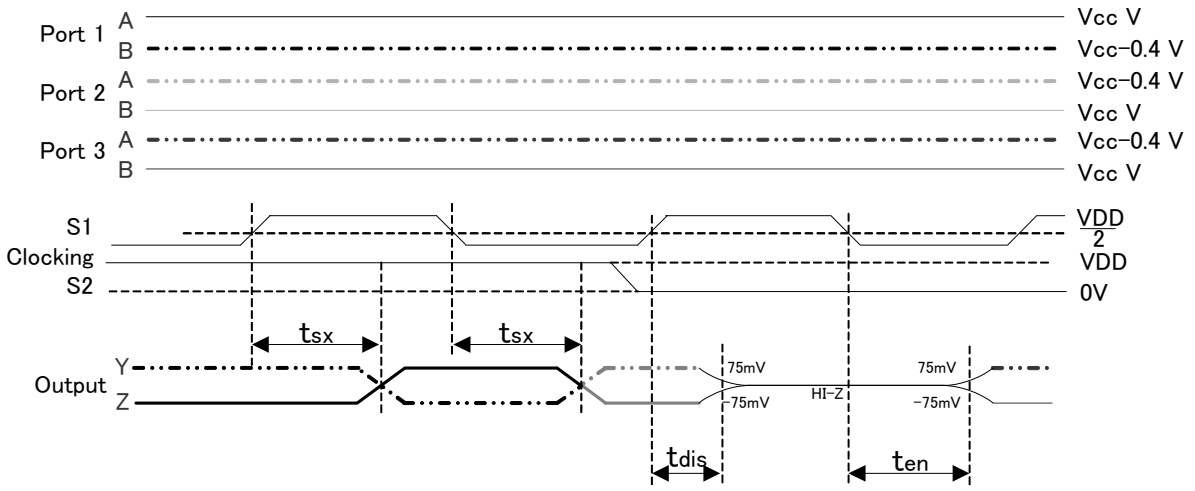


Figure 4 TMDS Outputs Control Timing Definitions

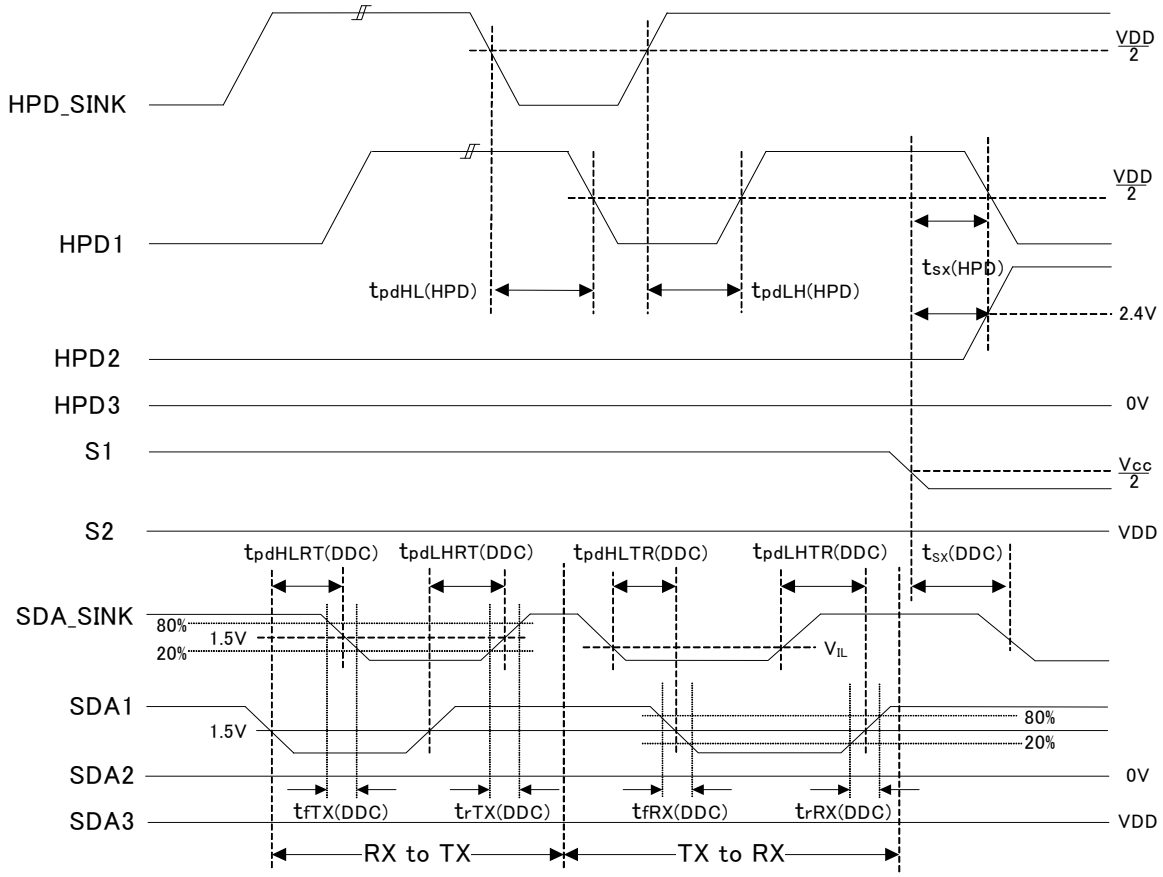


Figure 5 DDC and HPD Timing Definitions

●Reference Data of BU16027KV/BU16006KV

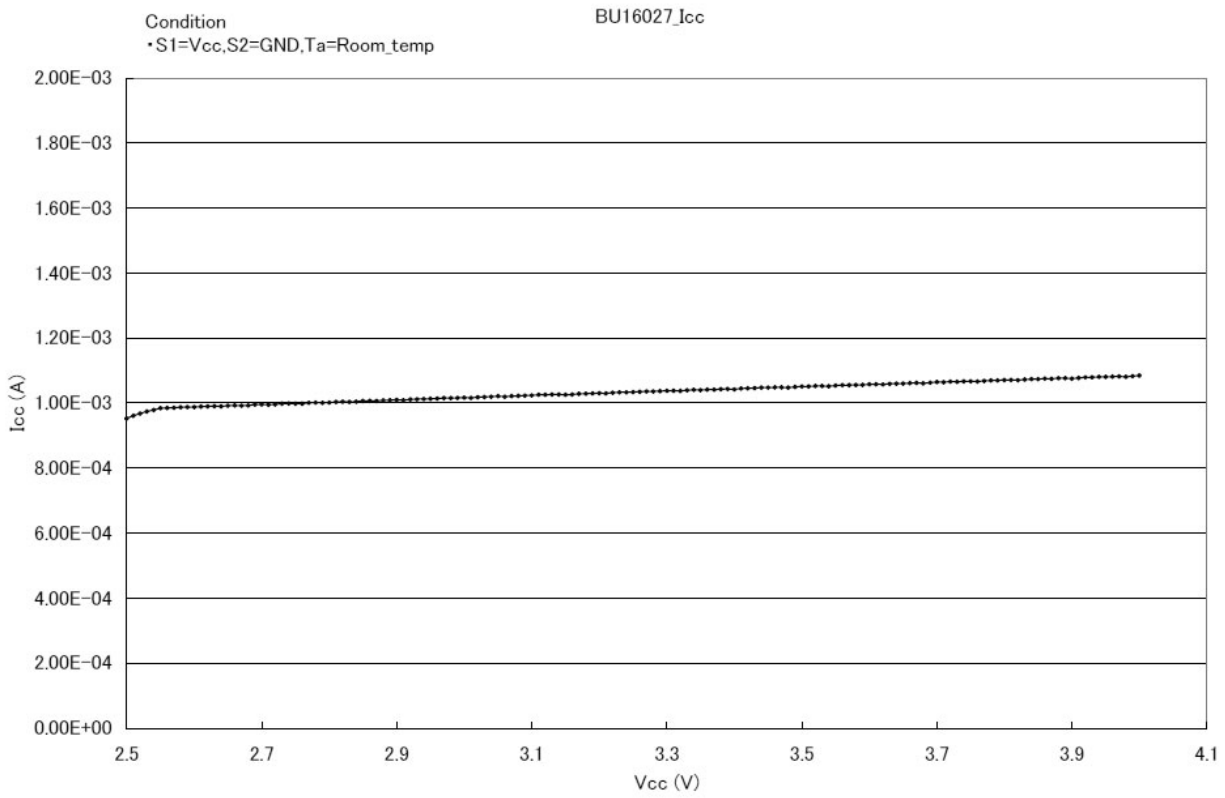
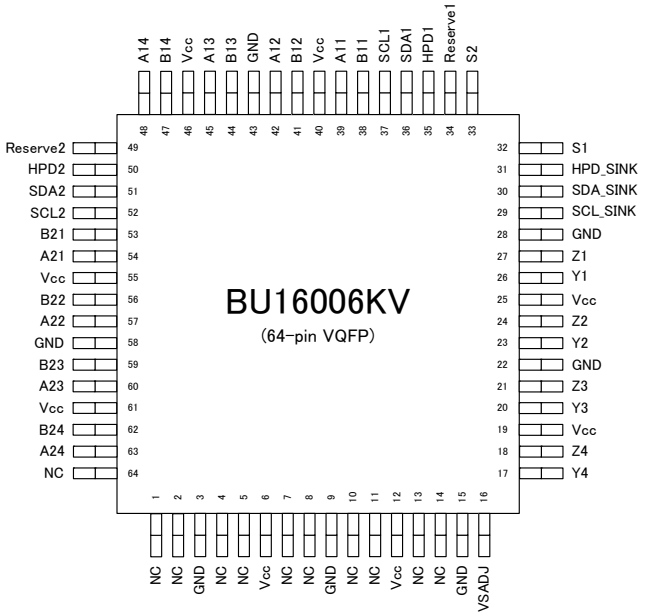
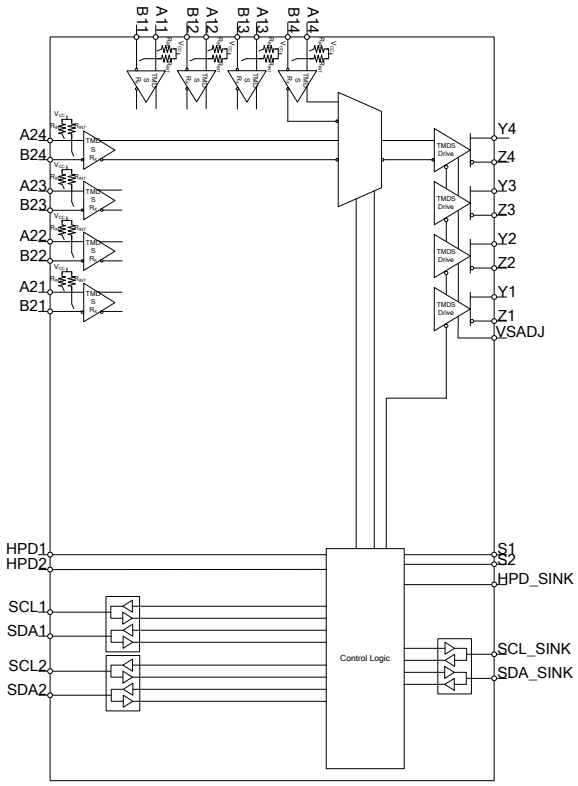


Figure 6 Supply voltage(Vcc) vs. Supply current(Icc) of BU16006KV/BU16027KV [S1=H,S2=L]

●Pin Assignment and Block Diagram of BU16006KV

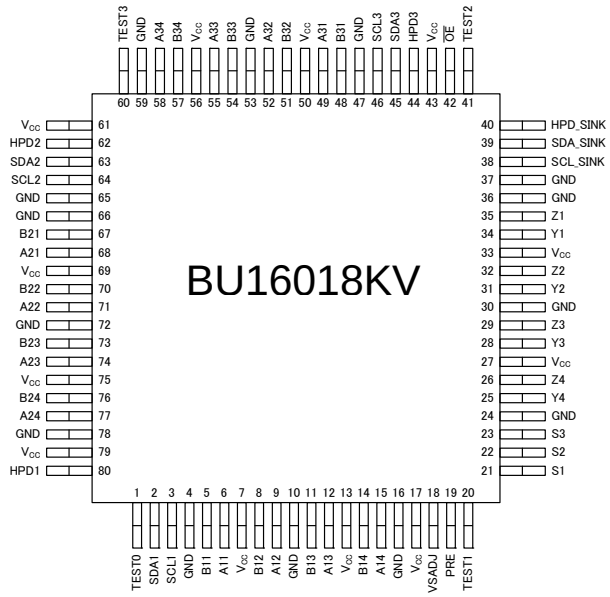


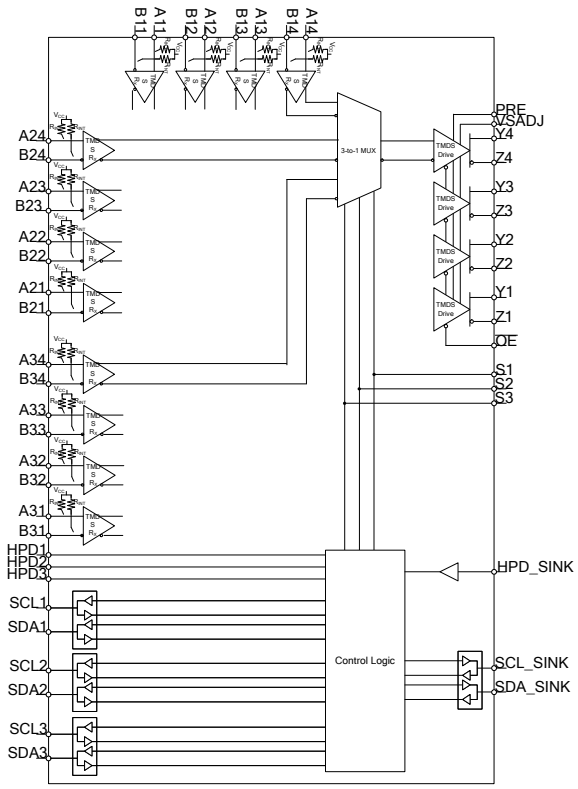


●Pin Explanation List

Terminal		I/O	Description
Name	No.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	-	Ground
HPD1	35	O	Source port 1 hot plug detector output
HPD2	50	O	Source port 2 hot plug detector output
HPD_SINK	31	I	Sink port hot plug detector input
Reserve1	34	I/O	Set to HIGH/LOW/OPEN
Reserve2	49	I/O	Non Connect Pin
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I^2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32, 33	I	Source selector
Vcc	6, 12, 19, 25, 40, 46, 55, 61	-	Power supply
VSADJ	16	I	TMDS compliant voltage swing control (4.64kΩ to GND)
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	TMDS negative outputs

●Pin Assignment and Block Diagram of BU16018KV

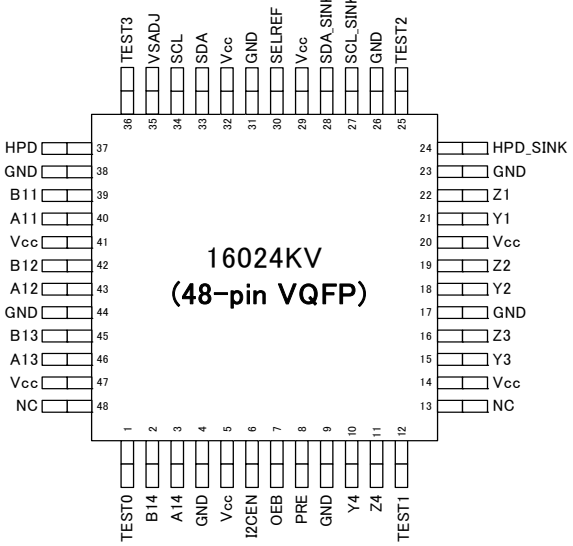


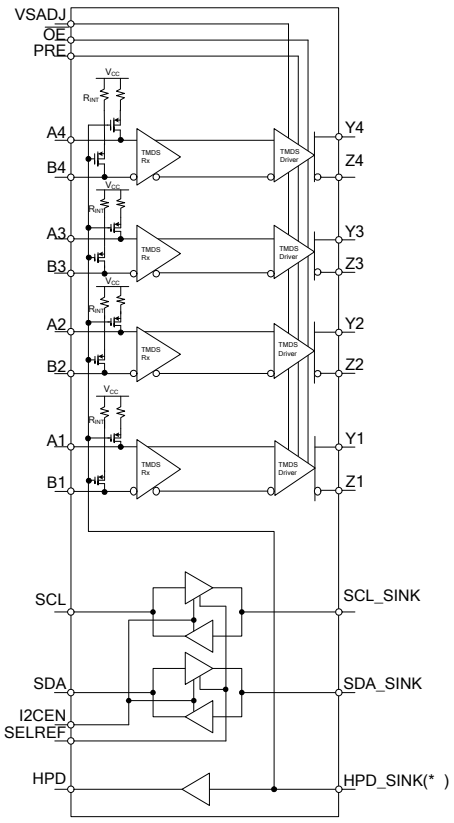


●Pin Explanation List

Terminal		I/O	Description
Name	**No.**		
A11, A12, A13, A14	6, 9, 12, 15	I	Port 1 TMDS positive inputs
A21, A22, A23, A24	68, 71, 74, 77	I	Port 2 TMDS positive inputs
A31, A32, A33, A34	49, 52, 55, 58	I	Port 3 TMDS positive inputs
B11, B12, B13, B14	5, 8, 11, 14	I	Port 1 TMDS negative inputs
B21, B22, B23, B24	67, 70, 73, 76	I	Port 2 TMDS negative inputs
B31, B32, B33, B34	48, 51, 54, 57	I	Port 3 TMDS negative inputs
GND	4, 10, 16, 24, 30, 36, 37, 47, 53, 59, 65, 66, 72, 78	-	Ground
HPD1	80	O	Port 1 hot plug detector output
HPD2	62	O	Port 2 hot plug detector output
HPD3	44	O	Port 3 hot plug detector output
HPD_SINK	40	I	Sink side hot plug detector input
TEST0,1,2,3	1, 20, 41, 60		Open or GND connect (recommend)
$\overline{OE}$	42	I	Output enable, active low
PRE	19	I	TMDS high speed mode SW High : ON, Low : OFF (above 165MHz recommend to High)
SCL1	3	I/O	Source port 1 DDC I^2C clock line
SCL2	64	I/O	Source port 2 DDC I^2C clock line
SCL3	46	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	38	I/O	Sink port DDC I^2C clock line
SDA1	2	I/O	Source port 1 DDC I^2C data line
SDA2	63	I/O	Source port 2 DDC I^2C data line
SDA3	45	I/O	Source port 3 DDC I^2C data line
SDA_SINK	39	I/O	Sink port DDC I^2C data line
S1, S2, S3	21, 22, 23	I	Source selector input
V_{CC}	7, 13, 17, 27, 33, 43, 50, 56, 61, 69, 75, 79	-	Power supply
VSADJ	18	I	TMDS voltage swing control. Connect to GND 4.64KΩ
Y1, Y2, Y3, Y4	34, 31, 28, 25	O	TMDS positive outputs
Z1, Z2, Z3, Z4	35, 32, 29, 26	O	TMDS negative outputs

●Pin Assignment and Block Diagram of BU16024KV



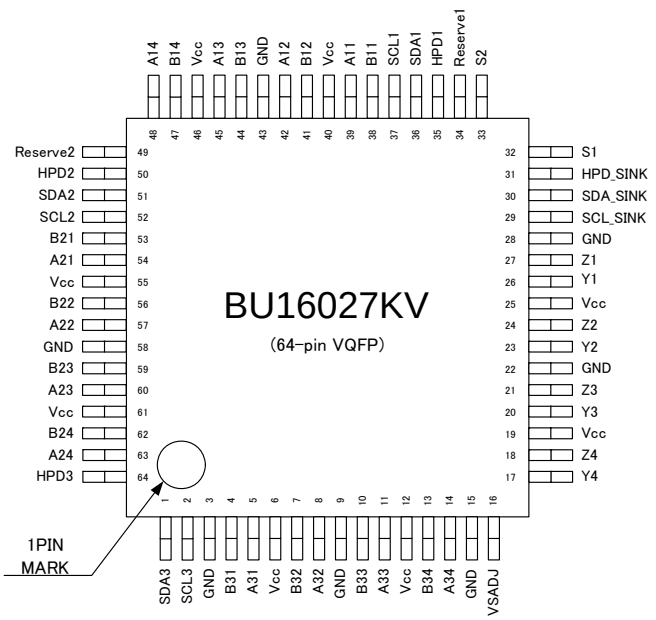


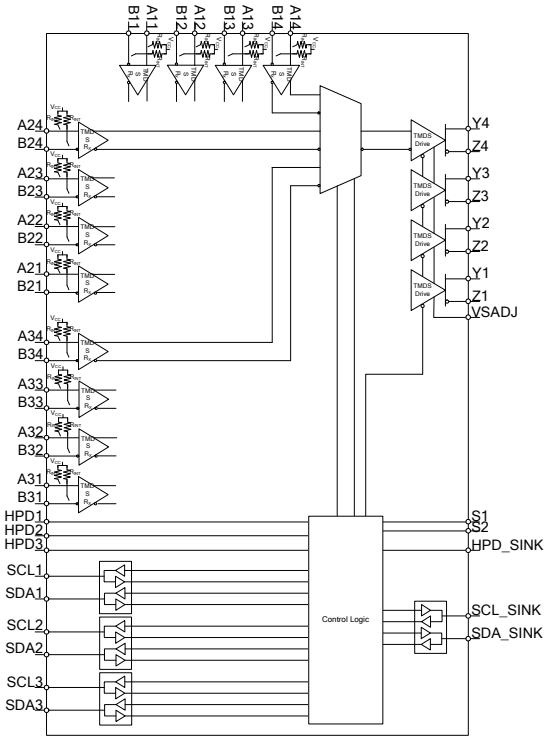
(*) when HPD_SINK = "L". Termination resistor is turned off.

●Pin Explanation List

Terminal		I/O	Description
Name	No.		
B1, B2, B3, B4	39, 42, 45, 2	I	TMDS Negative inputs
A1, A2, A3, A4	40, 43, 46, 3	I	TMDS Positive inputs
Z1, Z2, Z3, Z4	22, 19, 16, 11	O	TMDS Negative outputs
Y1, Y2, Y3, Y4	21, 18, 15, 10	O	TMDS Positive outputs
HPD	37	O	Source side hot plug detector output
HPD_SINK	24	I	Sink side hot plug detector input
SCL	34	I/O	Source port DDC I^2C clock line
SDA	33	I/O	Source port DDC I^2C data line
SCL_SINK	27	I/O	Sink port DDC I^2C clock line
SDA_SINK	28	I/O	Sink port DDC I^2C data line
VSADJ	35	I	TMDS voltage swing control(4.64kΩ to GND)
I^2CEN	6	I	I^2C Repeater enable Low : High-Z High : Active
SELREF	30	I	SCL_SINK/SDA_SINK Output voltage select
TEST0, 1, 2, 3	1, 12, 25, 36	I	Open or GND connect (recommend)
N.C	13, 48		Open or GND connect (recommend)
OEB	7	I	TMDS Output enable Low : Active High : High-Z
PRE	8	I	TMDS high speed mode SW High : ON, Low : OFF (above 165MHz recommend to High)
V_{CC}	5, 14, 20, 29, 32, 41, 47	-	Power supply
GND	4, 9, 17, 23, 26, 31, 38, 44	-	Ground

●Pin Assignment and Block Diagram of BU16027KV





●Pin Explanation List

Terminal		I/O	Description
Name	No.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58	-	Ground
HPD1	35	O	Source port 1 hot plug detector output (status pin)
HPD2	50	O	Source port 2 hot plug detector output (status pin)
HPD3	64	O	Source port 3 hot plug detector output (status pin)
HPD_SINK	31	I	Sink port hot plug detector input (status pin)
Reserve1	34	I/O	In High, Low, and Open, any setting is OK.
Reserve2	49	I/O	Non Connect Pin
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL3	2	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I^2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA3	1	I/O	Source port 3 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32, 33	I	Source selector
Vcc	6, 12, 19, 25, 40, 46, 55, 61	-	Power supply
VSADJ	16	I	TMDS voltage swing control (via 4.64kΩ to GND)
Y1, Y2, Y3, Y4	26, 23, 20, 17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27, 24, 21, 18	O	Sink port TMDS negative outputs

●Source Selection Lookup Table of BU16006KV

Control Pins			I/O Selected	Output Status			
HPD_SINK	**S1**	**S2**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	H	H	A1/B1 Termination resistors of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	H	L	L
H	L	H	A2/B2 Termination resistors of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	H	L
H	L	L	Disallowed (indeterminate) State All termination resistors are disconnected	None (Z)	L	L	H
H	H	L	None (Z) All termination resistors are disconnected		H	H	H
L	H	H	Disallowed (indeterminate) State All termination resistors are disconnected	SCL1 SDA1	L	L	L
L	L	H	Disallowed (indeterminate) State All termination resistors are disconnected	SCL2 SDA2	L	L	L
L	L	L	Disallowed (indeterminate)State All termination resistors are disconnected	None (Z)	L	L	L
L	H	L	None (Z) All termination resistors are disconnected		L	L	L

●Source Selection Lookup Table of BU16027KV

Control Pins			I/O Selected	Output Status			
HPD_SINK	**S1**	**S2**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H/L	H	H	A1/B1 Termination resistors of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD _SINK	L	L
H/L	L	H	A2/B2 Termination resistors of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD _SINK	L
H/L	L	L	A3/B3 Termination resistors A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD _SINK
H/L	H	L	None (Z) All terminations are disconnected	None (Z)	HPD _SINK	HPD _SINK	HPD _SINK

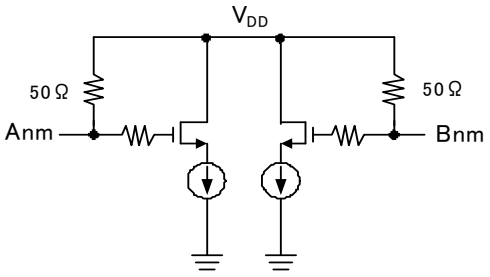
●Source Selection Lookup Table of BU16018KV

Control Pins				I/O Selected	Output Status			
HPD_SINK	**S1**	**S2**	**S3**	**Y/Z**	**SCL_SINK/SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	H	X	X	A1/B1 Termination resistors of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	H	L	L
H	L	H	X	A2/B2 Termination resistors of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	H	L
H	L	L	H	A3/B3 Termination resistors of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	H
H	L	L	L	None (Z) All terminations are disconnected	None (Z)	H	H	H
L	H	X	X	Disallowed (indeterminate)State All terminations are disconnected	SCL1 SDA1	L	L	L
L	L	H	X	Disallowed (indeterminate)State All terminations are disconnected	SCL2 SDA2	L	L	L
L	L	L	H	Disallowed (indeterminate)State All terminations are disconnected	SCL3 SDA3	L	L	L
L	L	L	L	None (Z) All terminations are disconnected	None (Z)	L	L	L

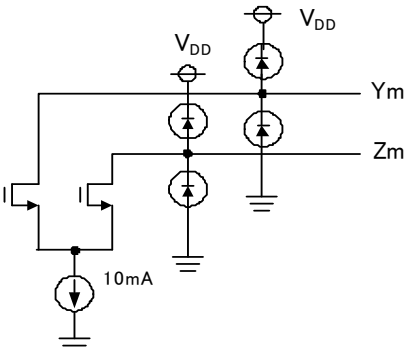
H: Logic high; L: Logic low; X: Don't care; Z: High impedance

●Equivalent Input And Output Schematic Diagrams

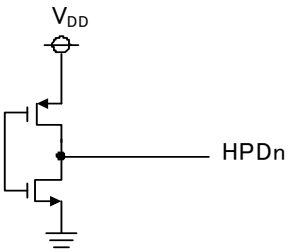
TMDS Input Stage



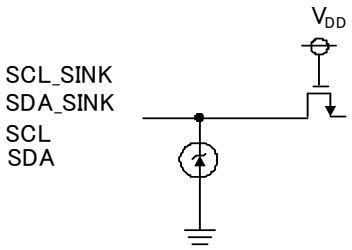
TMDS Output Stage



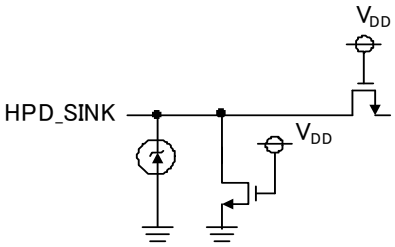
HPD Output Stage



R-Side I²C Input/Output Stage



T-Side I²C Input/Output Stage



※n=1,2,3 m=1,2,3,4

●Note for use

1). Attention on use as “repeater” or “source” equipment.
Y and Z terminals are connected to Vcc through ESD diode as Figure 7. When Vcc＋0.4 < AVcc, leak current flows from AVcc to Vcc. For this current, BU16006KV/BU16027KV can’t pass the compliance test as “Repeater” and “Source” equipment (Test ID 7-3 VOFF). BU16018KV/BU16024KV is able to pass the compliance test using external element like Figure 8

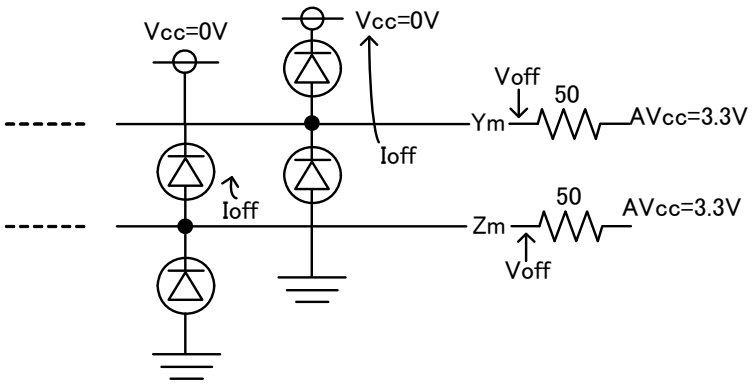


Figure 7 TMDS Equivalent output schematic

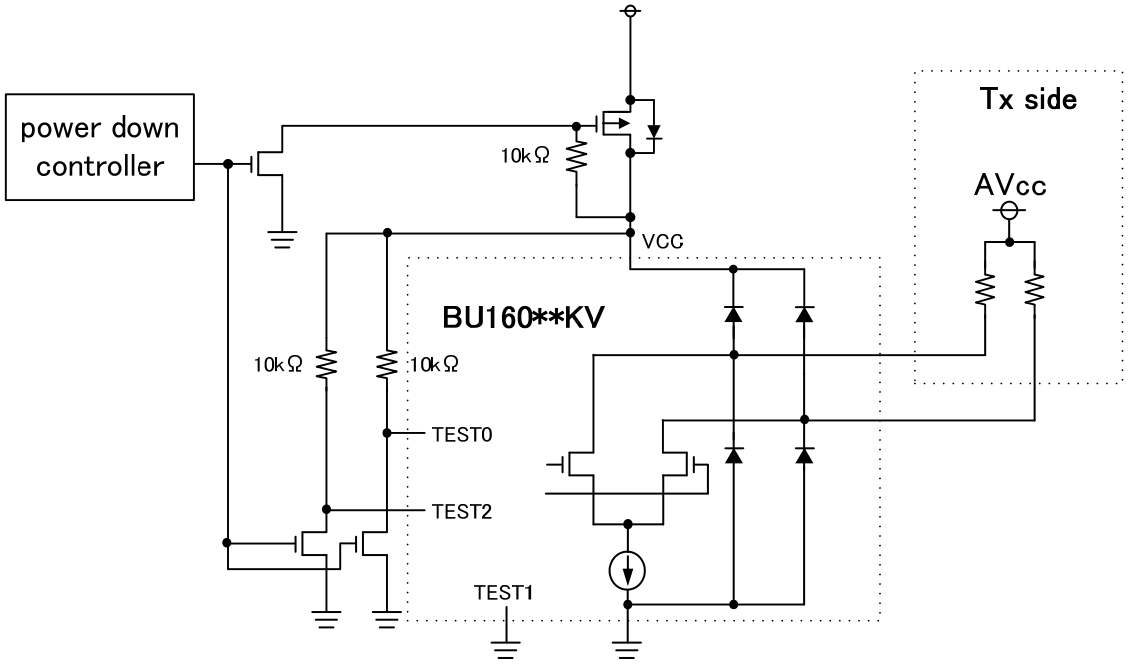


Figure 8 Leak current control in BU16018KV and BU16024KV

2). HPD_SINK Pull down resistance.
HPD_SINK have a 5V tolerant structure shown in Figure 9.It needs some drive current to pull down HPD_SINK "H" to "L". So to pull down HPD_SINK, please use 10kΩ(or under 10kΩ) resistor.

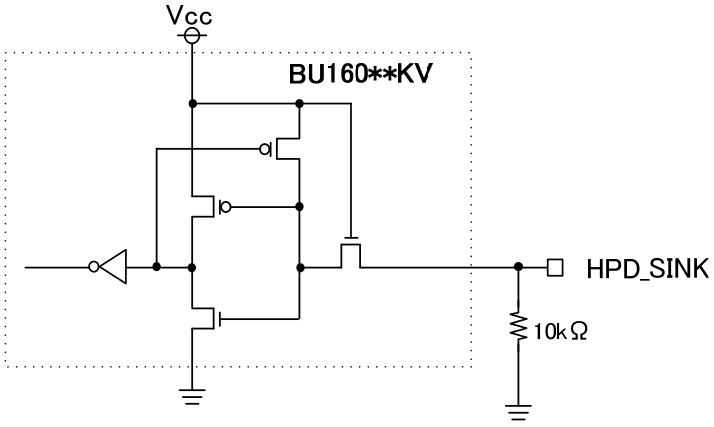


Figure 9 HPD_SINK I/O schematic

3). About don't use terminal.
3-1. Unused TMDS input channel recommend open.

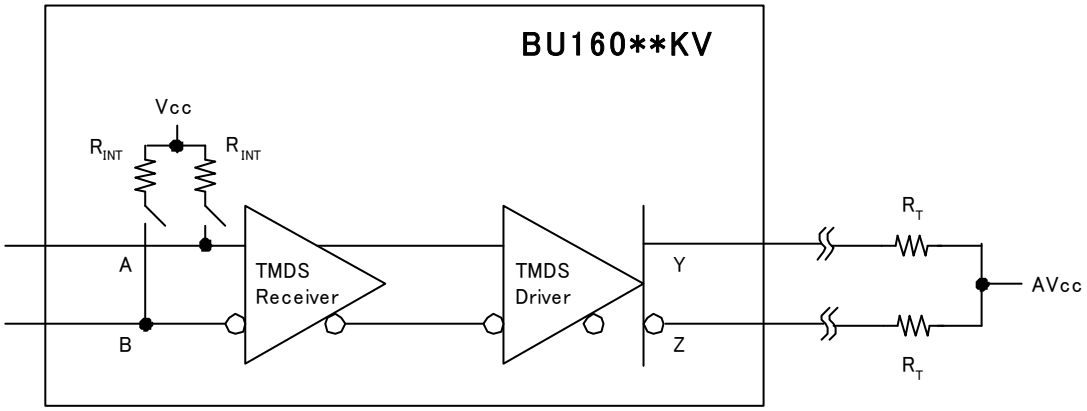


Figure 10 TMDS Input Recommendation

3-2. Unused DDC Buffers of R side recommend to pull up to Vcc.

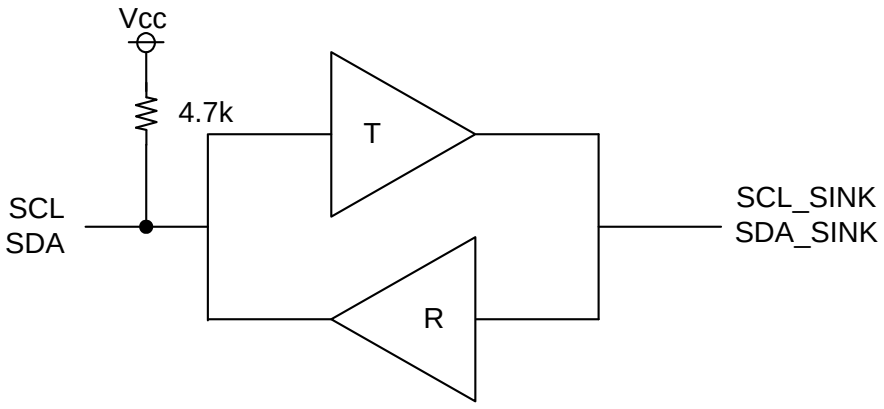


Figure 11 Unused DDC Buffers of R side

3-3. Unused DDC Buffers of R side recommend pull up to Vcc.

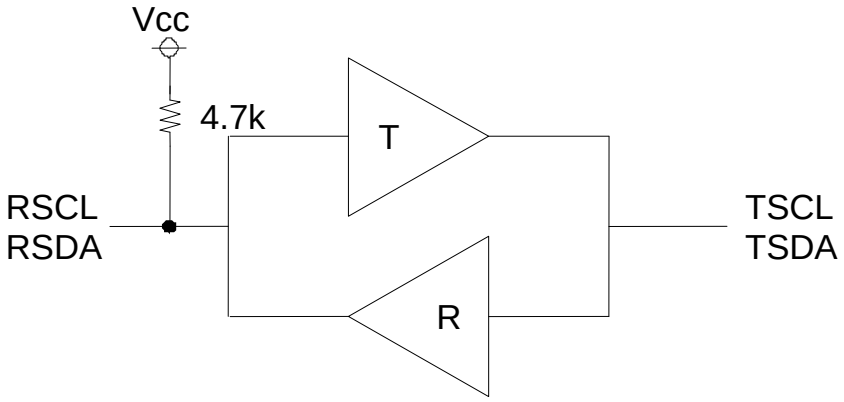


Figure 12 Unused DDC of T side

3-4. Unused HPDn recommend open.

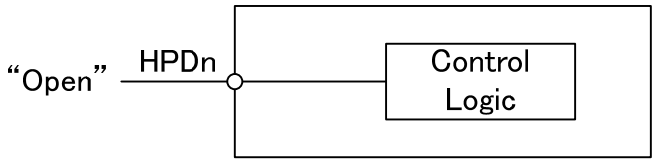


Figure 13 Open unused HPDn

4). About serial connection notice.
When BU160xxKV output connect to other HDMI sw input like following application the specification of Jitter tolerance is downed. Especially when system needs 1080p (12bit) data rate and cable or PCB trace lengths between BU160xxKV input and output is small, Deteriorations of Jitter tolerance is outstanding. This problem also depends on receiver IC characteristic. When system is required 1080p (12bit), Rohm doesn't recommend serial connect application.

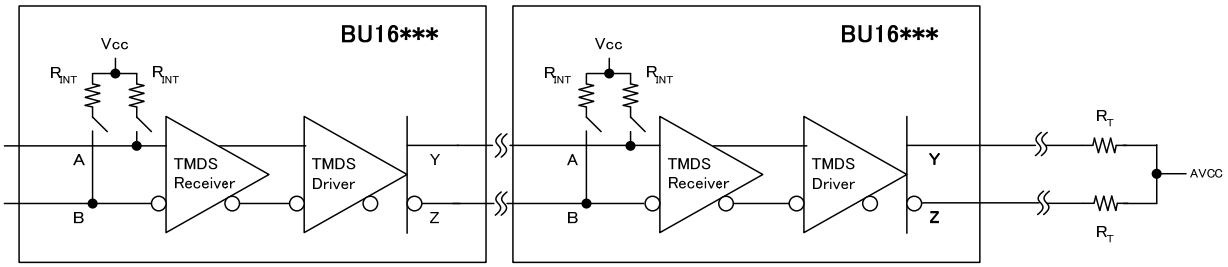


Figure 14 serial connection notice

5). AC Coupling notice
BU160xxKV can also communicate using AC coupling capacitor with TMDS line. But even connecting AC coupling capacitor, AC current may flow if input common mode voltage between two devices is different. For this current, the lower common mode voltage devices like PCIe or DP may be damaged by AC current.

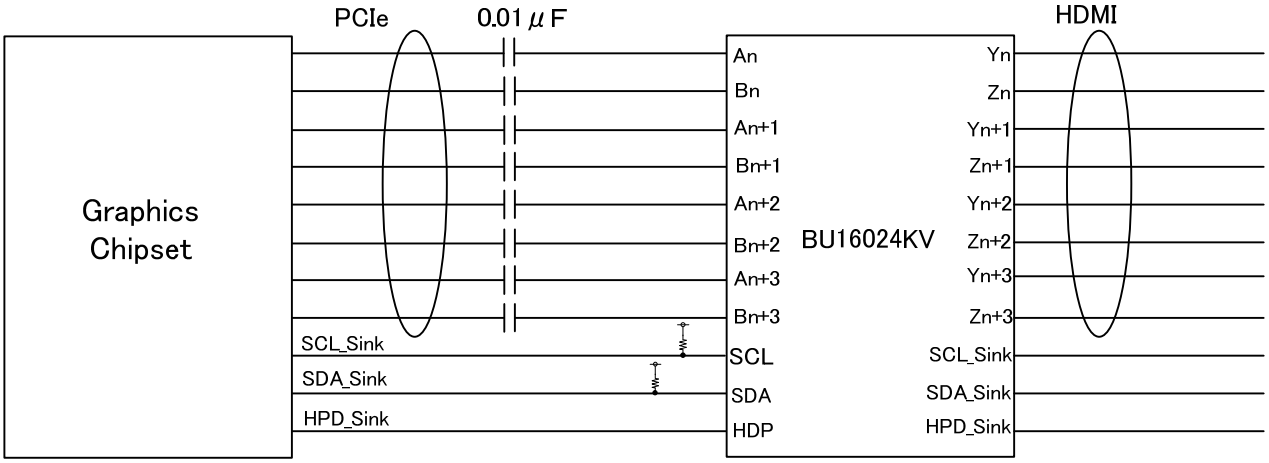


Figure 15 AC Coupling connection notice

6). TMDS output offset voltage notice.
Offset voltage may appear to TMDS output when there is no signal to TMDS input differential line. OE should set to “H” to avoid it.

7). Limitation of Master and slave direction as shown Figure 16.

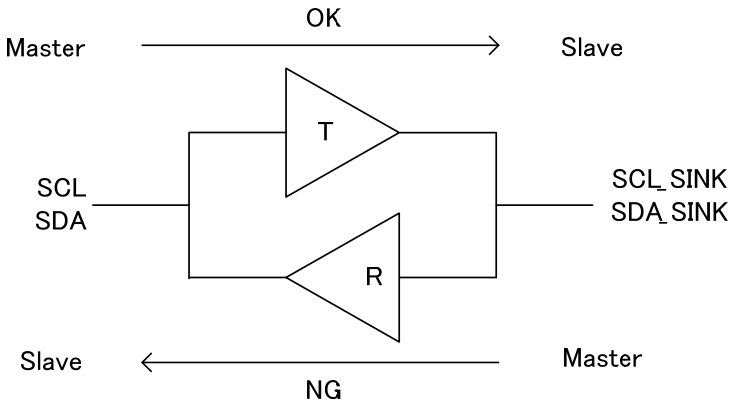


Figure 16 Limitation of Master and slave direction

●Ordering part number

B	U	1	6	0	0	6	K	V	-	E	2

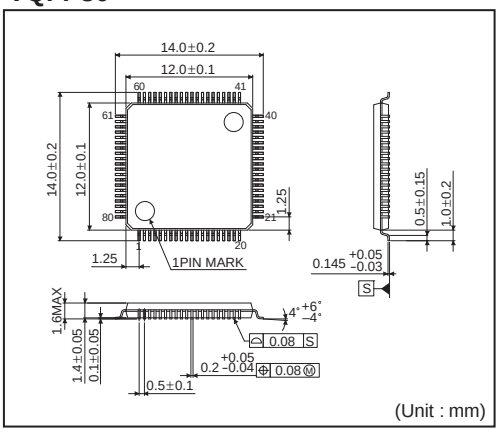
Part No.

Part No.
16006
16018
16024
16027

Package
KV: VQFP80
(BU16018),
VQFP64
(BU16027 /
BU16006),
VQFP48C
(BU16024)

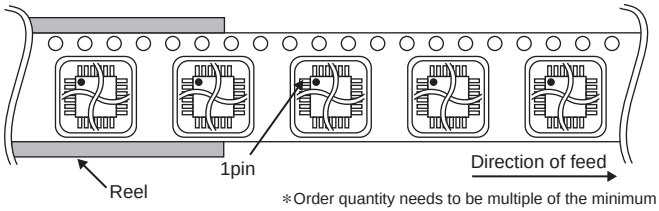
Packaging and forming specification
E2: Embossed tape and reel

VQFP80



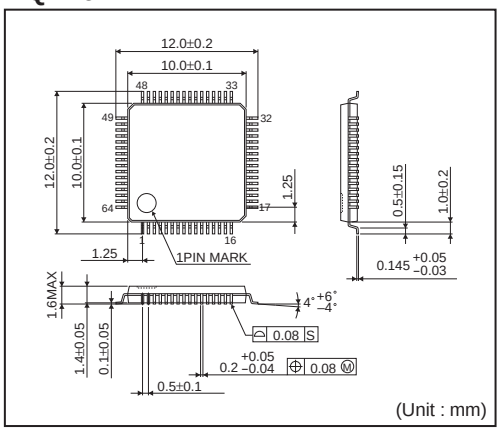
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



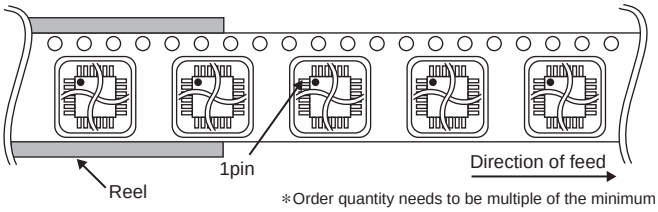
∗Order quantity needs to be multiple of the minimum quantity.

VQFP64



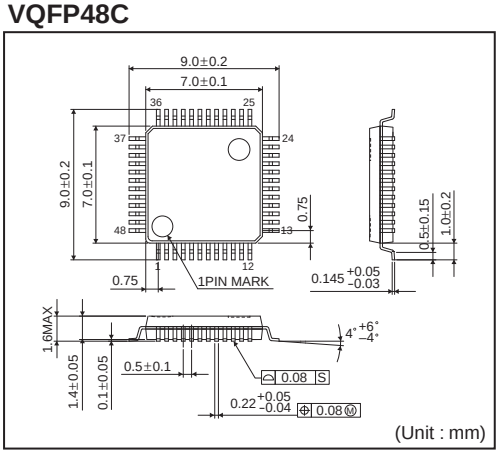
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



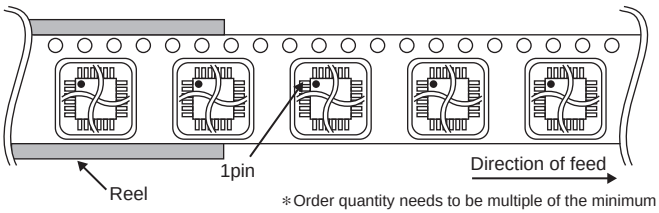
∗Order quantity needs to be multiple of the minimum quantity.

VQFP48C



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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