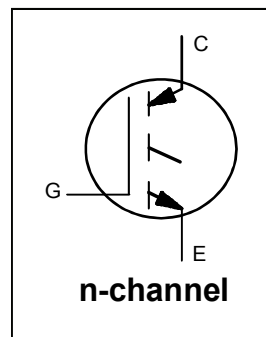


INSULATED GATE BIPOLAR TRANSISTOR

$V_{CES} = 1200V$ $I_{C(Nominal)} = 100A$ $T_{J(max)} = 175^{\circ}C$ $V_{CE(on)} \text{ typ} = 1.6V @ I_C = 100A$



G	C	E
Gate	Collector	Emitter

Applications

- Medium Power Drives
- UPS
- HEV Inverter
- Welding
- Induction Heating

Features	Benefits
Low $V_{CE(ON)}$ and switching Losses	High efficiency in a wide range of applications and switching frequencies
Square RBSOA and Maximum Junction Temperature $175^{\circ}C$	Improved Reliability due to rugged hard switching performance and higher power capability
Positive $V_{CE(ON)}$ Temperature Coefficient	Excellent current sharing in parallel operation
Integrated Gate Resistor	Easier Paralleling with Integrated Gate Resistor

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG7CH75UEF-R	Die on film	Wafer	1	IRG7CH75UEF-R

Mechanical Parameter

Die Size	10.4 x 10.4	mm ²
Minimum Street Width	75	μm
Emitter Pad Size (Included Gate Pad)	See Die Drawing	mm ²
Gate Pad Size	1.0 x 1.7	
Area Total / Active	108.2/81.3	
Thickness	120	μm
Wafer Size	200	mm
Notch Position	0	Degrees
Maximum-Possible Chips per Wafer	236 pcs	
Passivation Front side	Silicon Nitride	
Front Metal	Al, Si (4μm)	
Backside Metal	Al- Ti - Ni- Ag (1kA°-1kA°-4kA°-6kA°)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, $T_J=25^\circ\text{C}$	1200	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ②	400	A
V_{GE}	Gate Emitter Voltage	± 30	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	$^\circ\text{C}$

Static Characteristics (Tested on wafers) . $T_J=25^\circ\text{C}$

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	$V_{GE} = 0\text{V}, I_C = 100\mu\text{A}$ ③
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	—	2.0		$V_{GE} = 15\text{V}, I_C = 100\text{A}, T_J = 25^\circ\text{C}$
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	3.0	—	6.0		$I_C = 5.0\text{mA}, V_{CE} = V_{CE}$
I_{CES}	Zero Gate Voltage Collector Current	—	1.0	25	μA	$V_{CE} = 1200\text{V}, V_{GE} = 0\text{V}$
I_{GES}	Gate Emitter Leakage Current	—	—	± 400	nA	$V_{CE} = 0\text{V}, V_{GE} = \pm 30\text{V}$
$R_{G\text{ INTERNAL}}$	Internal Gate Resistance	1.9	2.5	3.1	Ω	

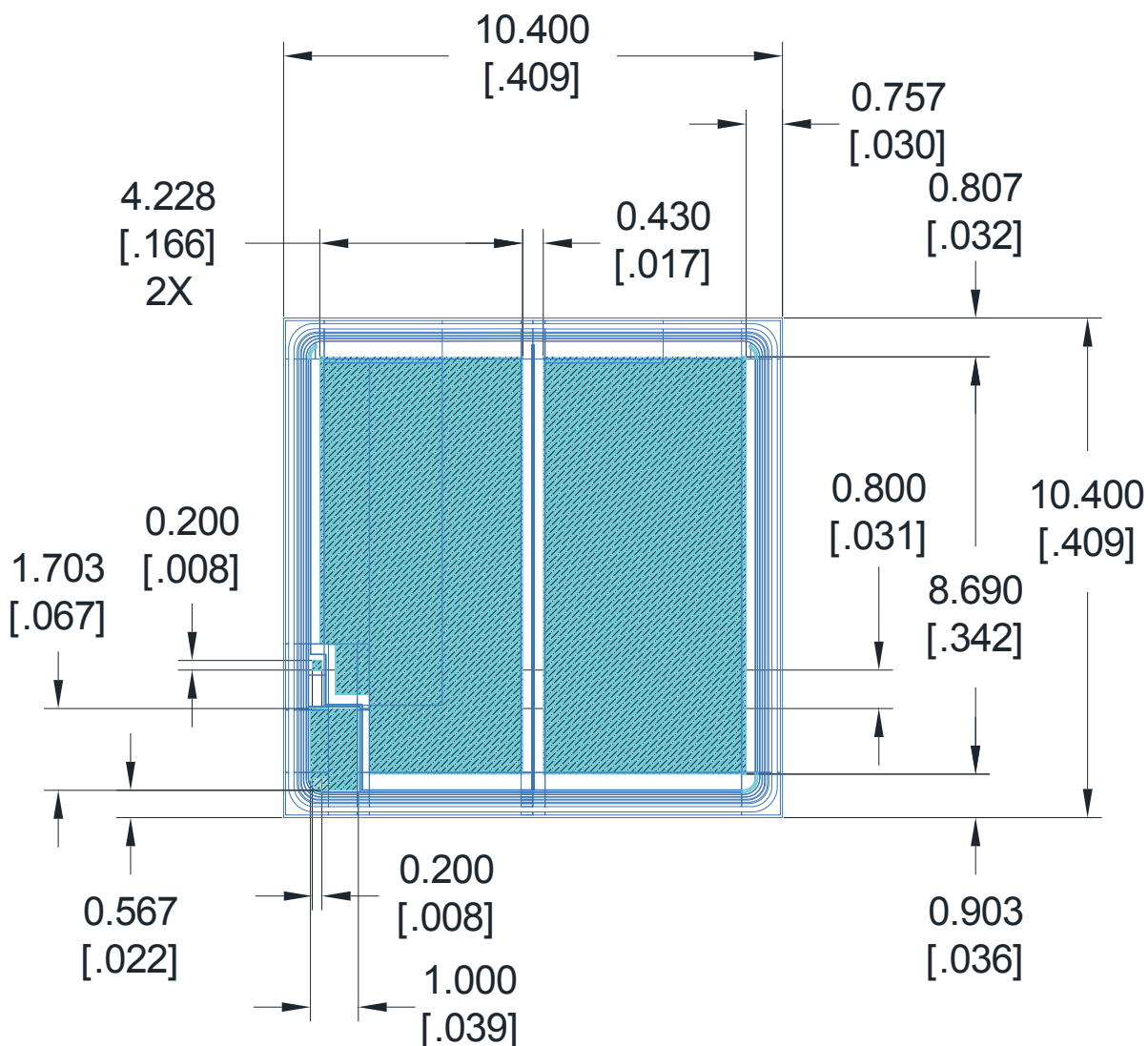
Electrical Characteristics (Not subject to production test- Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.6	—	V	$V_{GE} = 15\text{V}, I_C = 100\text{A}, T_J = 25^\circ\text{C}$ ④
		—	2.0	—		$V_{GE} = 15\text{V}, I_C = 100\text{A}, T_J = 175^\circ\text{C}$ ④
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 400\text{A}$ $V_{CC} = 960\text{V}, V_p \leq 1200\text{V}$ $R_g = 5\Omega, V_{GE} = +20\text{V to } 0\text{V}$
C_{iss}	Input Capacitance	—	12500	—	pF	$V_{GE} = 0\text{V}$
C_{oss}	Output Capacitance	—	460	—		$V_{CE} = 30\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	320	—		$f = 1.0\text{MHz}$
Q_g	Total Gate Charge (turn-on)	—	770	—	nC	$I_C = 100\text{A}$
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	90	—		$V_{GE} = 15\text{V}$
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	330	—		$V_{CC} = 600\text{V}$

Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions ⑤
$t_{d(on)}$	Turn-On delay time	—	120	—	ns	$I_C = 100\text{A}, V_{CC} = 600\text{V}$ $R_G = 5\Omega, V_{GE}=15\text{V}, L=100\mu\text{H}$ $T_J = 25^\circ\text{C}$
t_r	Rise time	—	100	—		
$t_{d(off)}$	Turn-Off delay time	—	890	—		
t_f	Fall time	—	80	—		
$t_{d(on)}$	Turn-On delay time	—	80	—		$I_C = 100\text{A}, V_{CC} = 600\text{V}$ $R_G = 5\Omega, V_{GE}=15\text{V}, L= 100\mu\text{H}$ $T_J = 175^\circ\text{C}$
t_r	Rise time	—	110	—		
$t_{d(off)}$	Turn-Off delay time	—	1060	—		
t_f	Fall time	—	140	—		

Die Drawing


NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: INCHES
3. DIE WIDTH AND LENGTH TOLERANCE: -0.0508 [.002]
4. DIE THICKNESS = 0.120 [.0047]

REFERENCE: IRG7CH75UB-R

Notes:

- ① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
- ② $V_{CC} = 80\% (V_{CES})$, $V_{GE} = 20V$, $L = 100\mu H$, $R_G = 5\Omega$.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely
- ④ Die Level Characterization
- ⑤ Values influenced by parasitic L and C in measurement

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Further Information

For further information please contact your local IR Sales office or email your enquiry to <http://die.irf.com>