

05

T-45-23-21

# 9305

## VARIABLE MODULUS COUNTER

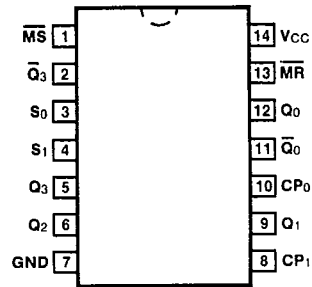
**DESCRIPTION** — The '05 is a monolithic, high speed, variable modulus counter circuit. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8 or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulus as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding Master Reset and Set inputs and the negation output of the final flip-flop output which allows the cascading of stages.

- **VARIOUS BINARY COUNTING MODES**  
 MODULO 2 AND MODULO 5, 6, 7, 8  
 MODULO 10 (8421 BCD) 12, 14, 16
- **VARIOUS DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**  
 MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**

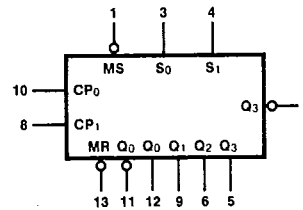
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	9305PC		9A
Ceramic DIP (D)	A	9305DC	9305DM	6A
Flatpak (F)	A	9305FC	9305FM	3B

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



V<sub>CC</sub> = Pin 14  
GND = Pin 7

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW
S <sub>0</sub> , S <sub>1</sub>	Select Inputs	1.0/1.0
CP <sub>0</sub>	First Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
CP <sub>1</sub>	Three Stage Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MS}$	Master Set Input (Active LOW)	1.0/1.0
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0
Q <sub>0</sub>	First Stage Output	16/8.0
$\overline{Q_0}$	Complementary First Stage Output	16/8.0
Q <sub>1</sub> — Q <sub>3</sub>	Three Stage Counter Outputs	16/8.0
$\overline{Q_3}$	Complementary Last Stage Output	20/10

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**FUNCTIONAL DESCRIPTION** — The '05 consists of four master/slave flip-flops which are separated into two functional units — a single toggle stage and a three stage synchronous counter. All four flip-flops change state on the LOW-to-HIGH transition of the clock. The three stage counter can be programmed with external connections to provide moduli of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

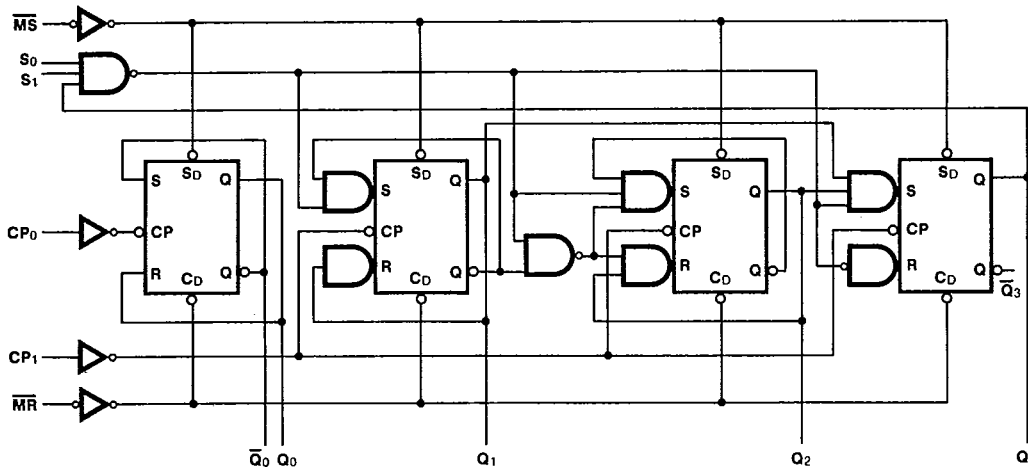
A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the  $\overline{Q}_3$  output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter moduli other than 10, 12, 14, 16 can be formed with a few extra gates.

Several '05 variable modulus counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the  $\overline{Q}_3$  output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs  $Q_0 - Q_3$  LOW and outputs  $\overline{Q}_0, \overline{Q}_3$  HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs  $Q_0 - Q_3$  HIGH and outputs  $\overline{Q}_0, \overline{Q}_3$  LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed.

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**LOGIC DIAGRAM**



**COUNTING MODE**

The following are rules specifying the external connections required for various counter and divider modulus.

**ASYNCHRONOUS MODE**

INPUTS		OUTPUTS					
MS	MR	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>3</sub>
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

\*As determined by programming connections.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

**PROGRAMMING CONNECTIONS FOR LAST THREE STAGES**

S <sub>0</sub>	S <sub>1</sub>	MODULO
NC	NC	5
Q <sub>1</sub>	NC	6
NC	Q <sub>1</sub>	6
Q <sub>2</sub>	NC	7
NC	Q <sub>2</sub>	7
Q <sub>1</sub>	Q <sub>2</sub>	8
Q <sub>2</sub>	Q <sub>1</sub>	8

NC = Not Connected

**CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS**

For Binary Counting Q <sub>0</sub> connected to CP <sub>1</sub> Incoming clock to CP <sub>0</sub>
For 50% Duty Cycle Output Q <sub>3</sub> connected to CP <sub>0</sub> Incoming Clock to CP <sub>1</sub>

**ALTERNATE PROGRAMMING CONNECTIONS FOR LAST THREE STAGES\*\***

MODULO	INPUTS		OUTPUT	AVAILABLE OUTPUT FAN-OUT
	S <sub>0</sub>	S <sub>1</sub>		
5	Q <sub>3</sub>	Q <sub>3</sub>	Q <sub>3</sub>	14/8.0
6	Q <sub>1</sub>	Q <sub>1</sub>	Q <sub>1</sub>	14/7.0
7	Q <sub>2</sub>	Q <sub>2</sub>	Q <sub>2</sub>	14/7.0
8	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>2</sub>	15/7.0
8	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>1</sub>	15/7.0

\*\*The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (See logic diagram), their connection to the counter outputs for the various count modulus provides the indicated output drive.

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**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
I <sub>SC</sub>	Output Short Circuit Current	-20	-70	mA	V <sub>CC</sub> = Max, V <sub>OUT</sub> = 0 V
I <sub>CC</sub>	Power Supply Current		66	mA	V <sub>CC</sub> = Max

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF			
		Min	Max		
f <sub>max</sub>	Maximum Count Frequency	23		MHz	Modulo 16 (S <sub>0</sub> to Q <sub>1</sub> , S <sub>1</sub> to Q <sub>2</sub> , Q <sub>0</sub> to CP <sub>1</sub> , Input to CP <sub>0</sub> ) Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>0</sub> to Q <sub>3</sub> (Modulo 16 Connection)		38 48	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>0</sub> to Q <sub>0</sub>		21 30	ns	Modulo-16 Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>1</sub> to Q <sub>3</sub> or Q <sub>3</sub>		23 30	ns	Modulo-8 Figs. 3-1, 3-8
t <sub>PLH</sub>	Propagation Delay M <sub>S</sub> to Q <sub>1</sub>		26	ns	Modulo-8 Figs. 3-1, 3-16
t <sub>PHL</sub>	Propagation Delay M <sub>R</sub> to Q <sub>1</sub>		35	ns	Modulo-8 Figs. 3-1, 3-16

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C

SYMBOL	PARAMETER	93XX		UNITS	CONDITIONS
		Min	Max		
t <sub>w</sub>	CP <sub>0</sub> Pulse Width	22		ns	Fig. 3-8
t <sub>w</sub>	M <sub>R</sub> or M <sub>S</sub> Pulse Width	24		ns	Fig. 3-16
t <sub>rec</sub>	Recovery Time M <sub>S</sub> to CP <sub>1</sub>	25		ns	Fig. 3-16
t <sub>rec</sub>	Recovery Time M <sub>R</sub> to CP <sub>1</sub>	30		ns	Fig. 3-16

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