

Power Switching Regulator

FEATURES

- Output Switch Current in Excess of 3.0A
- Operation from 2.5V to 40V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle-by-Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

TYPICAL APPLICATIONS

- Set-Top Boxes
- Industrial Controllers
- Network Boxes
- Automotive
- Computing
- Consumer Electronics

GENERAL DESCRIPTION

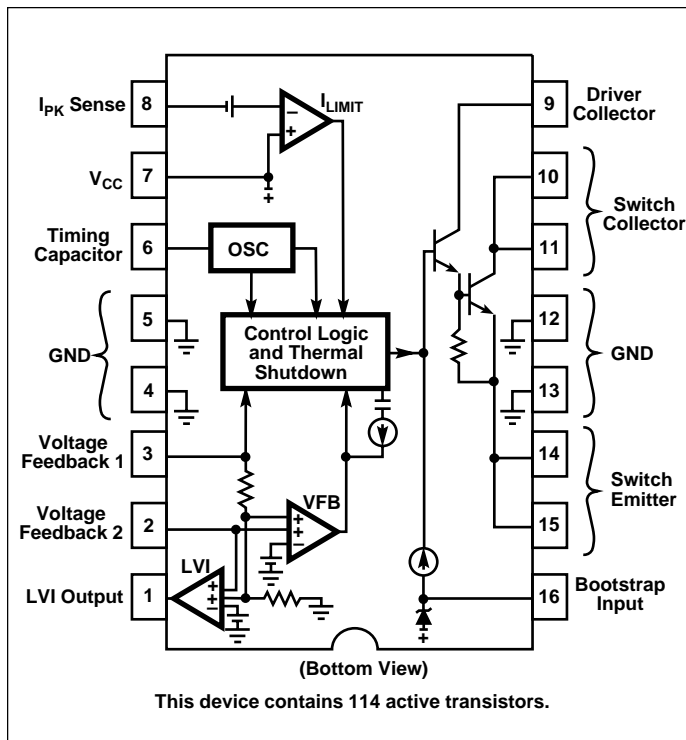
The TC33163 is a monolithic power switching regulator that contains the primary functions required for DC-to-DC converters. This device is specifically designed to be incorporated in step-up, step-down, and voltage-inverting applications with a minimum number of external components.

The TC33163 consists of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle-by-cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems. This device is contained in a 16-Pin dual-in-line heat tab plastic package for improved thermal conduction.

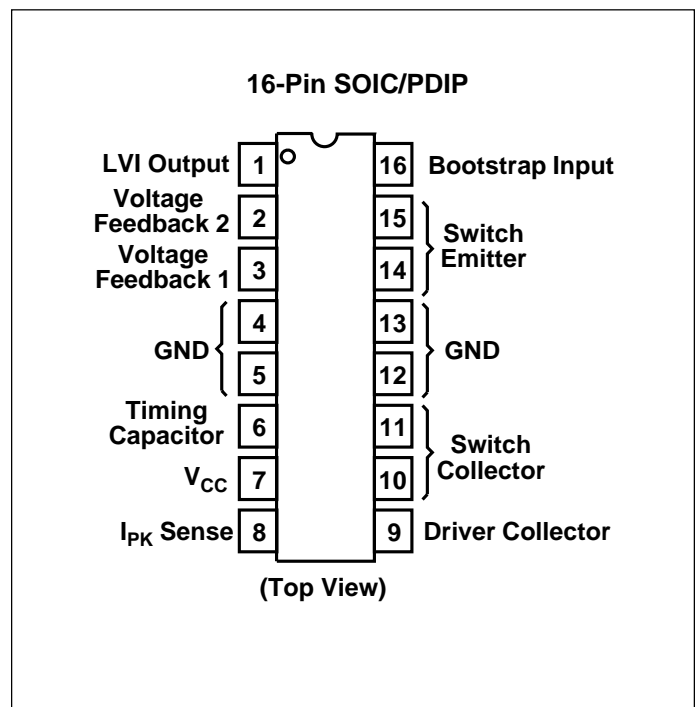
ORDERING INFORMATION

| Part Number | Package | Temperature Range |
|-------------|-----------------|----------------------------------|
| TC33163EOE | 16-Pin SOIC (W) | T _A = - 40° to + 85°C |
| TC33163EPE | 16-Pin PDIP (N) | T _A = - 40° to + 85°C |

REPRESENTATIVE BLOCK DIAGRAM



PIN CONFIGURATIONS



TC33163

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage $V_{CC} = 40V$
 Switch Collector Voltage Range $V_{C(SWITCH)} = -1.0$ to $40V$
 Switch Emitter Voltage Range $V_{E(SWITCH)} = -2.0$ to $V_{C(SWITCH)}$
 Switch Collector to Emitter Voltage $V_{CE(SWITCH)} = 40V$
 Switch Current (Note 1) $I_{SW} = 3.4A$
 Driver Collector Voltage $V_{C(DRIVER)} = -1.0$ to $40V$
 Driver Collector Current $I_{C(DRIVER)} = 150mA$
 Bootstrap Input Current Range (Note 1) $I_{BS} = -100$ to $+100mA$
 Current Sense Input Voltage Range:
 $V_{LPK(SENSE)} = (V_{CC} - 7.0)$ to $(V_{CC} + 1.0) V$
 Feedback and Timing Capacitor Input Voltage Range:
 $V_{IN} = -1.0$ to $+7.0V$
 Low Voltage Indicator Output Voltage Range:
 $V_{C(LVI)} = -1.0$ to $+40V$

Low Voltage Indicator Output Sink Current $I_{C(LVI)} = 10mA$

Thermal Characteristics:

16-Pin PDIP (N) Package

Thermal Resistance, Junction-to-Air $R_{\theta JA} = 80^{\circ}C/W$

Thermal Resistance, Junction-to-Case $R_{\theta JC} = 15^{\circ}C/W$

(Pins 4, 5 12, 13)

16-Pin SOIC (W) Package

Thermal Resistance, Junction-to-Air $R_{\theta JA} = 94^{\circ}C/W$

Thermal Resistance, Junction-to-Case $R_{\theta JC} = 18^{\circ}C/W$

(Pins 4, 5 12, 13)

Operating Junction Temperature $T_J = +150^{\circ}C$

Operating Ambient Temperature (Note 3) ... $T_A = -40$ to $+85^{\circ}C$

Storage Temperature Range $T_{STG} = -65$ to $+150^{\circ}C$

*This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{CC} = 15V$, Pin 16 = V_{CC} , $C_T = 620pF$, for typical values $T_A = 25^{\circ}C$, for min/max values T_A is the operating temperature range that applies (Note 3), unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|------------------------------|-----------------------------------|---|------------------|--------------------|---------------------|---------------|
| Oscillator | | | | | | |
| f_{OSC} | Frequency | $T_A = 25^{\circ}C$ Total variation over $V_{CC} = 2.5V$ to $40V$, and Temperature | 46 45 | 50 — | 54 55 | kHz |
| I_{CHG} | Charge Current | | — | 225 | — | μA |
| I_{DISCHG} | Discharge Current | | — | 25 | — | μA |
| I_{CHG} / I_{DISCHG} | Charge to Discharge Current Ratio | | 8.0 | 9.0 | 10 | — |
| $V_{OSC(P)}$ | Sawtooth Peak Voltage | | — | 1.25 | — | V |
| $V_{OSC(V)}$ | Sawtooth Valley Voltage | | — | 0.55 | — | V |
| Feedback Comparator 1 | | | | | | |
| $V_{TH(FB1)}$ | Threshold Voltage | $T_A = 25^{\circ}C$ Line Regulation ($V_{CC} = 2.5V$ to $40V$, $T_A = 25^{\circ}C$) Total Variation Over Line, and Temperature | 4.9 — 4.85 | 5.05 0.008 — | 5.2 0.03 5.25 | V %/V V |
| $I_{B(FB1)}$ | Input Bias Current | $V_{FB1} = 5.05V$ | — | 100 | 200 | μA |
| Feedback Comparator 2 | | | | | | |
| $V_{TH(FB2)}$ | Threshold Voltage | $T_A = 25^{\circ}C$ Line Regulation ($V_{CC} = 2.5V$ to $40V$, $T_A = 25^{\circ}C$) Total Variation Over Line, and Temperature | — 1.225 | 0.008 1.25 | 0.03 1.275 | %/V V |
| $I_{B(FB2)}$ | Input Bias Current | $V_{FB2} = 1.25V$ | -0.4 | 0 | 0.4 | μA |

- NOTES:**
1. Maximum package power dissipation limits must be observed.
 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 3. $T_{LOW} = -40^{\circ}C$ $T_{HIGH} = +85^{\circ}C$

Power Switching Regulator

TC33163

ELECTRICAL CHARACTERISTICS: $V_{CC} = 15V$, Pin 16 = V_{CC} , $C_T = 620pF$, for typical values $T_A = 25^\circ C$, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--|---|--|----------------|----------------|----------------|---------|
| Current Limit Comparator | | | | | | |
| $V_{TH(LPK\ SENSE)}$ | Threshold Voltage | $T_A = 25^\circ C$ Total Variation Over $V_{CC} = 2.5V$ to 40V, and Temperature | — 230 | 250 — | — 270 | mV |
| $I_{B(SENSE)}$ | Input Bias Current | $V_{LPK\ (SENSE)} = 15V$ | — | 1.0 | 20 | μA |
| Driver and Output Switch (Note 2) | | | | | | |
| $V_{CE(SAT)}$ | Sink Saturation Voltage Non-Darlington Connection Darlington Connection | $I_{SW} = 2.5A$, Pins 14, 15 Grounded $R_{PIN9} = 110\Omega$ to V_{CC} , $I_{SW}/I_{DRV} = 20$ Pins 9, 10, 11 Connected | — — | 0.6 1.0 | 1.0 1.4 | V |
| $I_{C(OFF)}$ | Collector Off-State Leakage Current | $V_{CE} = 40V$ | — | 0.02 | 100 | μA |
| $I_{SOURCE\ (DRV)}$ | Bootstrap Input Current Source | $V_{BS} = V_{CC} + 5.0V$ | 0.5 | 2.0 | 4.0 | mA |
| V_Z | Bootstrap Input Zener Clamp Voltage | $I_Z = 25mA$ | $V_{CC} + 6.0$ | $V_{CC} + 6.0$ | $V_{CC} + 9.0$ | V |
| Low Voltage Indicator | | | | | | |
| V_{TH} | Input Threshold | V_{FB2} Increasing | 1.07 | 1.125 | 1.18 | V |
| V_H | Input Hysteresis | V_{FB2} Decreasing | — | 15 | — | mV |
| $V_{OL(LVI)}$ | Output Sink Saturation Voltage | $I_{SINK} = 2.0mA$ | — | 0.15 | 0.4 | V |
| I_{OH} | Output Off-State Leakage Current | $V_{OH} = 15V$ | — | 0.01 | 5.0 | μA |
| Total Device | | | | | | |
| I_{CC} | Standby Supply Current | $V_{CC} = 2.5V$ to 40V, Pin 8 = V_{CC} , Pins 6, 14, 15 = GND, Remaining Pins Open | — | 6.0 | 10 | mA |

- NOTES:**
1. Maximum package power dissipation limits must be observed.
 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
 3. $T_{LOW} = -40^\circ C$ $T_{HIGH} = +85^\circ C$

TC33163

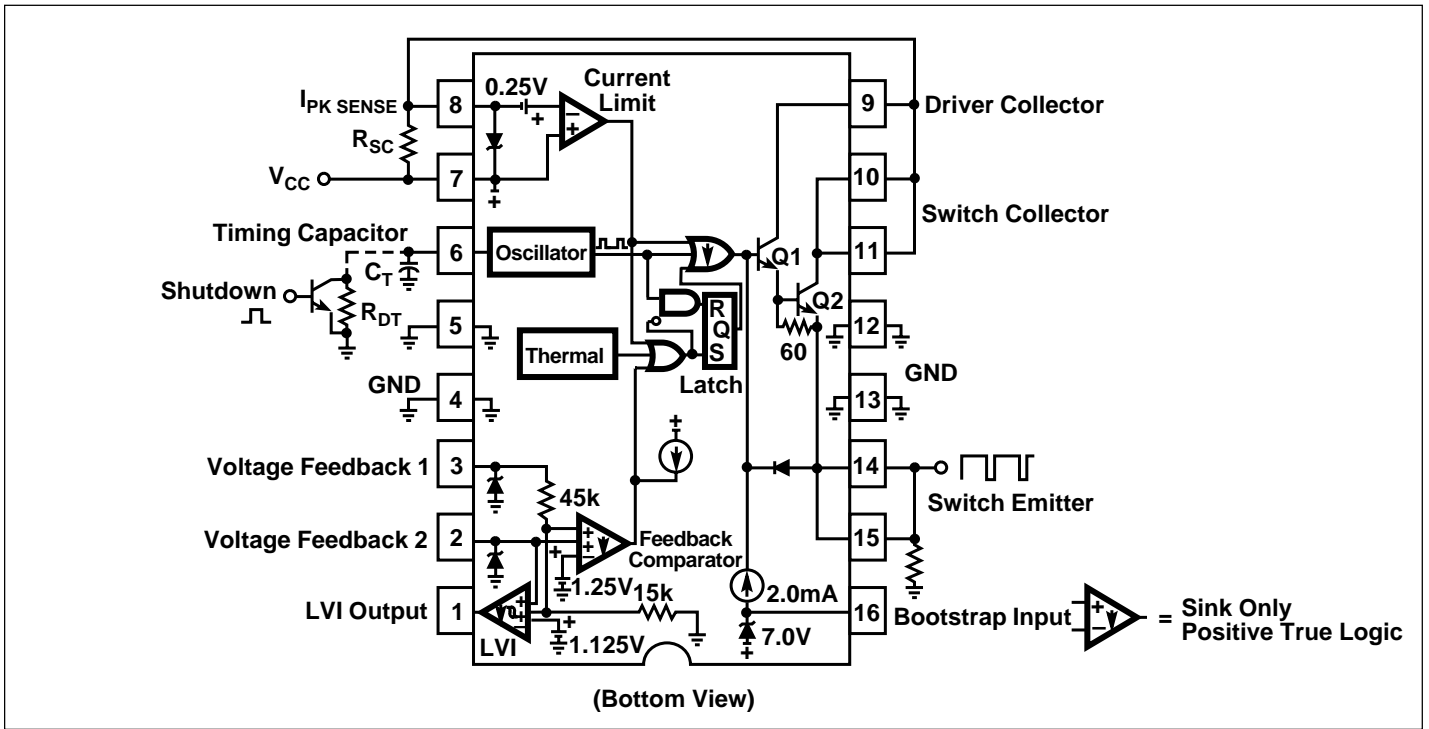


Figure 1. Representative Block Diagram

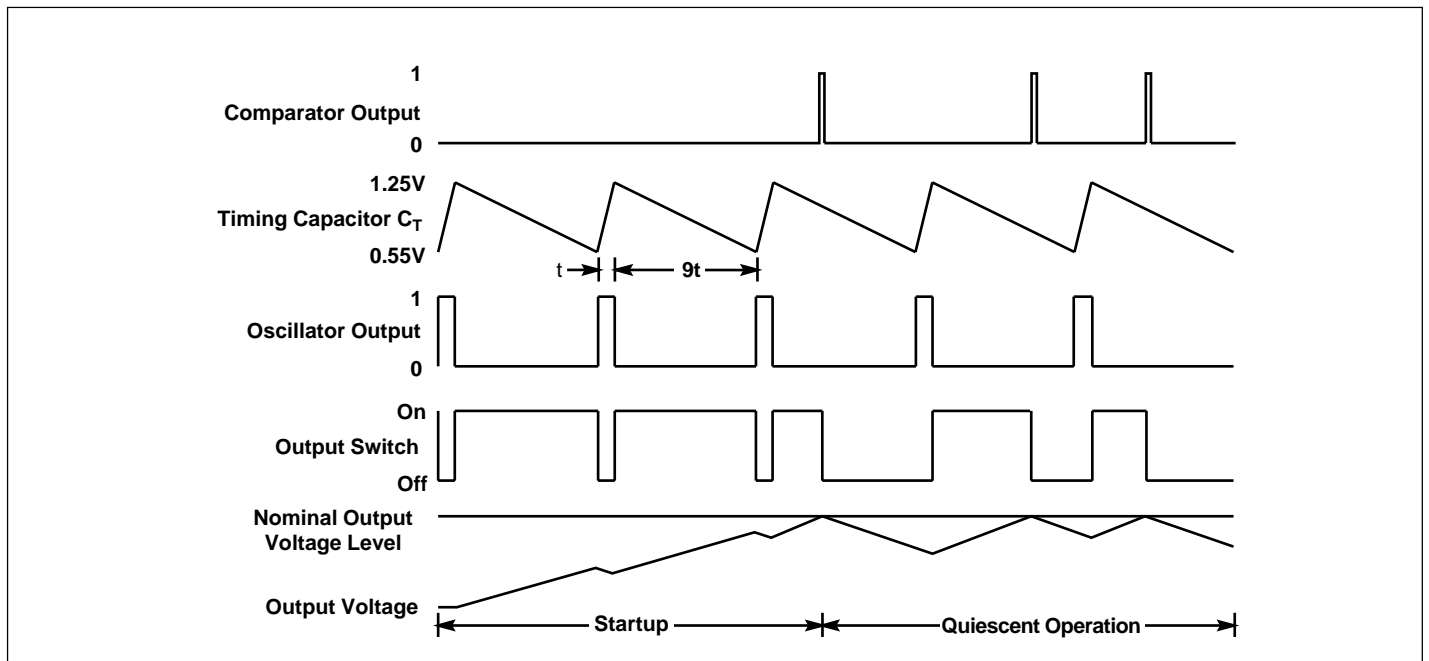


Figure 2. Typical Operating Waveforms

INTRODUCTION

The TC33163 series are monolithic power switching regulators optimized for DC-to-DC converter applications. The combination of features in this series enables the system designer to directly implement step-up, step-down, and voltage-inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 1.

OPERATING DESCRIPTION

The TC33163 operates as a fixed on-time, variable off-time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 2. The output voltage waveform shown is for a step-down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on-time of the output switch are programmed by the value selected for timing capacitor C_T . Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp-up and can be enabled by the comparator output only at the start of ramp-down. The oscillator peak and valley thresholds are 1.25V and 0.55V, respectively, with a charge current of 225 μ A and a discharge current of 25 μ A, yielding a maximum on-time duty cycle of 90%. A reduction of the maximum duty cycle may

This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T . The resistor increases the discharge current which reduces the on-time of the output switch. A graph of the Output Switch On-Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 11. Note that the maximum output duty cycle, ($t_{ON}/t_{ON} + t_{OFF}$), remains constant for values of C_T greater than 0.2nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small-signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is $\pm 0.4\mu$ A, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05V. The additional 50mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor-based systems. The inverting input is internally biased at 1.125V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0mA (see Figure 20). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{TH(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 3.

$$t_{DLY} = R_{LVI} C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{TH(MPU)}}{V_{OUT}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

TC33163

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC} , in series with V_{CC} and output switch transistor Q_2 . The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250mV with respect to V_{CC} , the comparator will set the latch and terminate output switch conduction on a cycle-by-cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on-time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25V}{I_{PK(SWITCH)}}$$

Figures 21 and 22 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 μ A. The propagation delay from the comparator input to the Output Switch is typically 200nsec. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5A and is designed to switch a maximum of 40V collector to emitter, with up to 3.4A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(MIN)} = \frac{0.25V}{3.4A} = 0.0735\Omega$$

When configured for step-down or voltage-inverting applications, as in Figures 3 and 7, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 19 shows that by clamping the emitter to 0.5V, the collector current will be in the range 10 μ A over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step-down and voltage-inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0mA bias current source above V_{CC} . An internal zener limits the bootstrap input voltage to $V_{CC} + 7.0V$. The capacitor's equivalent series resistance must limit the zener current to less than 100mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(MIN)} = 1 \frac{\Delta t}{\Delta V} = 4.0mA \frac{t_{ON}}{4.0V} = 0.001t_{ON}$$

Parametric operation of the TC33163 is guaranteed over a supply voltage range of 2.5V to 40V. When operating below 3.0V, the Bootstrap Input should be connected to V_{CC} . Figure 25 shows that functional operation down to 1.7V at room temperature is possible.

Package

The TC33163 is contained in a heatsinkable 16-lead plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 26 and 27 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction-to-air thermal resistance. These examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown of the circuit diagrams on the following page.

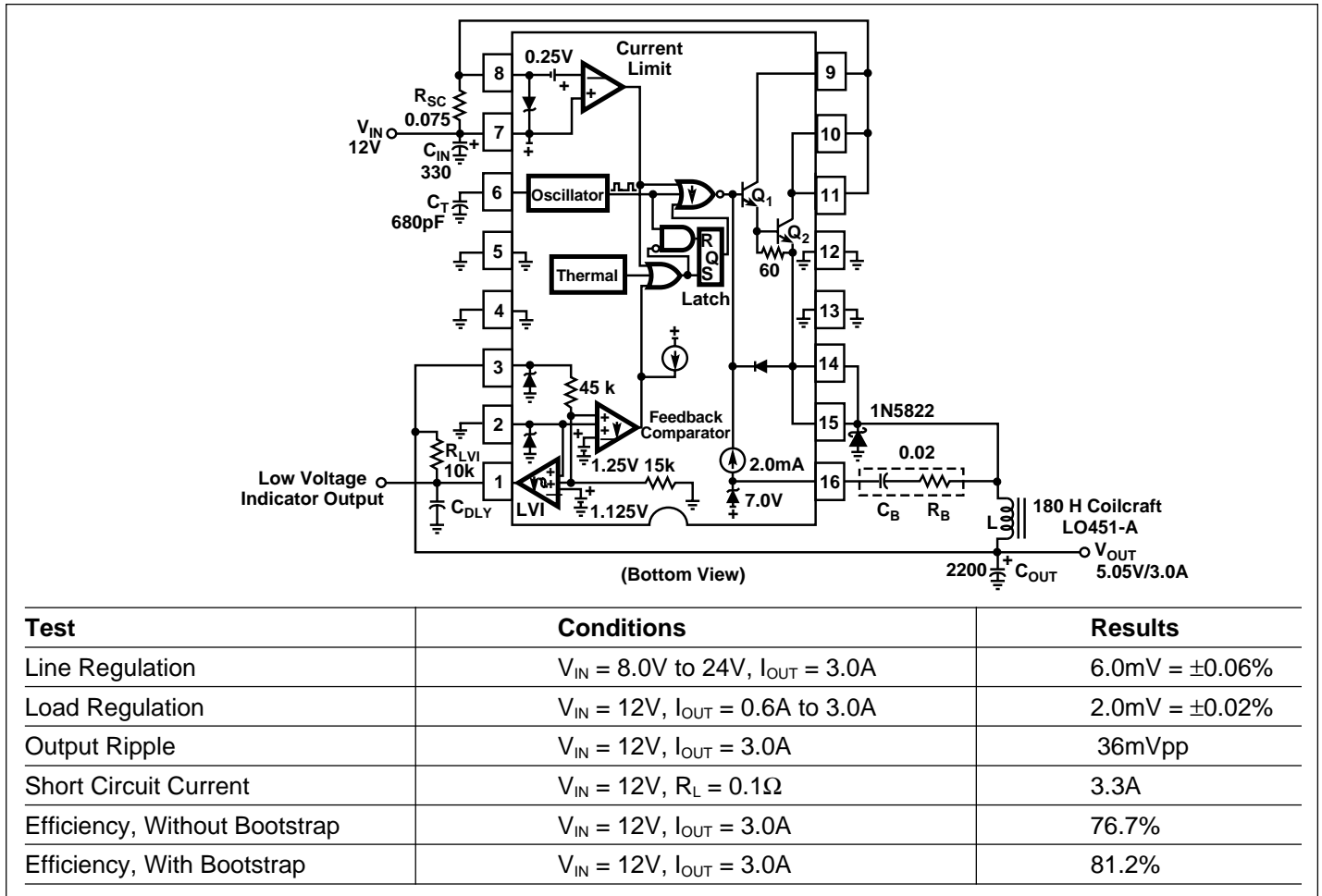


Figure 3. Step-Down Converter

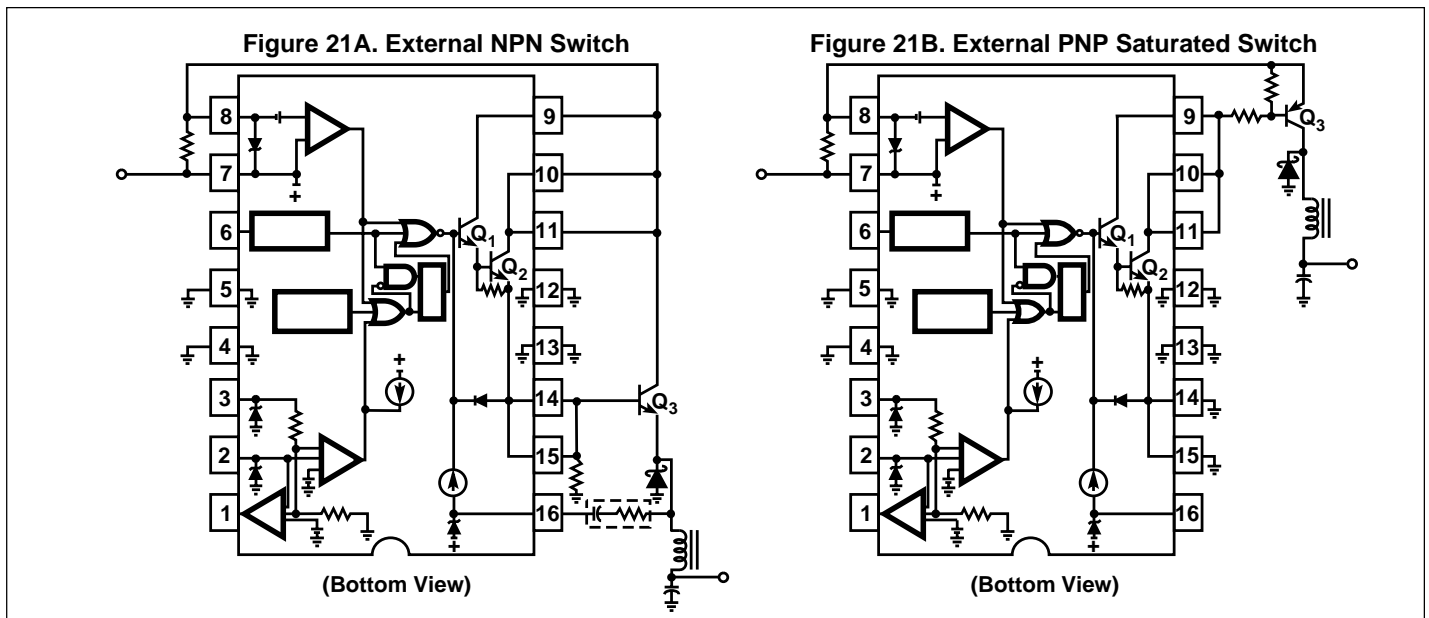
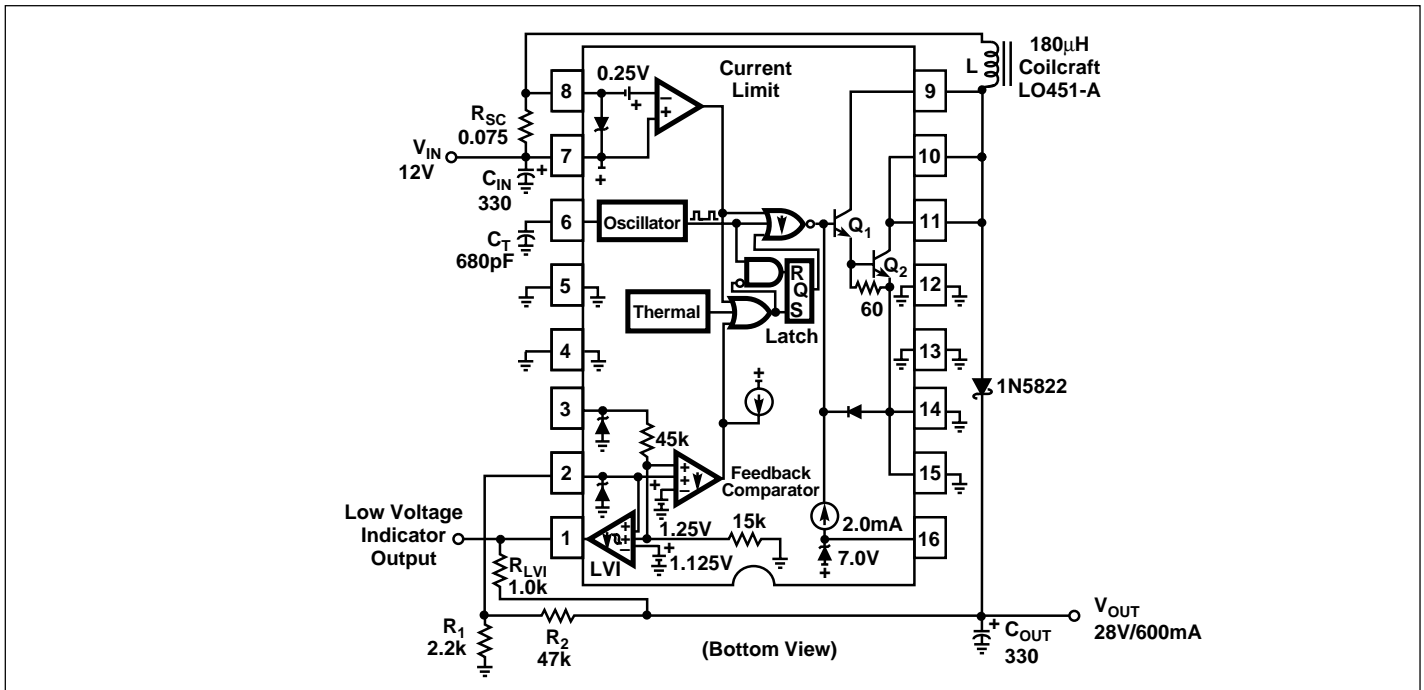


Figure 4. External Current Boost Connections for $I_{PK(SWITCH)}$ Greater than 3.4A

TC33163



| Test | Condition | Results |
|-----------------|---|---------------------|
| Line Regulation | $V_{IN} = 9.0V \text{ to } 16V, I_{OUT} = 0.6A$ | $30mV = \pm 0.05\%$ |
| Load Regulation | $V_{IN} = 12V, I_{OUT} = 0.1A \text{ to } 0.6A$ | $50mV = \pm 0.09\%$ |
| Output Ripple | $V_{IN} = 12V, I_{OUT} = 0.6A$ | $140mV_{pp}$ |
| Efficiency | $V_{IN} = 12V, I_{OUT} = 0.6A$ | 88.1% |

Figure 5. Step-Up Converter

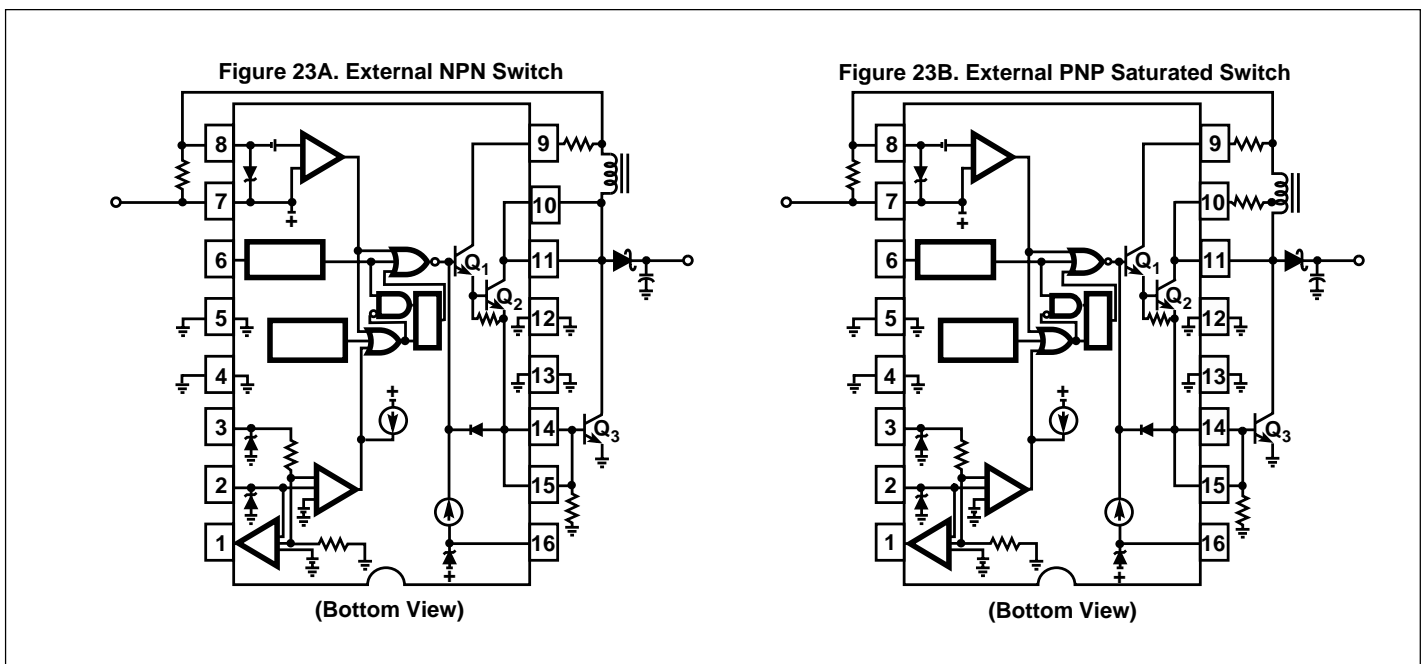
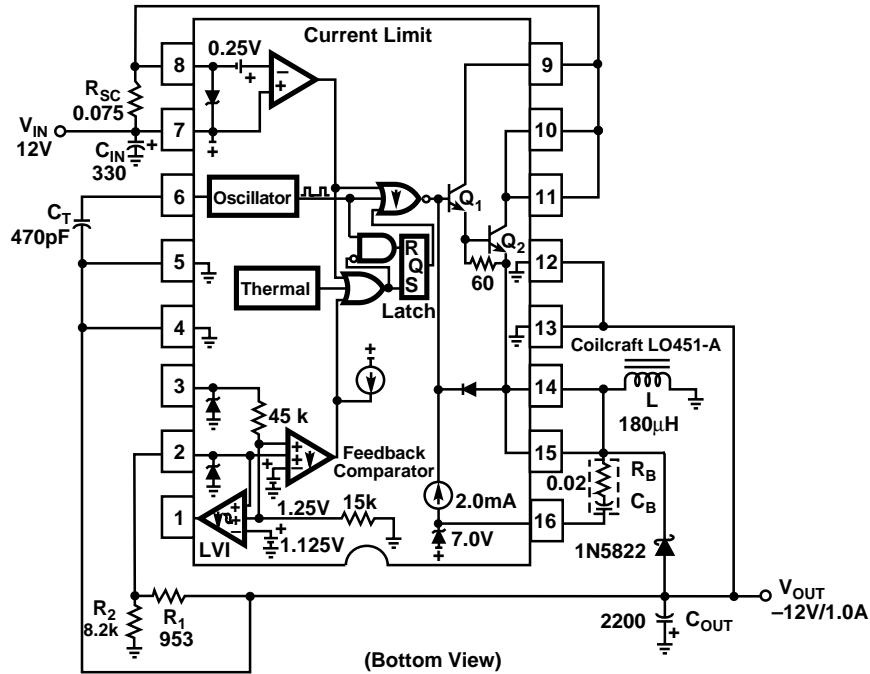


Figure 6. External Current Boost Connections for $I_{PK(SWITCH)}$ Greater than 3.4A



| Test | Condition | Results |
|-------------------------------|---|----------------------|
| Line Regulation | $V_{IN} = 9.0V$ to $16V$, $I_{OUT} = 1.0A$ | $5.0mV = \pm 0.02\%$ |
| Load Regulation | $V_{IN} = 12V$, $I_{OUT} = 0.6A$ to $1.0A$ | $2.0mV = \pm 0.01\%$ |
| Output Ripple | $V_{IN} = 12V$, $I_{OUT} = 1.0A$ | $130mV_{pp}$ |
| Short Circuit Current | $V_{IN} = 12V$, $R_L = 0.1\Omega$ | $3.2A$ |
| Efficiency, Without Bootstrap | $V_{IN} = 12V$, $I_{OUT} = 1.0A$ | 73.1% |
| Efficiency, With Bootstrap | $V_{IN} = 12V$, $I_{OUT} = 1.0A$ | 77.5% |

Figure 7. Voltage Inverting Converter

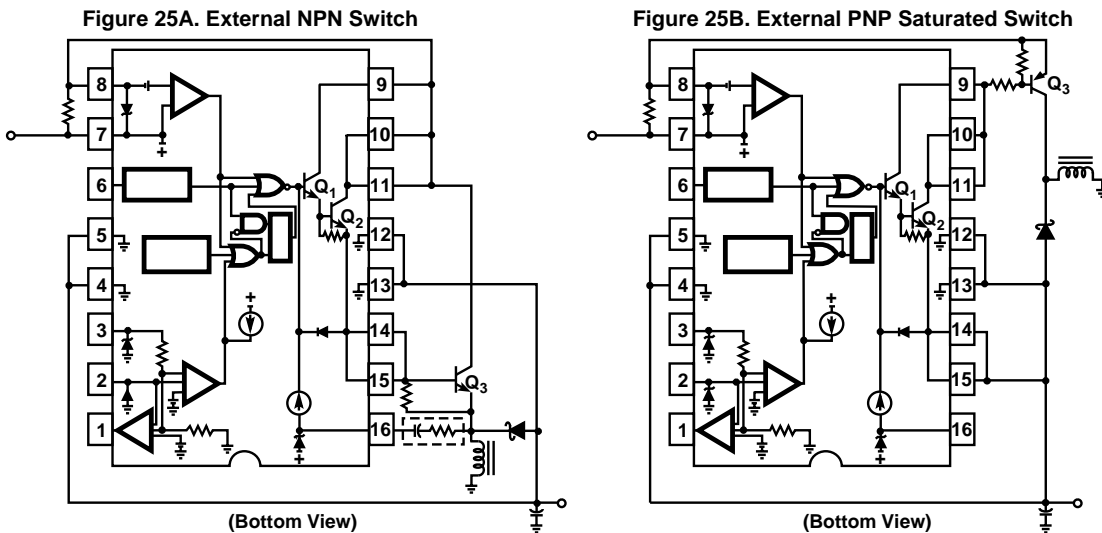


Figure 8. External Current Boost Connections for $I_{PK(SWITCH)}$ Greater than $3.4A$

TC33163

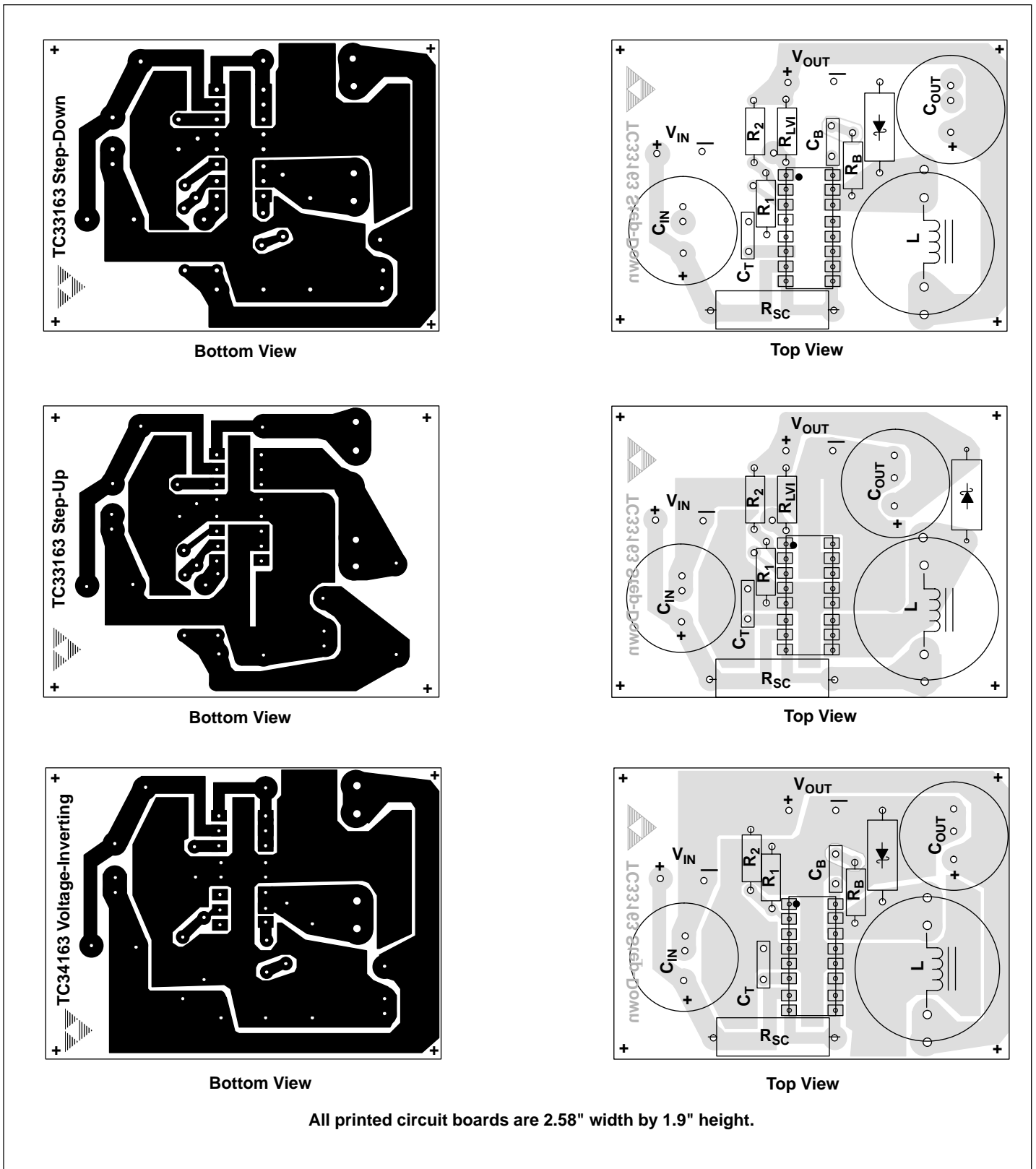


Figure 9. Printed Circuit Board and Component Layout (Circuits of Figures 3, 5, 7)

| Calculation | Step-Down | Step-Up | Voltage-Inverting |
|---|--|--|--|
| $\frac{t_{ON}}{t_{OFF}}$ (Notes 1, 2, 3) | $\frac{V_{OUT} + V_F}{V_{IN} - V_{SAT} - V_{OUT}}$ | $\frac{V_{OUT} + V_F - V_{IN}}{V_{IN} - V_{SAT}}$ | $\frac{V_{OUT} + V_F}{V_{IN} - V_{SAT}}$ |
| t_{ON} | $\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$ | $\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$ | $\frac{t_{ON}}{t_{OFF}} \cdot \frac{1}{f \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)}$ |
| C_T | $\frac{32.143 \cdot 10^{-6}}{f}$ | $\frac{32.143 \cdot 10^{-6}}{f}$ | $\frac{32.143 \cdot 10^{-6}}{f}$ |
| $I_{L(AVG)}$ | I_{OUT} | $I_{OUT} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$ | $I_{OUT} \left(\frac{t_{ON}}{t_{OFF}} + 1 \right)$ |
| R_{SC} | $\frac{0.25}{I_{PK(SWITCH)}}$ | $\frac{0.25}{I_{PK(SWITCH)}}$ | $\frac{0.25}{I_{PK(SWITCH)}}$ |
| $I_{PK(SWITCH)}$ | $I_{L(AVG)} + \frac{\Delta I_L}{2}$ | $I_{L(AVG)} + \frac{\Delta I_L}{2}$ | $I_{L(AVG)} + \frac{\Delta I_L}{2}$ |
| L | $\left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{\Delta I_L} \right) t_{ON}$ | $\left(\frac{V_{IN} - V_{SAT}}{\Delta I_L} \right) t_{ON}$ | $\left(\frac{V_{IN} - V_{SAT}}{\Delta I_L} \right) t_{ON}$ |
| $V_{RIPPLE(PP)}$ | $\Delta I_L \sqrt{\left(\frac{1}{8f C_O} \right)^2 + (ESR)^2}$ | $\approx \frac{t_{ON} I_{OUT}}{C_O}$ | $\approx \frac{t_{ON} I_{OUT}}{C_O}$ |
| V_{OUT} | $V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$ | $V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$ | $V_{REF} \left(\frac{R_2}{R_1} + 1 \right)$ |

Figure 10. Design Equations

The Following Converter Characteristics must be chosen:

- V_{IN} – Nominal operating input voltage.
- V_{OUT} – Desired output voltage.
- I_{OUT} – Desired output current.
- ΔI_L – Desired peak-to-peak output ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(AVG)}$. This will help prevent $I_{PK(SWITCH)}$ from reaching the current limit threshold set by R_{SC} . If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(AVG)})$. This will proportionally reduce converter output current capability.
- f – Maximum output switch frequency.
- $V_{RIPPLE(PP)}$ – Desired peak-to-peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

- NOTES:**
1. V_{SAT} – Saturation voltage of the output switch, refer to Figures 17 and 18.
 2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5V.
 3. The calculated t_{ON}/t_{OFF} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

TYPICAL CHARACTERISTICS

Figure 11. Output Switch On-Off Time Versus Oscillator Timing Capacitor

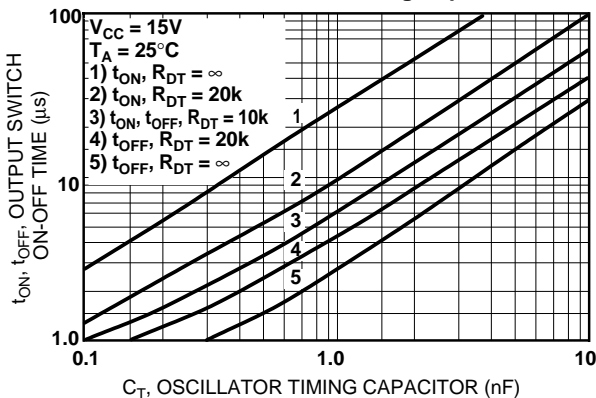
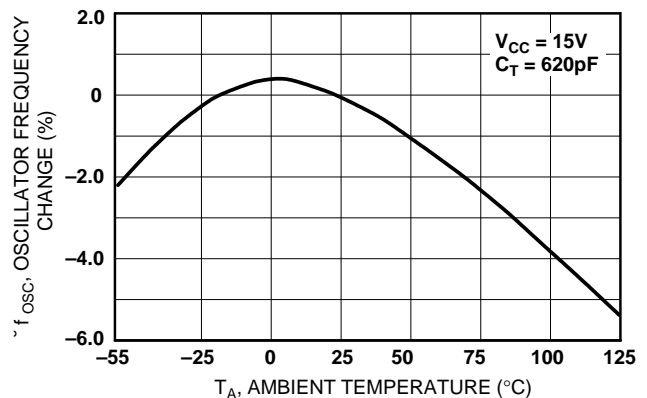


Figure 12. Oscillator Frequency Change Versus Temperature



TC33163

TYPICAL CHARACTERISTICS

Figure 13. Feedback Comparator 1 Input Bias Current Versus Temperature

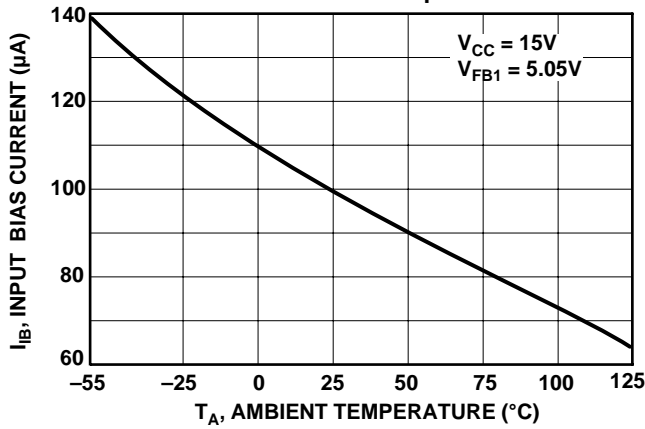


Figure 14. Feedback Comparator 2 Threshold Voltage Versus Temperature

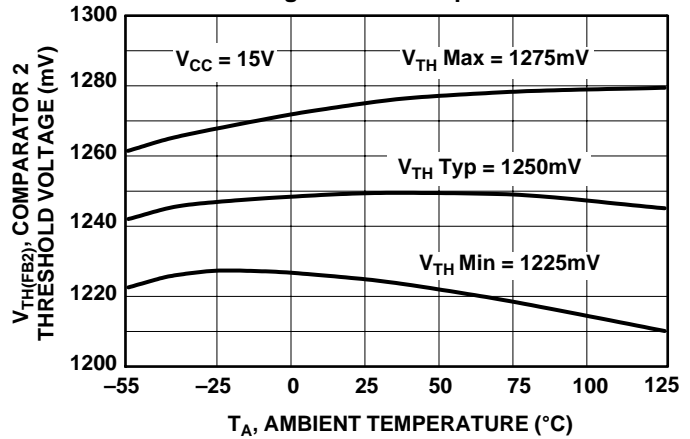


Figure 15. Bootstrap Input Current Source Versus Temperature

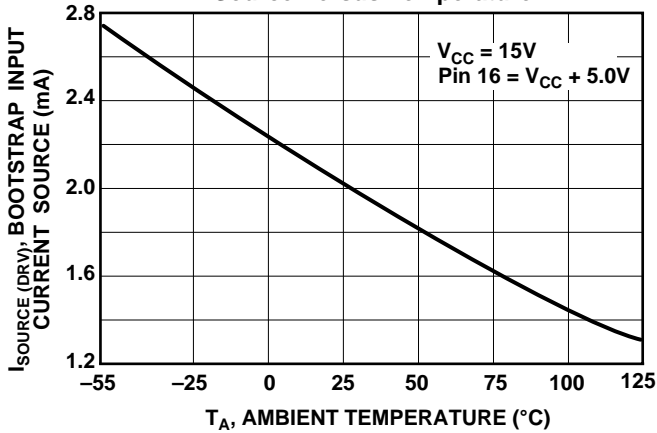


Figure 16. Bootstrap Input Zener Clamp Voltage Versus Temperature

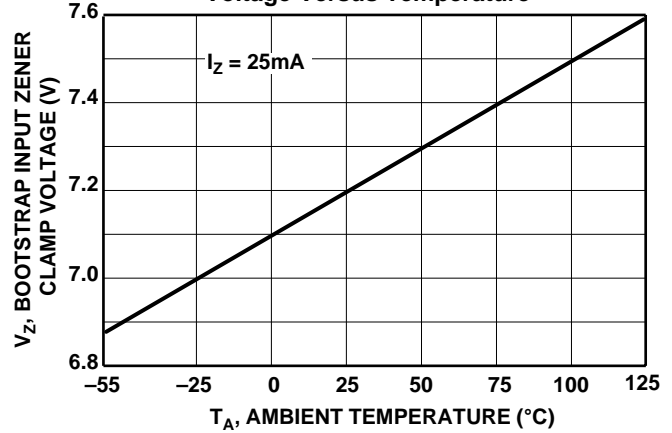


Figure 17. Output Switch Source Saturation Versus Emitter Current

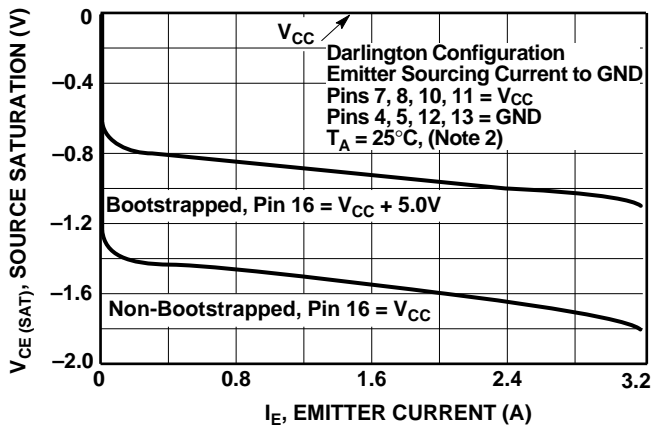
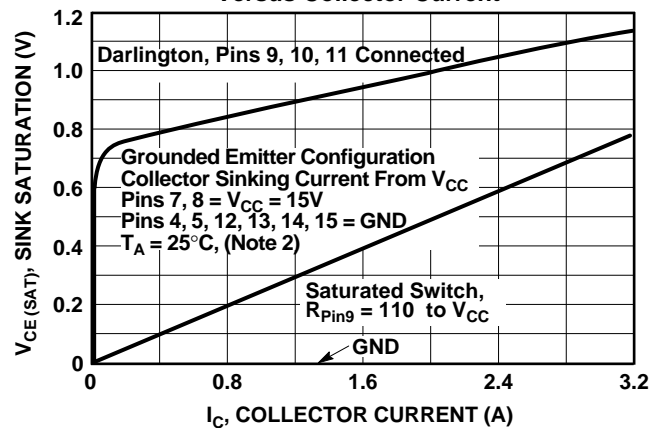


Figure 18. Output Switch Sink Saturation Versus Collector Current



TYPICAL CHARACTERISTICS

Figure 19. Output Switch Negative Emitter Voltage Versus Temperature

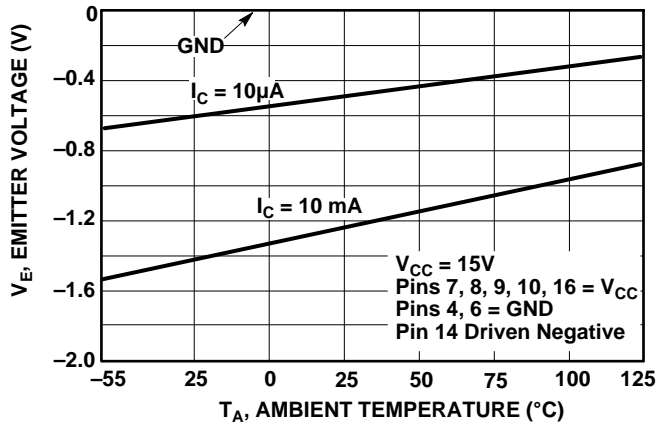


Figure 20. Low Voltage Indicator Output Sink Saturation Voltage Versus Sink Current

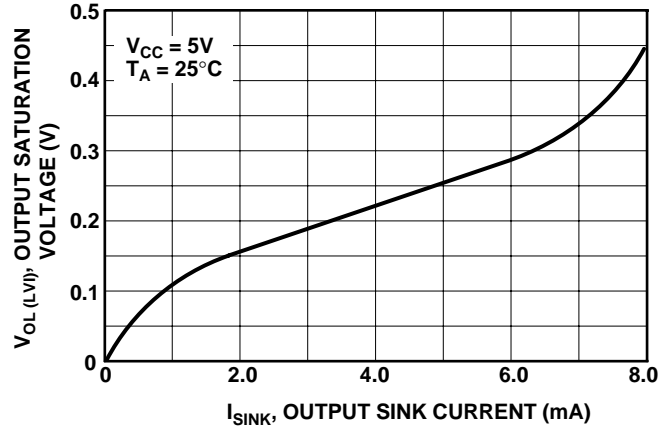


Figure 21. Current Limit Comparator Threshold Voltage Versus Temperature

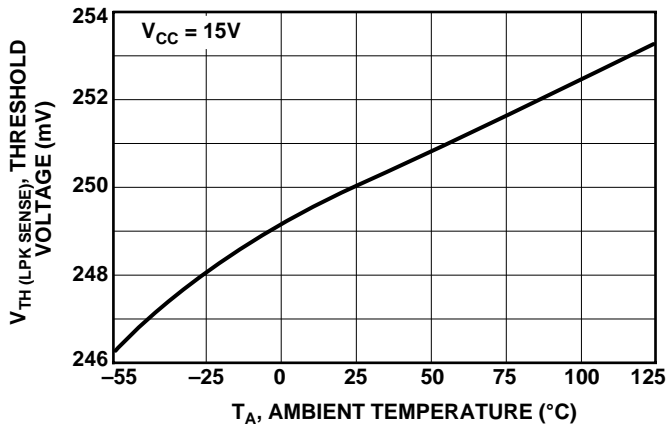


Figure 22. Current Limit Comparator Input Bias Current Versus Temperature

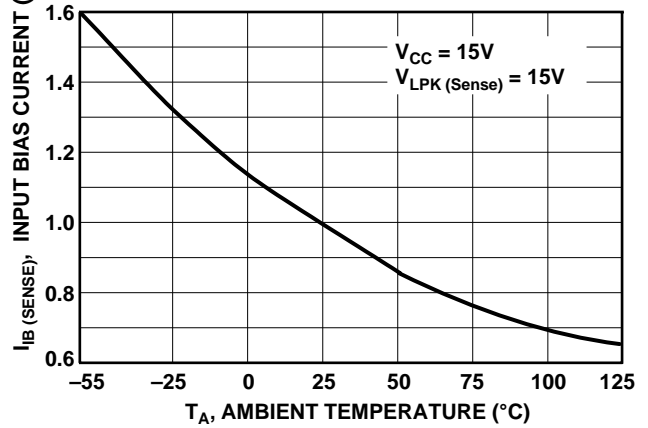


Figure 23. Standby Supply Current versus Supply Voltage

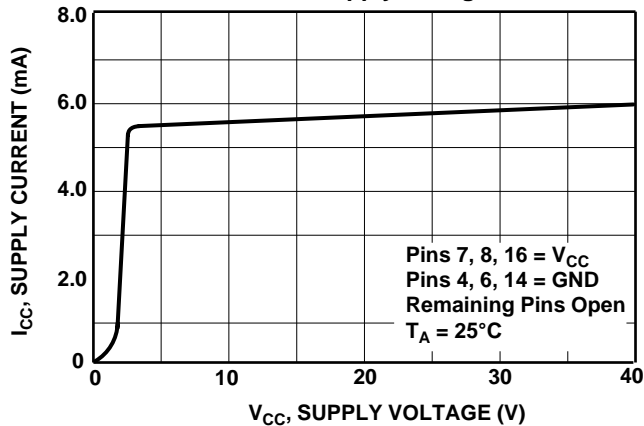
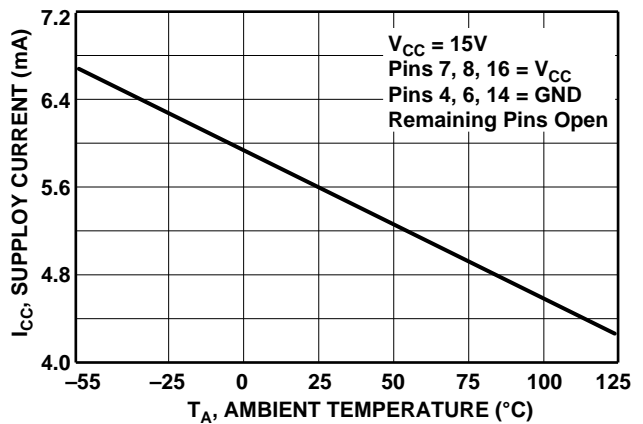


Figure 24. Standby Supply Current versus Temperature



TC33163

TYPICAL CHARACTERISTICS

Figure 25. Minimum Operating Supply Voltage Versus Temperature

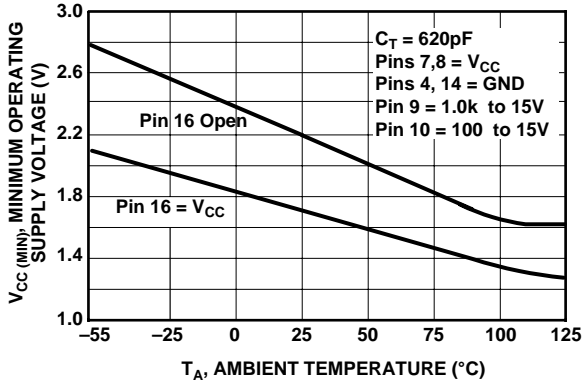


Figure 26. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

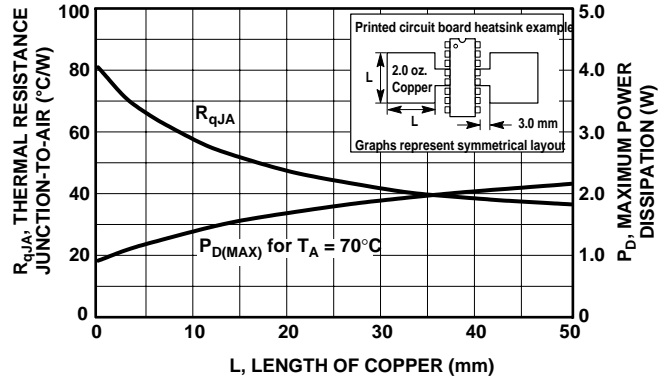
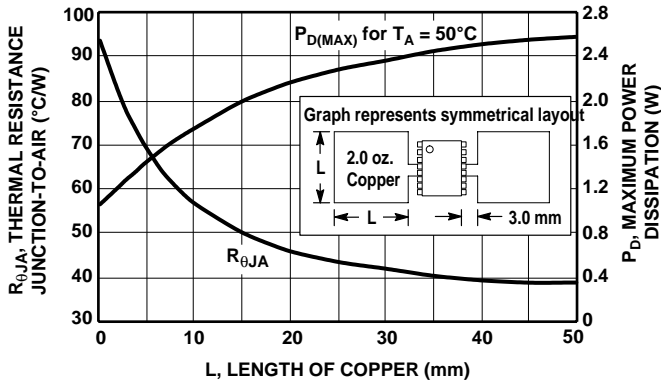
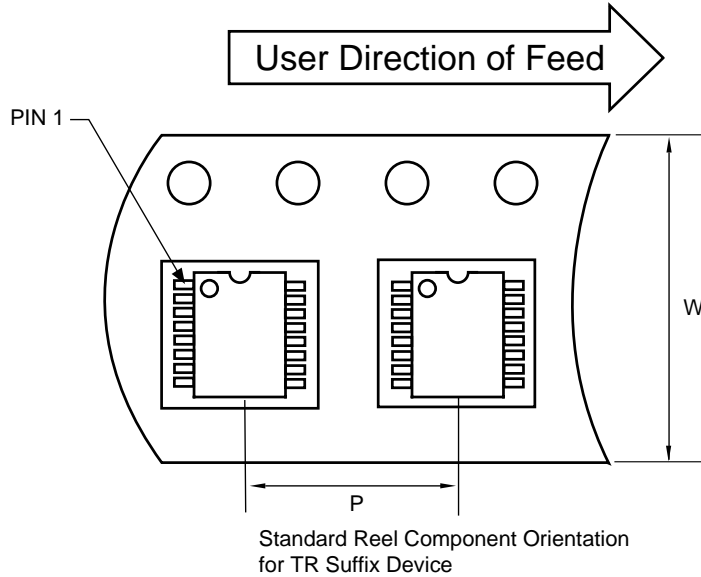


Figure 27. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



TAPE AND REEL SPECIFICATIONS

Component Taping Orientation for 16-Pin SOIC (Wide) Devices



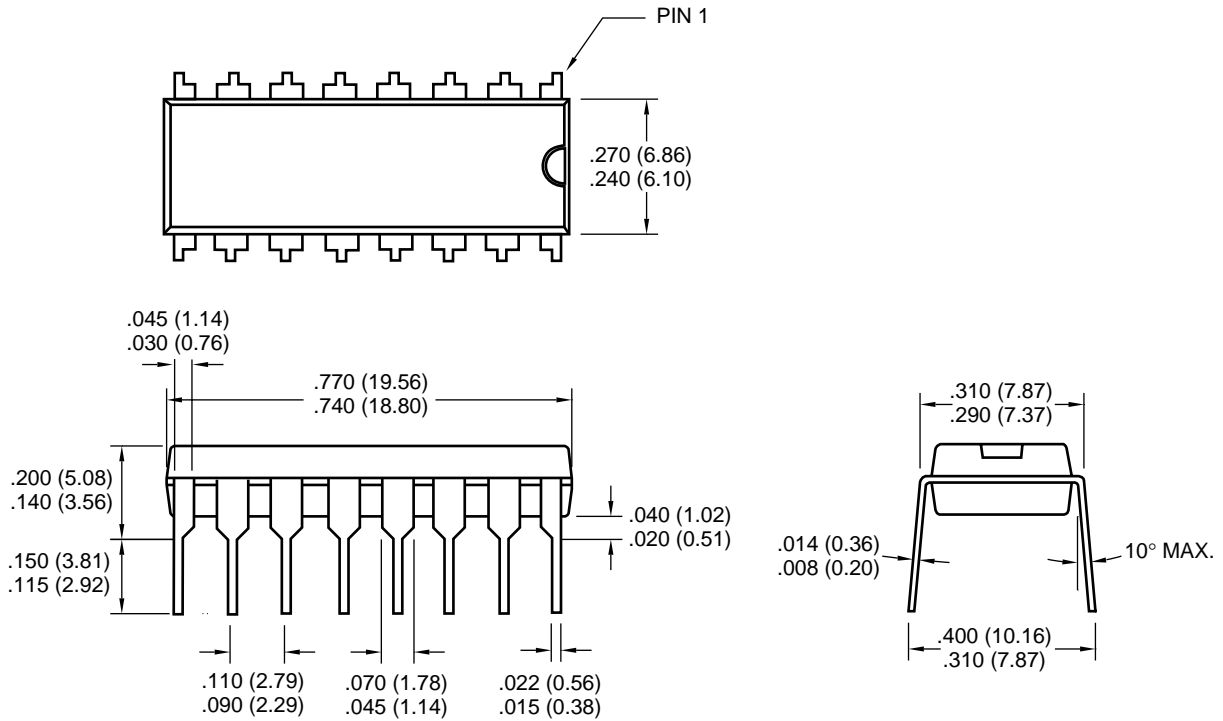
Carrier Tape, Reel Size, and Number of Components Per Reel

| Package | Carrier Width (W) | Pitch (P) | Part Per Full Reel | Reel Size |
|-----------------|-------------------|-----------|--------------------|-----------|
| 16-Pin SOIC (W) | 16 mm | 12 mm | 1000 | 13 in |

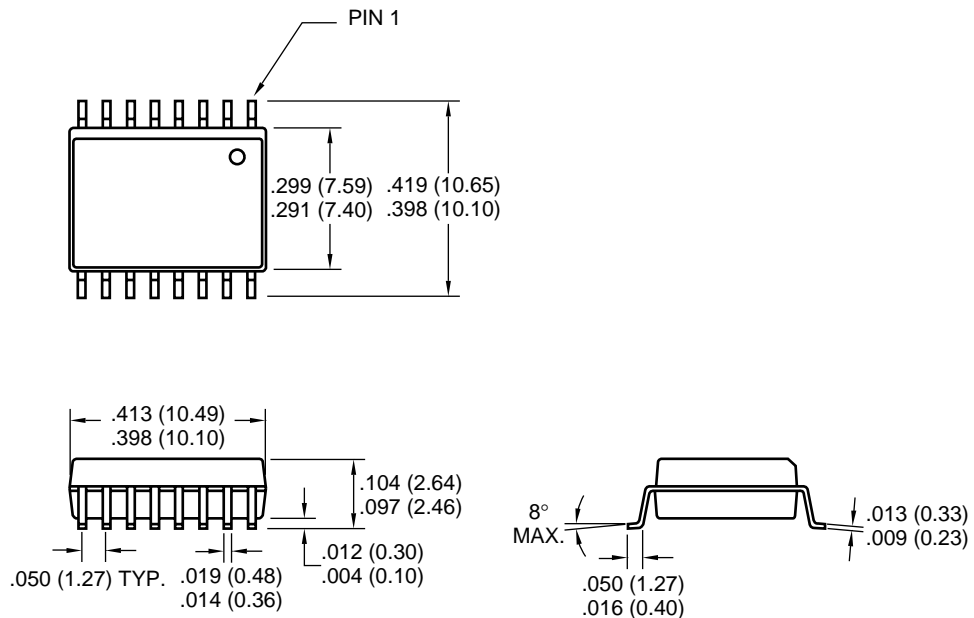
TC33163

PACKAGE DIMENSIONS

16-Pin PDIP (Narrow)



16-Pin SOIC (Wide)



Dimensions: inches (mm)

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