HARRIS SEMICONDUCTOR

HM-6504/883

March 1997

4096 x 1 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby . . . . . 125µW Max**
- **Low Power Operation . . . . . 35mW/MHz Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time. . . . . 120/200ns Max**
- **18 Pin Package for High Density**
- **On-Chip Address Register**
- **Gated Inputs - No Pull Up or Pull Down Resistors Required**

Description

The HM-6504/883 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminate the need for pull up or pull down resistors. The HM-6504/883 is a fully static RAM and may be maintained in any state for an indefinite period of time.

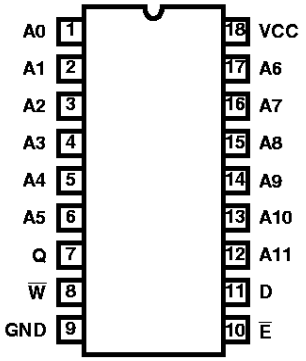
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	200ns	300ns	PKG. NO
CERDIP	-55°C to +125°C	HM1-6504B/883	HM1-6504/883	F18.3

Pinout

HM-6504/883 (CERDIP)
TOP VIEW

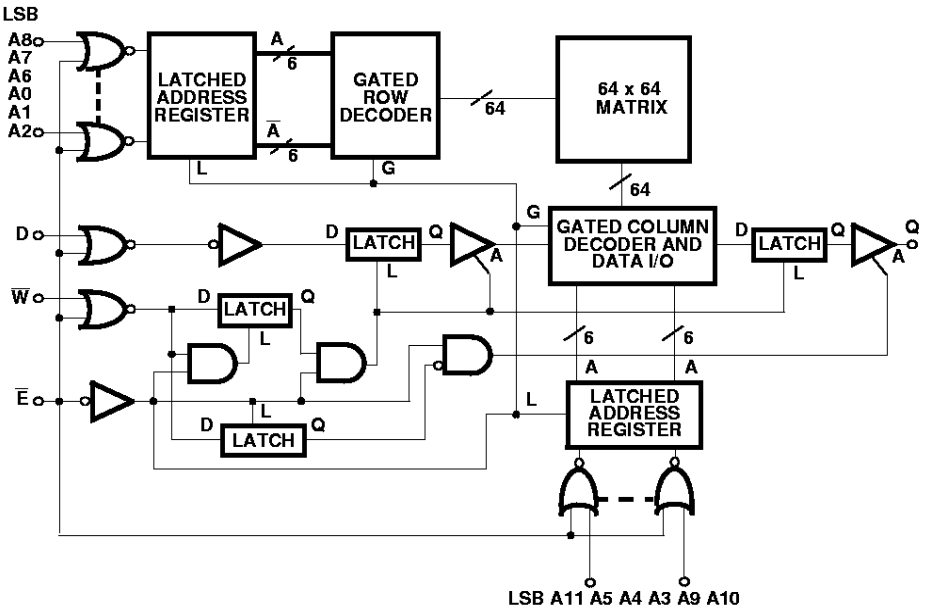


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2993.1**

Functional Diagram



NOTES:

1. All lines active high-positive logic.
2. Three-state Buffers: A high $\rightarrow$ output active.
3. Control and Data Latches: L low $\rightarrow$ Q = D and Q latches on rising edge of L.
4. Address Latches: Latch on falling edge of $\overline{E}$.
5. Gated Decoders: Gate on rising edge of G.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	75°C/W	15°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . -0.3V to +0.8V
Input High Voltage . . . . . VCC -2.0V to VCC +0.3V

TABLE 1. HM-6504/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 2mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -1.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
Output Leakage Current	IOZ	VCC = 5.5V, VO = GND or VCC	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.0V, $\overline{E}$ = VCC -0.3V, IO = 0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	50	µA

NOTES:

1. All voltage referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6504/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-6504S/883		HM-6504B/883		HM-6504/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	220	-	320	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	90	-	120	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	20	-	20	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	50	-	ns
Write Enable Pulse Width	(9) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	60	-	80	-	ns
Write Enable Pulse Setup Time	(10) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	150	-	200	-	ns
Early Write Pulse Setup Time	(11) TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Early Write Pulse Hold Time	(13) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	60	-	80	-	ns
Data Setup Time	(14) TDVWL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Early Write Data Setup Time	(15) TDVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Data Hold Time	(16) TWLDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	60	-	80	-	ns
Early Write Data Hold Time	(17) TELDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	60	-	80	-	ns
Read or Write Cycle Time	(18) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	170	-	290	-	420	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6504/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	HM-6504S/883 LIMITS MIN	HM-6504S/883 LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	8	pF
Output Capacitance	CO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	T_A = +25°C	-	10	pF
Chip Enable Output Disable Time	(3) TELQX	VCC = 4.5 and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
Chip Enable Output Disable Time	(4) TEHQZ	VCC = 4.5 and 5.5V HM-6504S/883	1	-55°C ≤ T_A ≤ +125°C	-	50	ns
		VCC = 4.5 and 5.5V HM-6504B/883	1	-55°C ≤ T_A ≤ +125°C	-	80	ns
		VCC = 4.5 and 5.5V HM-6504/883	1	-55°C ≤ T_A ≤ +125°C	-	100	ns
Write Enable Read Mode Setup Time	(12) TWHEL	VCC = 4.5 and 5.5V	1	-55°C ≤ T_A ≤ +125°C	0	-	ns
High Level Output Voltage	VOHL	VCC = 4.5V, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VCC - 0.4	-	V

NOTE:

1. The parameters listed in Table 3 are controlled via design, or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

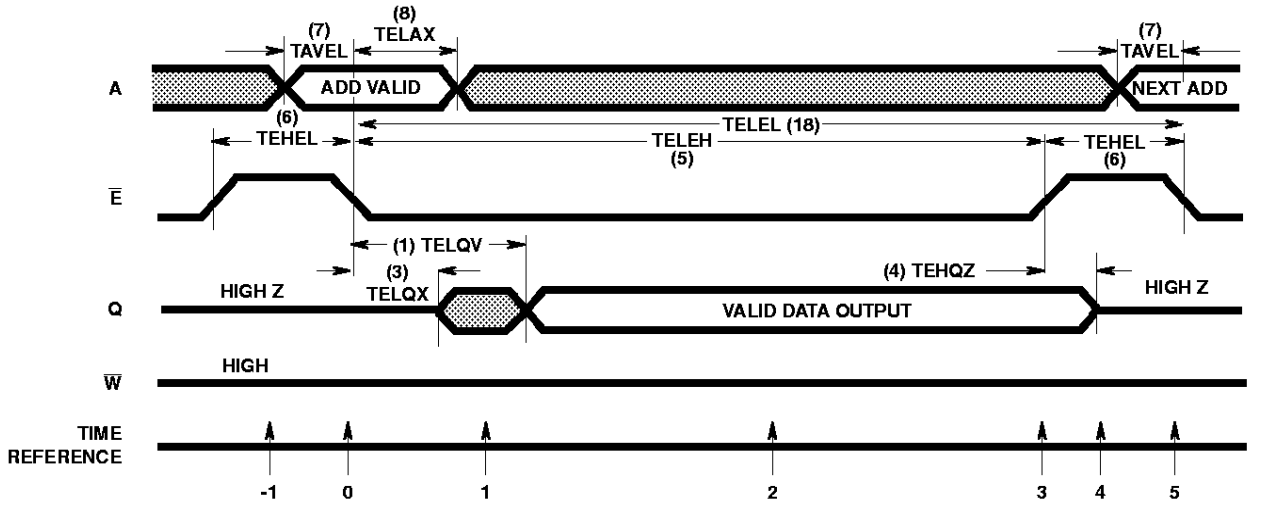


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	Q	
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all input, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

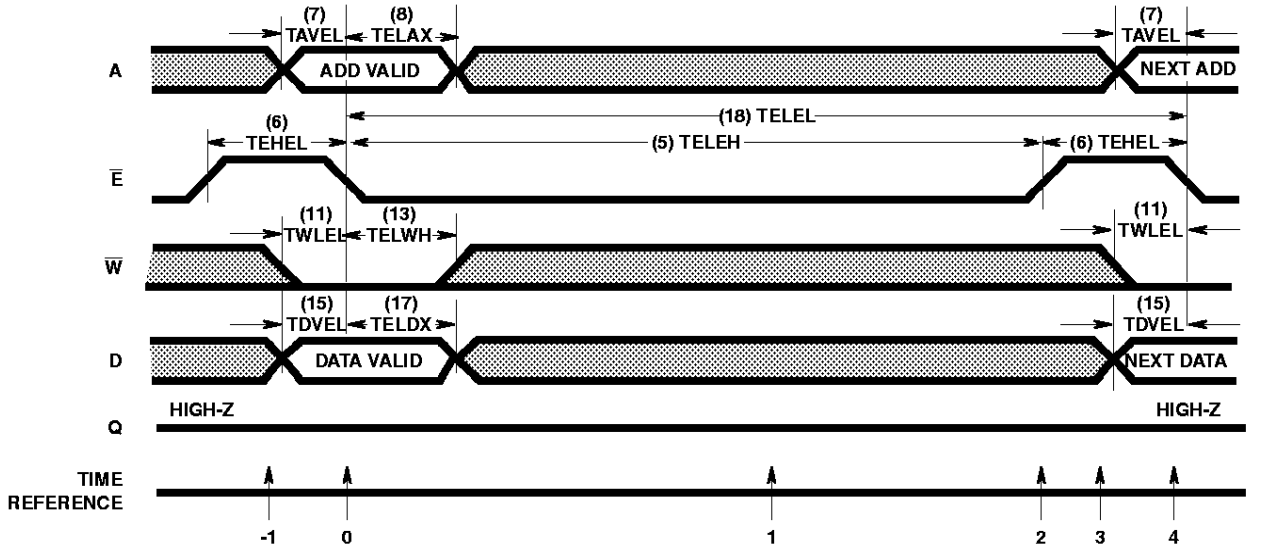


FIGURE 2. EARLY WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↗	X	X	X	Z	Write Completed
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↘	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on-chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore, data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state, the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Timing Waveforms (Continued)

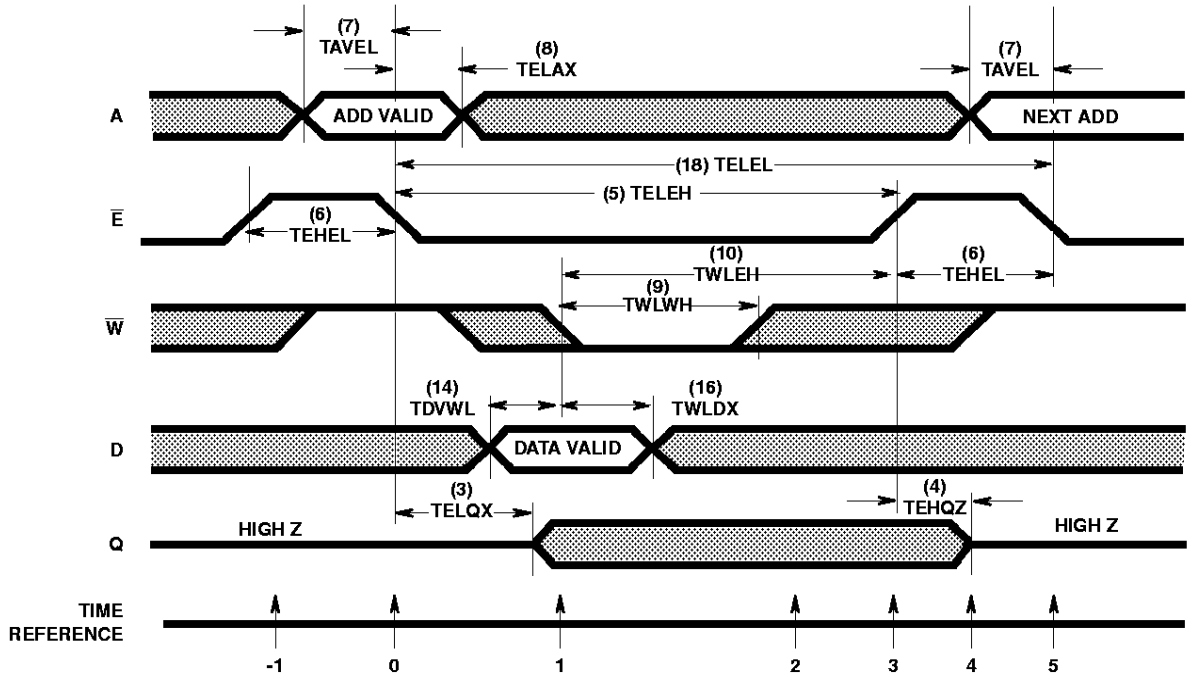


FIGURE 3. LATE WRITE CYCLE

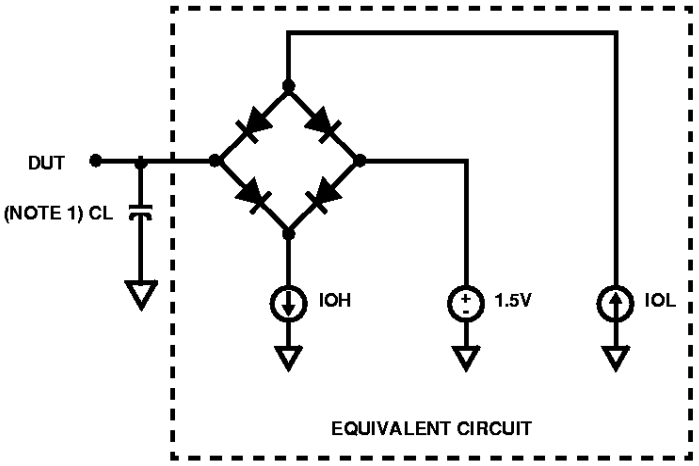
TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write In Progress Internally
3	↗	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write, the output is guaranteed to remain high impedance, and in the read-modify-write, the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

Test Load Circuit

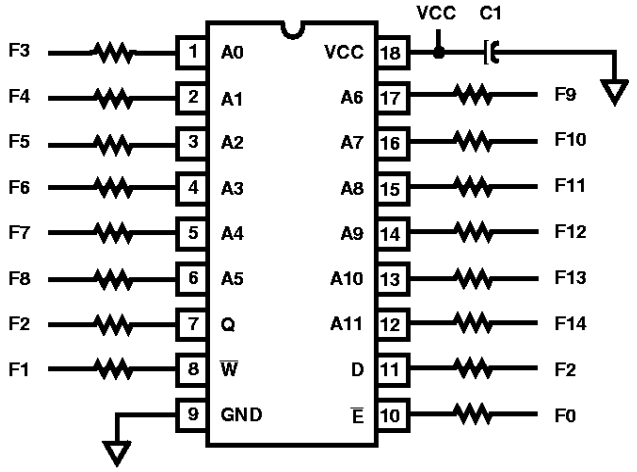


NOTE:

1. Test head capacitance includes stray and jig capacitance.

Burn-In Circuit

HM-6504/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 169 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

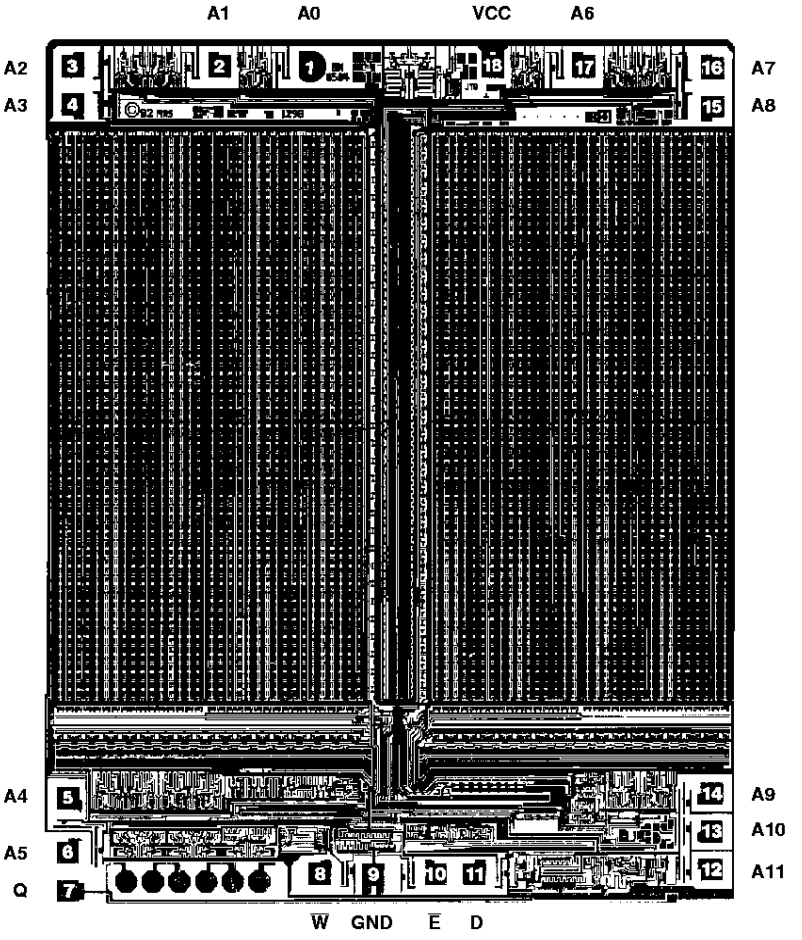
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.79 x 10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
≤ 300°C

Metallization Mask Layout

HM-6504/883



NOTE:

1. Pin numbers correspond to DIP Package only.