数据资料 December 2008 FN9124.4

改善的业界标准单端电流模式 PWM 控制器

可调频率、低电源、电流模式 PWM 控制器的系列：ISL6840, ISL6841, ISL6842、ISL6843、ISL6844 和 ISL6845 是设计用于大范围能量变换应用，包括升压、反馈和隔离输出的结构。峰值电流模式控制可有效地处理能量瞬变且有固有的过流保护。

这个先进的 BiCMOS 设计不但兼容了业界标准 384x 控制器系列的引脚，而且显著地改善了其性能。其特点包括低运作电流、60 μA 启动电流、可调工作频率高达 2MHz 和 20ns 升降时间的高峰值电流驱动力。

零件号码	上升欠压切断	最大占空比
ISL6840	7.0V	100%
ISL6841	7.0V	50%
ISL6842	14.4V	100%
ISL6843	8.4V	100%
ISL6844	14.4V	50%
ISL6845	8.4V	50%

主要特点

- 1A MOSFET 驱动器
- 60 μA 启动电流, 其峰值为 100 μA
- 控制到输出的延迟是 30ns
- 高峰值电流模式控制固有的快速瞬变反应
- 可调开关频率高达 2MHz
- 20ns 升降时间以 1nF 输出负载
- 平衡的定时电容的放电电流适合于精确死区时间/最大占空比控制
- 高带宽误差放大器
- 遍及输入、负载和温度范围的精密的容差电压基准
- 精密的容差电流门限值
- 不含 Pb 的包装

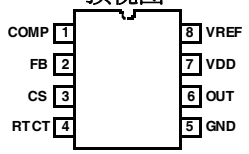
应用

- 电信和信息电源
- 无线基站电源
- 档案服务器电源
- 工业动力系统
- 个人计算机电源
- 隔离降压和反馈变换器
- 升压调节器

插脚引线

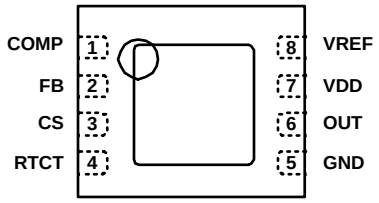
ISL6840, ISL6841, ISL6842, ISL6843, ISL6844, ISL6845
(8-PIN SOIC, MSOP)

顶视图



(8-PIN DFN)

顶视图



定购资料

零件号码	温度范围 (°C)	包装	包装图号 #
ISL6840IB	-40 to 105	8 Ld SOIC	M8.15
ISL6840IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6840IU	-40 to 105	8 Ld MSOP	M8.118
ISL6840IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6841IB	-40 to 105	8 Ld SOIC	M8.15
ISL6841IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6841IU	-40 to 105	8 Ld MSOP	M8.118
ISL6841IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6842IB	-40 to 105	8 Ld SOIC	M8.15
ISL6842IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6842IU	-40 to 105	8 Ld MSOP	M8.118
ISL6842IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6843IB	-40 to 105	8 Ld SOIC	M8.15
ISL6843IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6843IU	-40 to 105	8 Ld MSOP	M8.118
ISL6843IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6844IB	-40 to 105	8 Ld SOIC	M8.15
ISL6844IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6844IU	-40 to 105	8 Ld MSOP	M8.118
ISL6844IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6845IB	-40 to 105	8 Ld SOIC	M8.15
ISL6845IBZ (See Note)	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL6845IU	-40 to 105	8 Ld MSOP	M8.118
ISL6845IUZ (See Note)	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL6840IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6841IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6842IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6843IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6844IRZ-T* (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6845IRZ-T (See Note)	-40 to 105	8 Ld 2x3 DFN (Pb-free)	L8.2x3

Add -T to part number for Tape and Reel packaging

*Contact Factory for Availability

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

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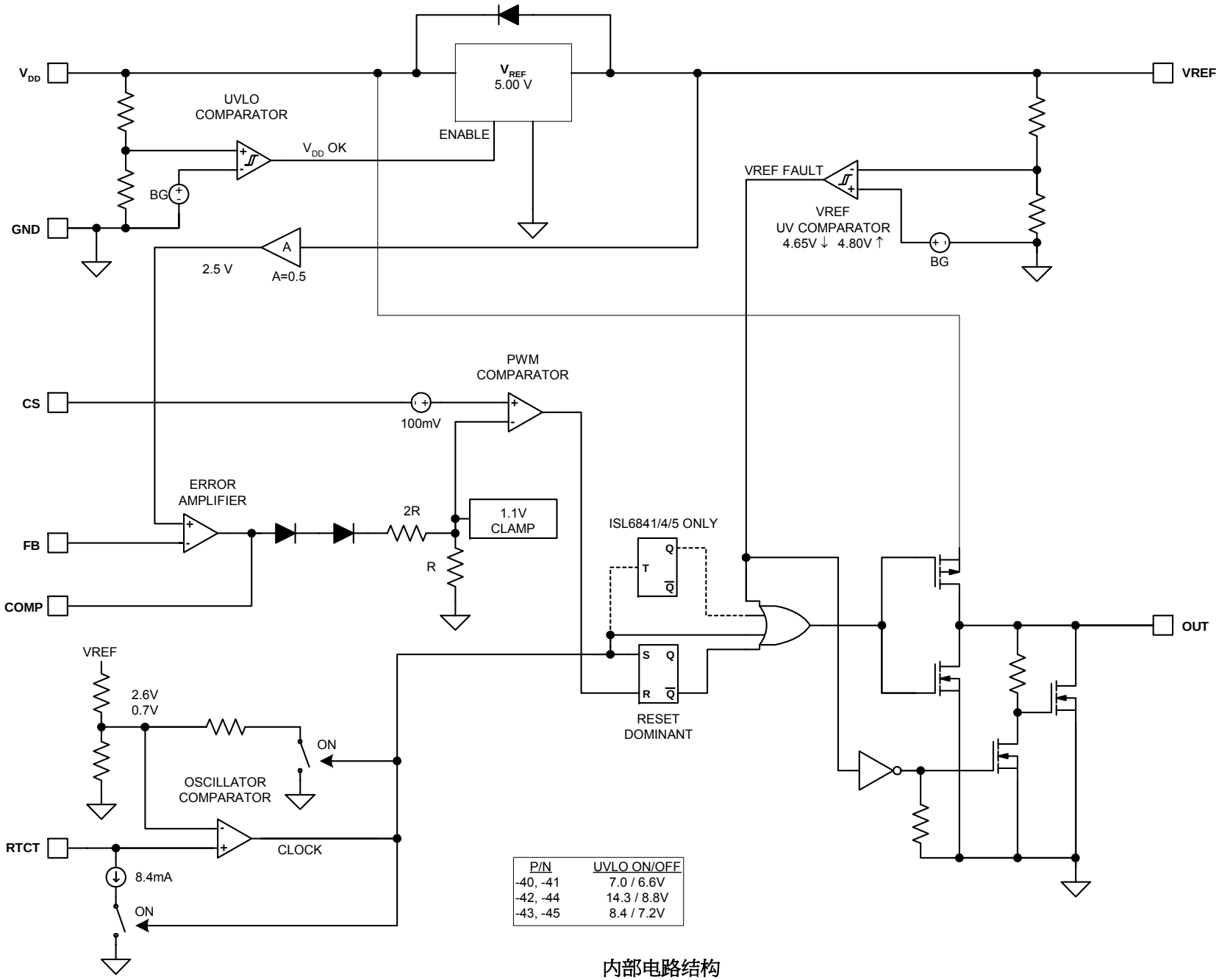
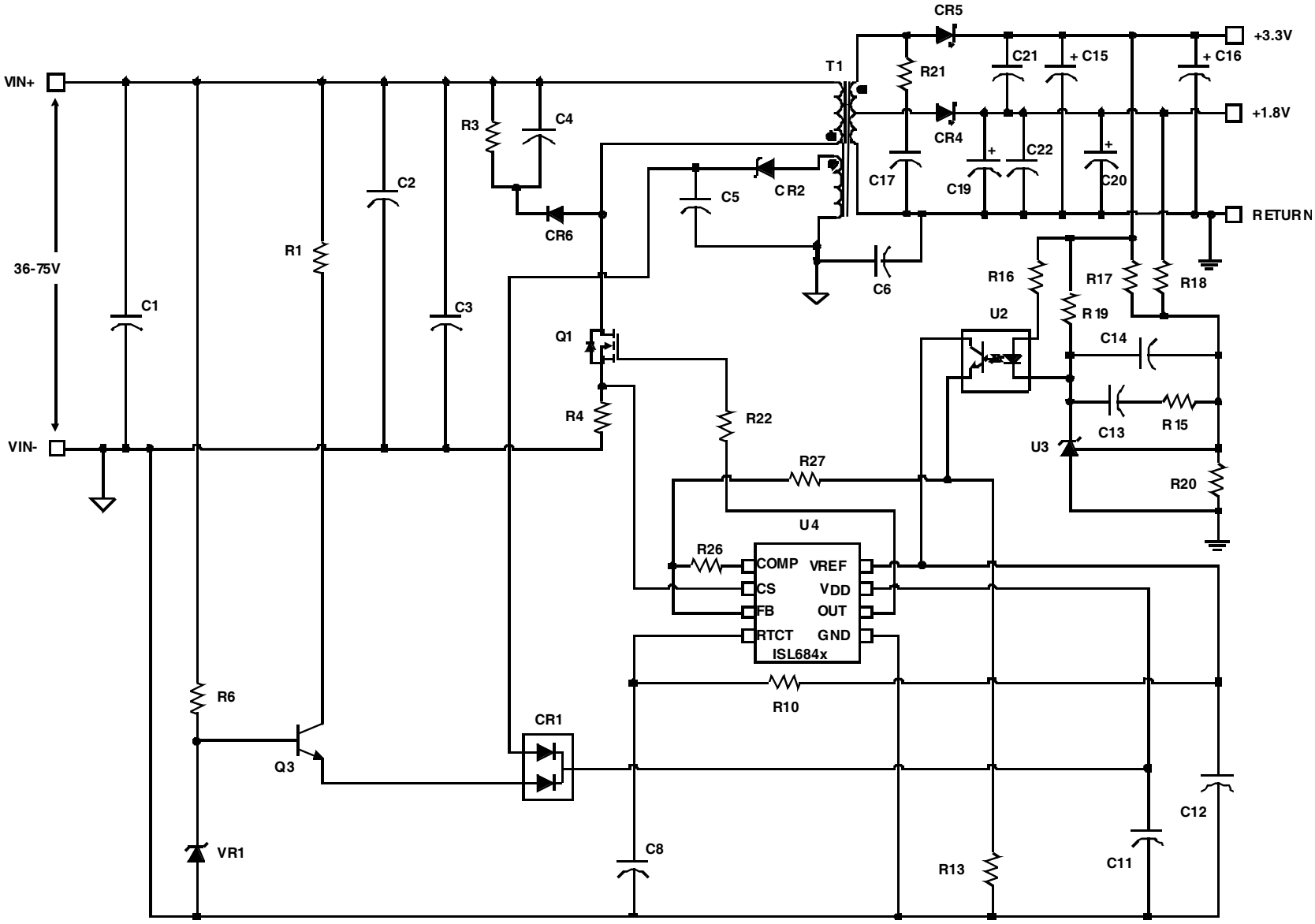


P/N	UVLO ON/OFF
-40, -41	7.0 / 6.6V
-42, -44	14.3 / 8.8V
-43, -45	8.4 / 7.2V

内部电路结构



典型应用: 48V 输入双输出反馈转换器

额定值

Supply Voltage, V_{DD} ----------GND-0.3V to +20V
OUT---------- GND - 0.3V to V_{DD} + 0.3V
Signal Pins----------GND-0.3V to 6.0V
Peak GATE Current ---------- 1A
ESD Classification
Human Body Model (Per MIL-STD-883 Method 3015.7) ---------- 2000V
Charged Device Model (Per EOS/ESD DS5.3, 4/14/93) ---------- 1000V

运行条件

Supply Voltage Range (Typical)
ISL6840/1 ---------- 7.5V-14VDC
ISL6843/5 ----------9-16VDC
ISL6842/4 ---------- 15V-18VDC
Temperature Range
ISL684xIx---------- -40°C to 105°C

热性能的资料

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
DFN Package (Note 2) ----------77 6
SOIC Package---------- 100 N/A
MSOP Package----------130 N/A
Maximum Junction Temperature ---------- -55°C to 150°C
Maximum Storage Temperature Range ---------- -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ---------- 300°C
(SOIC – Lead Tips Only)

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

Notes:

1) θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

2) For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

3) All voltages are to be measured with respect to GND, unless otherwise specified.

电气规范 Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application *Schematic.*

V_{DD} = 15V (Note 7), R_T = 10KΩ, C_T = 3.3nF, T_A = -40°C to 105°C (Note 4), Typical values are at T_A= 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold (ISL6840, ISL6841)		6.5	7.0	7.5	V
START Threshold (ISL6843, ISL6845)		7.8	8.4	9.0	V
START Threshold (ISL6842, ISL6844)		13.3	14.3	15.3	V
STOP Threshold (ISL6840, ISL6841)		6.1	6.6	6.9	V
STOP Threshold (ISL6843, ISL6845)		6.7	7.2	7.7	
STOP Threshold (ISL6842, ISL6844)		8.0	8.8	9.6	V
Hysteresis (ISL6840, ISL6841)		-	0.4	-	V
Hysteresis (ISL6843, ISL6845)		-	0.8	-	V
Hysteresis (ISL6842, ISL6844)		-	5.4	-	V
Start-Up Current, I_{DD}	V_{DD} < START Threshold	-	60	100	µA
Operating Current, I_{DD}	(Note 5)	-	3.3	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	-	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temp	4.925	5.000	5.050	V
Long Term Stability	T_A = 125°C, 1000 hours (Note 6)	-	5	-	mV
Fault Voltage		4.40	4.65	4.85	V
VREF Good Voltage		4.60	4.80	VREF-0.05	V
Hysteresis		50	165	250	mV
Current Limit, Sourcing		-20	-	-	mA

Current Limit, Sinking		5	-	-	mA

电气规范 **Electrical Specifications** **Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application *Schematic.* V_{DD} = 15V (Note 6), R_T = 10KΩ, C_T = 3.3nF, T_A = -40°C to 105°C (Note 3), Typical values are at T_A= 25°C. (continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1	µA
CS Offset Voltage	V_{CS} = 0V (Note 6)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 6)	0.80	1.15	1.30	V
Input Signal, Maximum		0.91	0.97	1.03	V
Gain, $A_{CS} = DV_{COMP}/DV_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V (Note 6)	2.5	3	3.5	V/V
CS to OUT Delay	(Note 6)	-	25	40	nS
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 6)	60	90	-	dB
Unity Gain Bandwidth	(Note 6)	3.5	5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.475	2.500	2.525	V
FB Input Bias Current	V_{FB} = 0	-1.0	-0.2	1.0	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	1.0	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	-0.4	-	-	mA
COMP VOH	V_{FB} = 2.3V	4.80	-	VREF	V
COMP VOL	V_{FB} = 2.7V	0.4	-	1.0	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 6)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_J = 25°C	49	52	55	KHz
Frequency Variation with V_{DD}	T = 25°C (F_{18V} - F_{12V})/F_{12V}	-	0.2	1.0	%
Temperature Stability	(Note 6)	-	-	5	%
Amplitude, Peak to Peak		-	1.9	-	V
RTCT Discharge Voltage		-	0.7	-	V
Discharge Current	RTCT = 2.0V	7.2	8.4	9.5	mA
OUTPUT					
Gate VOH	V_{DD} - OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate VOL	OUT - GND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 6)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 6)	-	20	40	nS
Fall Time	C_{OUT} = 1nF (Note 6)	-	20	40	nS
PWM					
Maximum Duty Cycle	ISL6840, ISL6842, ISL6843	94	96	-	%
	ISL6841, ISL6844, ISL6845	47	48	-	%

电气规范

Electrical Specifications **Recommended Operating Conditions, Unless Otherwise Noted. Refer to Block Diagram and Typical Application *Schematic.* V_{DD} = 15V (Note 6), R_T = 10KΩ, C_T = 3.3nF, T_A = -40°C to 105°C (Note 3), Typical values are at T_A= 25°C. (continued)**

Minimum Duty Cycle	ISL6840, ISL6842, ISL6843	-	-	0	%
	ISL6841, ISL6844, ISL6845	-	-	0	%

Notes:

4. Specifications at -40°C are guaranteed by design, not production tested.

5. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.

6. Guaranteed by design, not 100% tested in production.

7. Adjust V_{DD} above the start threshold and then lower to 15V.

典型性能曲线图

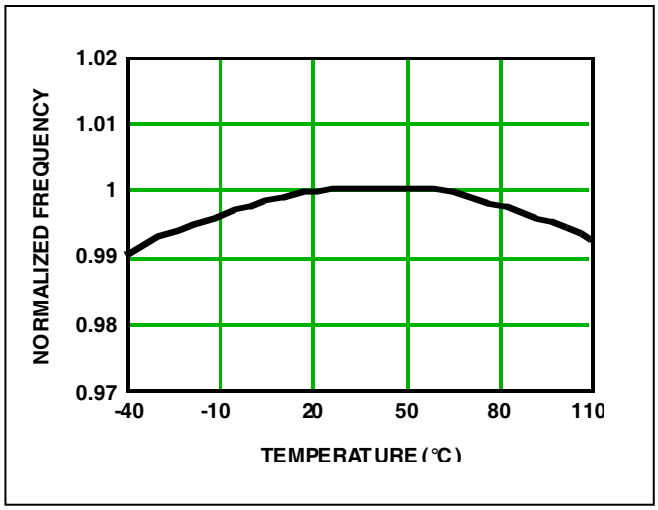


FIGURE 1. FREQUENCY vs TEMPERATURE

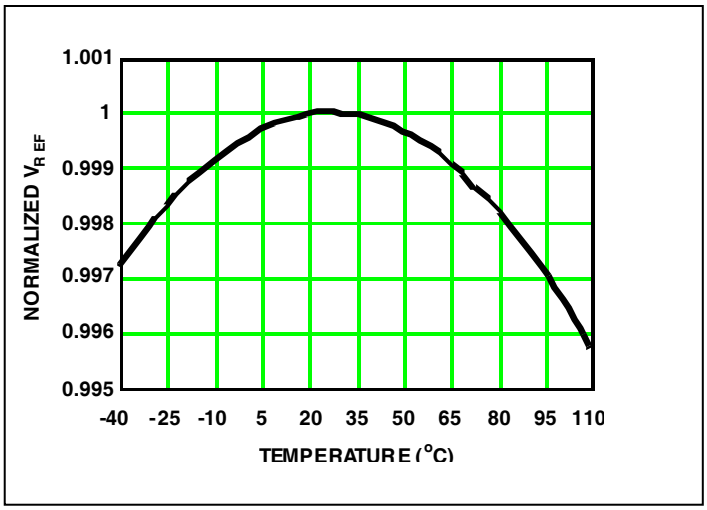


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

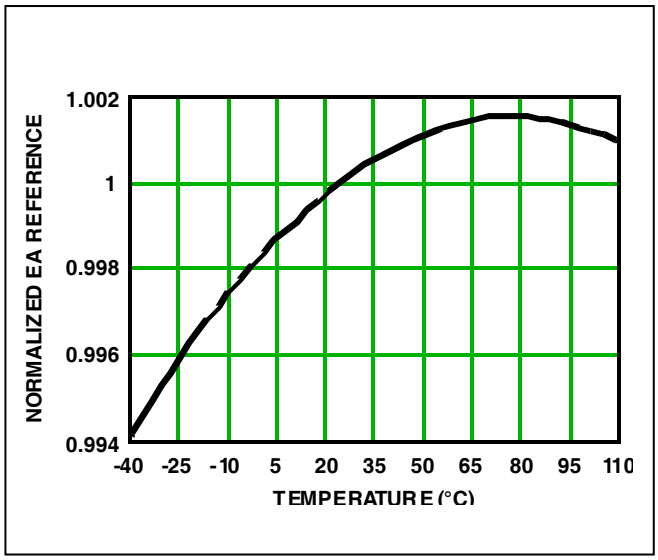


FIGURE 3. EA REFERENCE vs TEMPERATURE

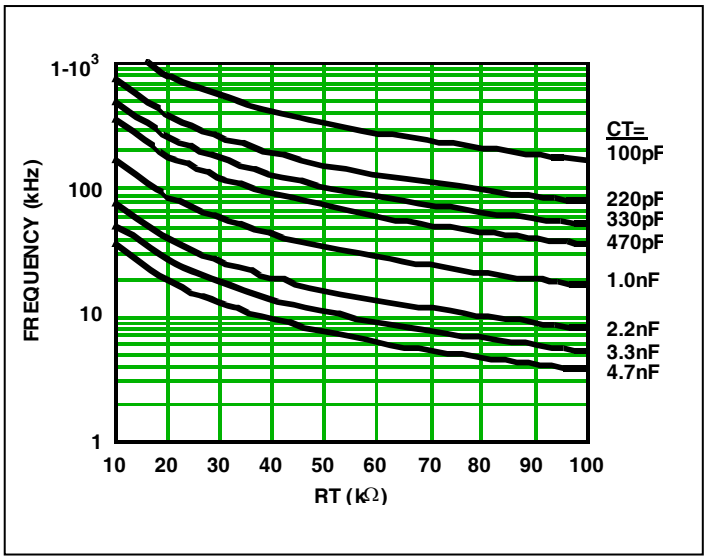


FIGURE 4. RTCT vs FREQUENCY

各管脚简介

RTCT

这是振荡器定时控制引脚。由这引脚间连接一电阻(R_T)到V_{REF}与和一定时电容(C_T)到 GND 之间可设置工作频率和最大占空比。振荡器产生一个可调频率高达 2.0MHz 的锯齿波。充电时间（T_C)、 放电时间（T_D）、 开关频率（f）和最大占空比（D_{max}）可用以下等式计算:

$$T_C \approx 0.583 \bullet R_T \bullet C_T \quad \text{(EQ. 1)}$$

$$T_D \approx -R_T \bullet C_T \bullet \ln\left(\frac{0.0083 \bullet R_T - 4.3}{0.0083 \bullet R_T - 2.4}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(T_C + T_D) \quad \text{(EQ. 3)}$$

$$D\max = T_C \bullet f \quad \text{(EQ. 4)}$$

在选择电容和电阻值所需指定的频率时，可用图4作为指南.

COMP

COMP 是误差放大器的输出端和 PWM 比较器的输入端。控制环频率补偿网络应连接在 COMP 和 FB 引脚之间。

FB

通过这个引脚输出电压的反馈连接到误差放大器的倒相输入， 而误差放大器的正相输入连接于内部的基准电压。

CS

这是 PWM 比较器电流检测输入端。 输入信号的范围在典型值 0 到 1.0V，且有 100mV 内部偏压。

GND

器件上所有功能和电源地都以这个引脚为基准。

OUT

这是电源开关元件的驱动输出端。它具有 1.0A 峰值电流驱动 MOSFET 门极。当 VDD 低于 UVLO 门限值时，门极输出就会降低。

VDD

VDD 是电源输入端。总供应电流取决于 OUT 输出负载，而总 IDD 电流是工作电流和平均输出电流之和。平均输出电流与工作频率（f）和 MOSFET 门极电荷（Qg）成正比，可用以下公式计算：

$$I_{OUT} = Q_g \bullet f \quad \text{(EQ. 5)}$$

要优化抗扰度，用一个陶瓷电容器尽可能靠近并挎接在 V_{DD} 和 GND 引脚。

VREF

这是 5.00V 的基准电压输出端，且有+1.0/-1.5%的容差遍及输入、负载和温度范围。可连接 0.1µF 至 3.3µF 的电容至 GND 以作滤波这输出所需。

功能概述

主要特点

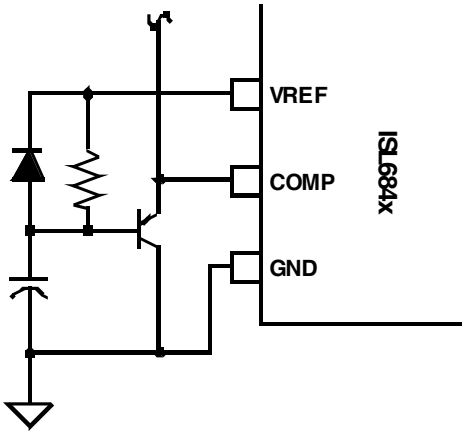
ISL684x 电流模式 PWMs 为那些低成本反激式和正激式拓扑结构的应用提供了一个理想的选择。因为其改善性能的远胜过于业界标准零件, 所以 ISL684x 是新设计或更新现存设计的优先选择。

振荡器

ISL684x 控制器有一个可调频率高达 2MHz 的锯齿振荡器。在 RTCT 引脚连接一电阻至 VREF 和电容至 GND 可设置工作频率。 (电阻和电容所需的指定频率可参見图 4。)

软启动运作

软启动必须在外部实施。以一方法为例 說明如下,电压钳位在 COMP。



SOFT START

FIGURE 5. SOFT START

门极驱动器

ISL684x 可灌出和吸收1A 峰值电流。要限制峰值电流通過IC, 可放置一个外部电阻在IC的推拉输出(OUT引脚)和MOSFET 門极之間。而这个小串联电阻能阻尼由线组寄生电感和FET 的输入电容的共振所产生的振荡。

斜坡补尝

应用的最大占空比少于 50%时，斜坡补尝可提高抗扰度，尤其在负载较小时。 测试表明：要优化抗扰度则需用一定数量的斜坡补偿，一般約是 10% 全方位的电流反馈信号。 若应用的占空比大于 50% 时，则需用斜坡补偿来防止不稳定，而所需的最低量斜坡补偿是相当于电感下坡的一半。外加过量的斜坡补偿，会导致控制环路由电流模式控制转化为电压模式控制。

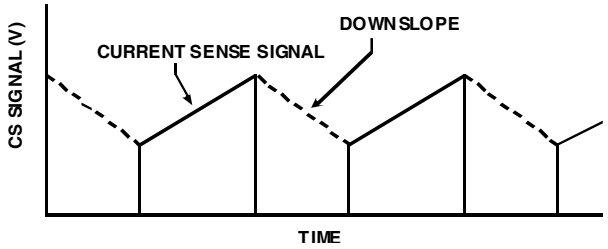


FIGURE 6. CURRENT SENSE DOWNSLOPE

用以下方式可增加傾斜补偿的 CS 信号:

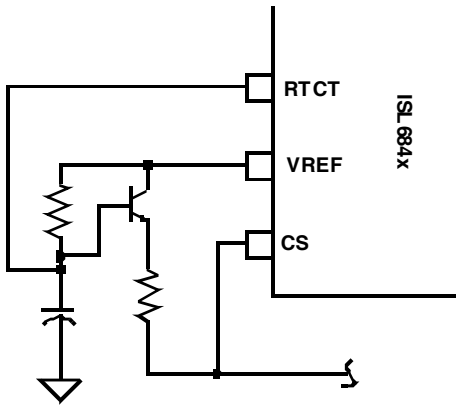


FIGURE 7. SLOPE COMPENSATION

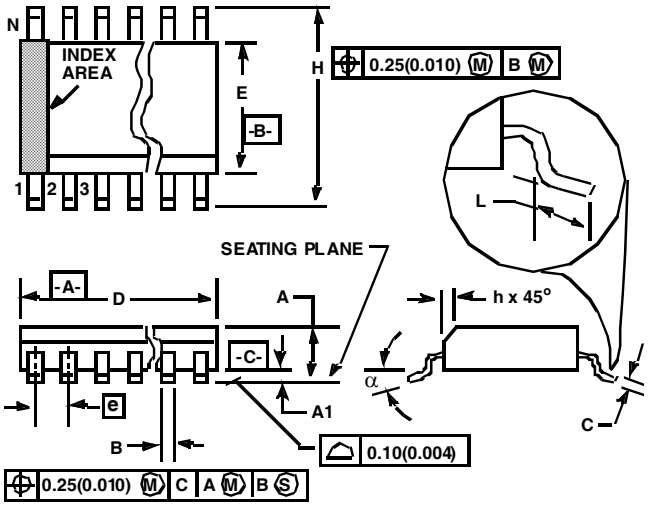
故障保护

VREF 跌落低于 4.65V 时会产生故障。当检测出故障时，OUT 输出就会被截止。VREF 超过 4.80V 时，则排除了故障，且 OUT 会重新输出。

接地面

为这个器件能理想操作，应要仔细布局，特别是应用一个好的接地面。其中独一部分的接地面必须设置为高的 di/dt 电流输出， 且VDD 必须以一个好的高频电容直接连接到地(GND)。

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions and are measured at Datum Plane. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

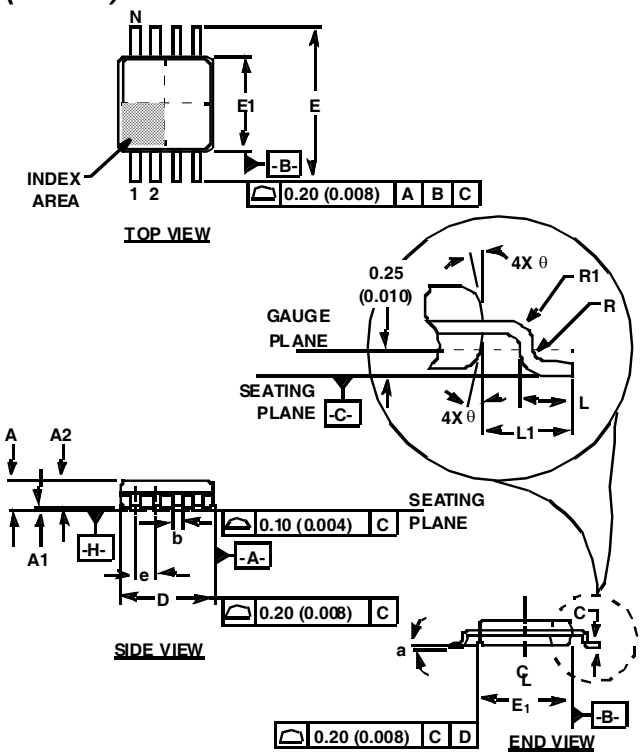
M8.15 (JEDEC MS-012-AA ISSUE C)

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^O	8^O	0^O	8^O	-

Rev.0 12/93

Mini Small Outline Plastic Packages (MSOP)



Notes:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane.Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums -A- and -B- to be determined at Datum plane -H-.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

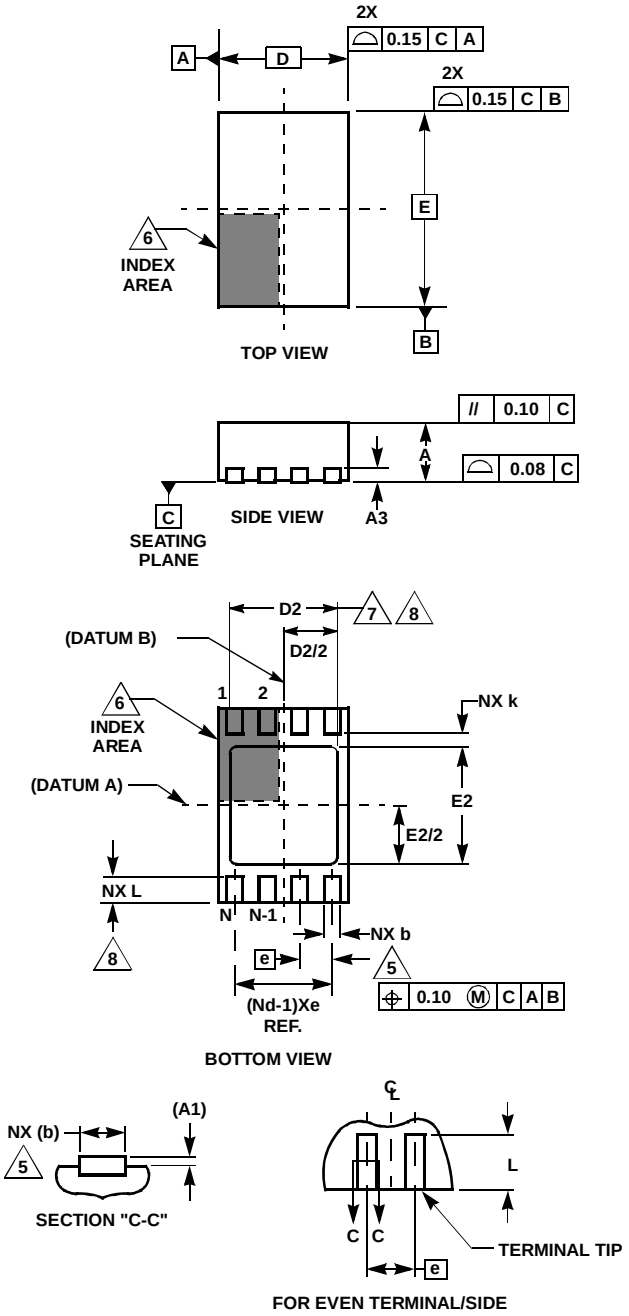
M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^{O}	15^{O}	5^{O}	15^{O}	-
α	0^{O}	6^{O}	0^{O}	6^{O}	-

Rev.2 01/03

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.