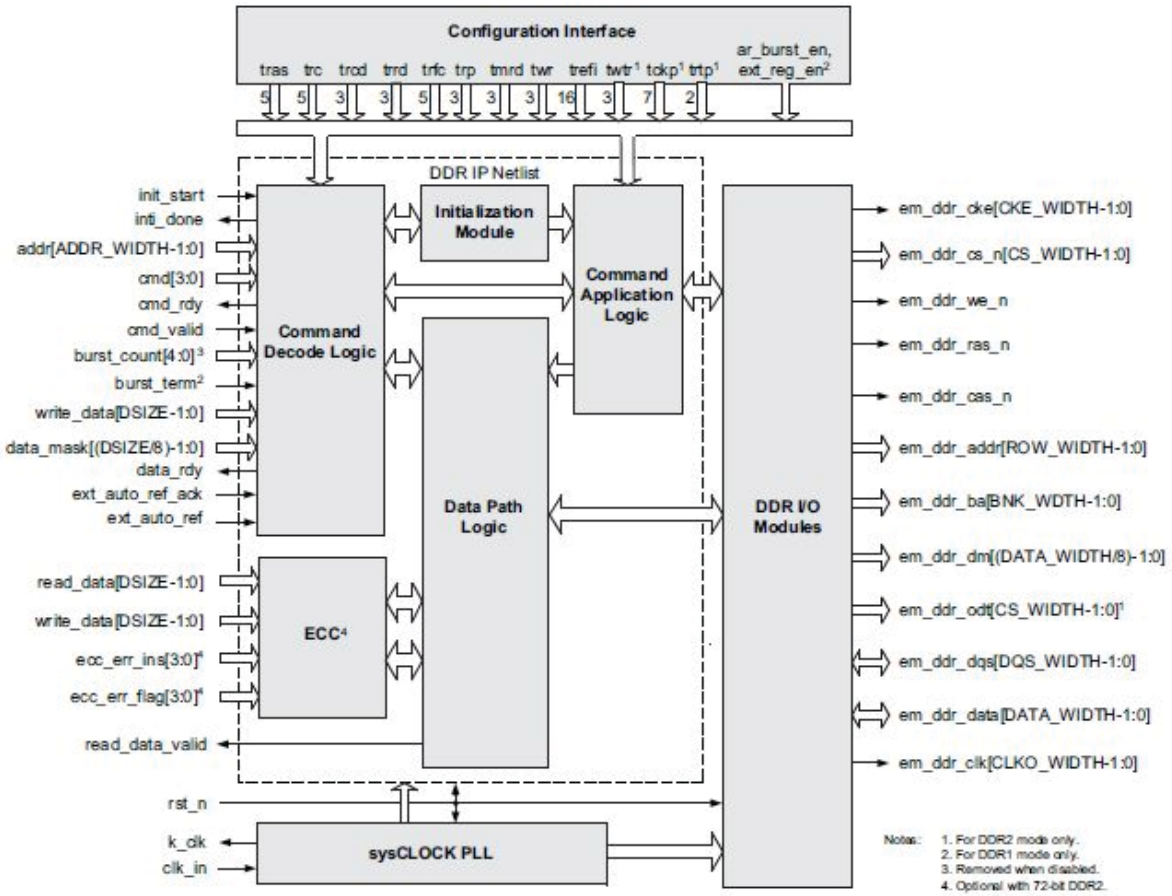
DDR2 SDRAM Controller - Pipelined

Overview

The Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) Controller is a general-purpose memory controller that interfaces with industry standard **DDR2 SDRAM**. The memory controller provides a generic command interface to the user's application. This interface reduces the effort to integrate the module with the remainder of the application and minimizes the need to deal with the DDR2 SDRAM command interface. The timing parameters for the memory can be set through the signals that are input to the core as part of the configuration interface. This enables switching between different memory devices and modification of timing parameters to suit the application using the same netlist.



Features

- Interfaces to Industry Standard DDR2 SDRAM
- High-Performance DDR2 533/400/333/266/200/133 operation
- Programmable Burst Lengths of 4 or 8
- Programmable CAS Latency of 3, 4, 5 or 6 Cycles
- Intelligent Bank Management to Minimize ACTIVE Commands
- Supports All Standard DDR Commands
- Synchronous Implementation for Reliable Operation
- Command Pipeline to Maximize Throughput
- Up to 4 chip selects for multiple DIMM support
- Supports all Common Memory Configurations

- SDRAM data path widths of 8, 16, 32, 64 and 72 bits
- Variable address widths for different memory devices
- Programmable timing parameters
- Byte level writing through Data Mask signals
- Burst termination

The DDR2 SDRAM Controller - Pipelined is available as an IPexpress user configurable IP core, which allows the configuration of the IP and generation of a netlist and simulation file for use in designs. Please note that generating a bitstream may be prevented or the bitstream may have time logic present unless a license for the IP is purchased.

Performance and Resource Utilization

LatticeECP3[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)[3]
User Guide Table 3-1 parameter defaults	1189	1386	1567	258	266 MHz (533 DDR2)

1. Performance and utilization characteristics are generated using LFE3-95E-8FN1156CES with Lattice ispLEVER 8.1 software in DDR2 mode. Performance may vary when using this IP core in a different density, speed or grade within the LatticeECP3 family.
2. SDRAM data path width of 32 bits.
3. The DDR2 IP core can operate at 266 MHz (533 DDR2) in the fastest speed-grade (-8) when the data width is 64 bits or less and 2 or fewer chip selects are used. For help with designs running at 266 MHz, contact your local sales office.

LatticeECP2M/S[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)[3]
User Guide Table 3-1 parameter defaults	1234	1435	1530	258	266 MHz (533 DDR2)

1. Performance and utilization characteristics are generated using LFECP2M-35E-6F672C with Lattice ispLEVER 8.1 software in DDR2 mode. Performance may vary when using this IP core in a different density, speed or grade within the LatticeECP2M/S family.
2. SDRAM data path width of 32 bits.
3. The DDR2 IP core can operate at 266 MHz (533 DDR2) in the fastest speed-grade (-7) when the data width is 64 bits or less and 2 or fewer chip selects are used. For help with designs running at 266 MHz, contact your local sales office.

LatticeECP2/S[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)[3]
User Guide Table 3-1 parameter defaults	1234	1435	1530	258	266 MHz (533 DDR2)

1. Performance and utilization characteristics are generated using LFECP2-50E-6F672C Lattice ispLEVER 8.1 software in DDR2 mode. Performance may vary when using this IP core in a different density, speed or grade within the LatticeECP2/S family.
2. SDRAM data path width of 32 bits.
3. The DDR2 IP core can operate at 266 MHz (533 DDR2) in the fastest speed-grade (-7) when the data width is 64 bits or less and 2 or fewer chip selects are used. For help with designs running at 266 MHz, contact your local sales office.

LatticeSC/M[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)
User Guide Table 3-1 parameter defaults	1261	1490	1530	246	266 MHz (533 DDR2)

1. Performance and utilization characteristics are generated using LFSC3GA25E-6F900C Lattice ispLEVER 8.1 software in DDR2 mode. Performance may vary when using this IP core in a different density, speed or grade within the LatticeSC/M family.
2. SDRAM data path width of 32 bits.

MachXO2[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)
User Guide Table 3-1 parameter defaults	704	1325	1118	152	133 MHz (266 DDR2)

8.1 software. Performance may vary when using this IP core in a different density, speed or grade within the MachXO2 family.
2. SDRAM data path width of 16 bits.

LatticeXP2[1]

Parameter Settings[2]	SLICEs	LUTs	Registers	I/O	f_{MAX} (MHz)
User Guide Table 3-1 parameter defaults	1232	1433	1530	258	200 MHz (400 DDR2)

1. Performance and utilization characteristics are generated using LFXP2-17E-6F484C Lattice ispLEVER 8.1 software in DDR2 mode. Performance may vary when using this IP core in a different density, speed or grade within the LatticeXP2 family.
2. SDRAM data path width of 32 bits.

Ordering Information

Family	Part Number
LatticeECP3	DDR2-P-E3-U6
LatticeECP2M/S	DDR2-P-PM-U6
LatticeECP2/S	DDR2-P-P2-U6
LatticeSC/M	DDR2-P-SC-U6
MachXO2	DDR2CTWB-M2-U
LatticeXP2	DDR2-P-X2-U6

IP Version: 7.2
Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.