HV9808

32-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs

Features

- 80V Maximum Output Voltage
- Low-Power Level Shifting
- 8 MHz Shift Register Speed
- Latched Data Outputs
- 5V CMOS-Compatible Inputs
- Forward and Reverse Shifting Options
- Diode to V_{PP} allows Efficient Power Recovery

Applications

- Piezoelectric Driver
- Inkjet Printer Driver
- Display Driver
- Microelectromechanical Systems Applications

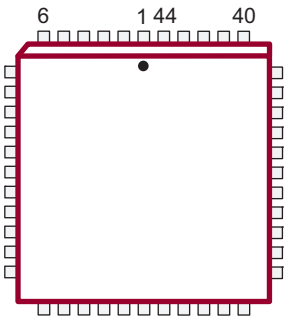
General Description

The HV9808 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. This device is designed as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple-output high-voltage low-current sourcing-and-sinking capabilities, such as driving plasma panels, vacuum fluorescent displays, and large matrix LCD displays. The inputs are fully CMOS compatible.

The device consists of a 32-bit Shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the Shift register through the polarity and blanking logic. Data is shifted through the Shift register on the low-to-high transition of the clock. The HV9808 shifts data counter-clockwise when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register, $HV_{OUT}32$. Operation of the Shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$), and polarity ($\overline{POL}$) inputs. Transfer of data from the Shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch is retained when $\overline{LE}$ is low.

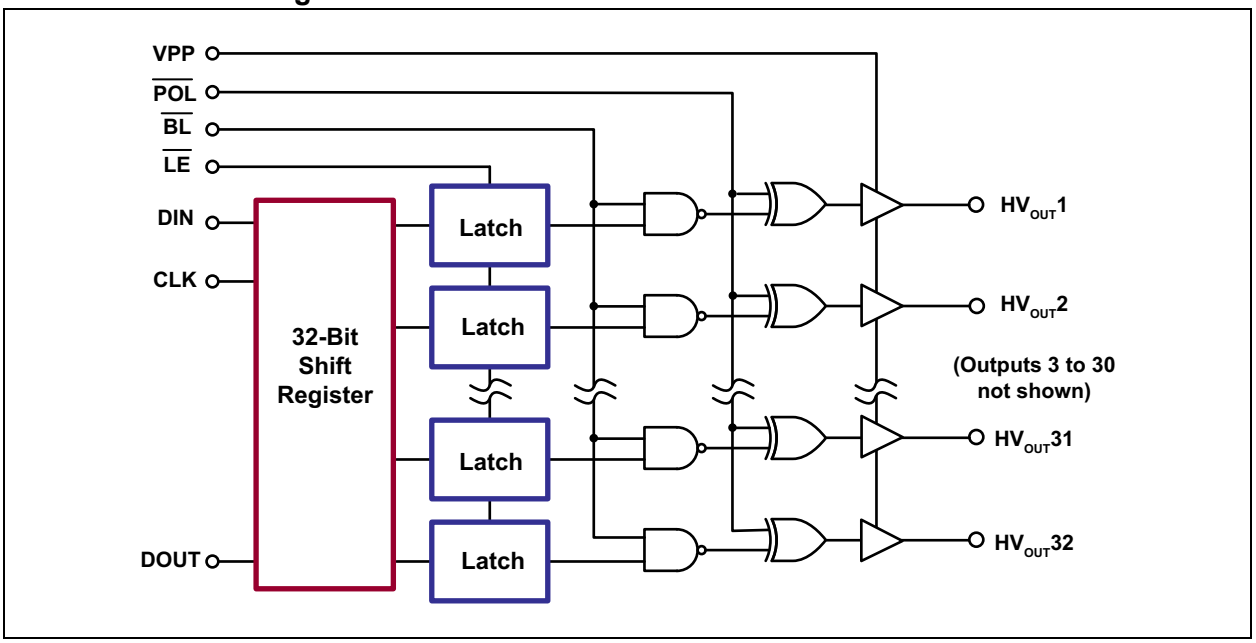
Package Type

44-lead PLCC
(Top view)

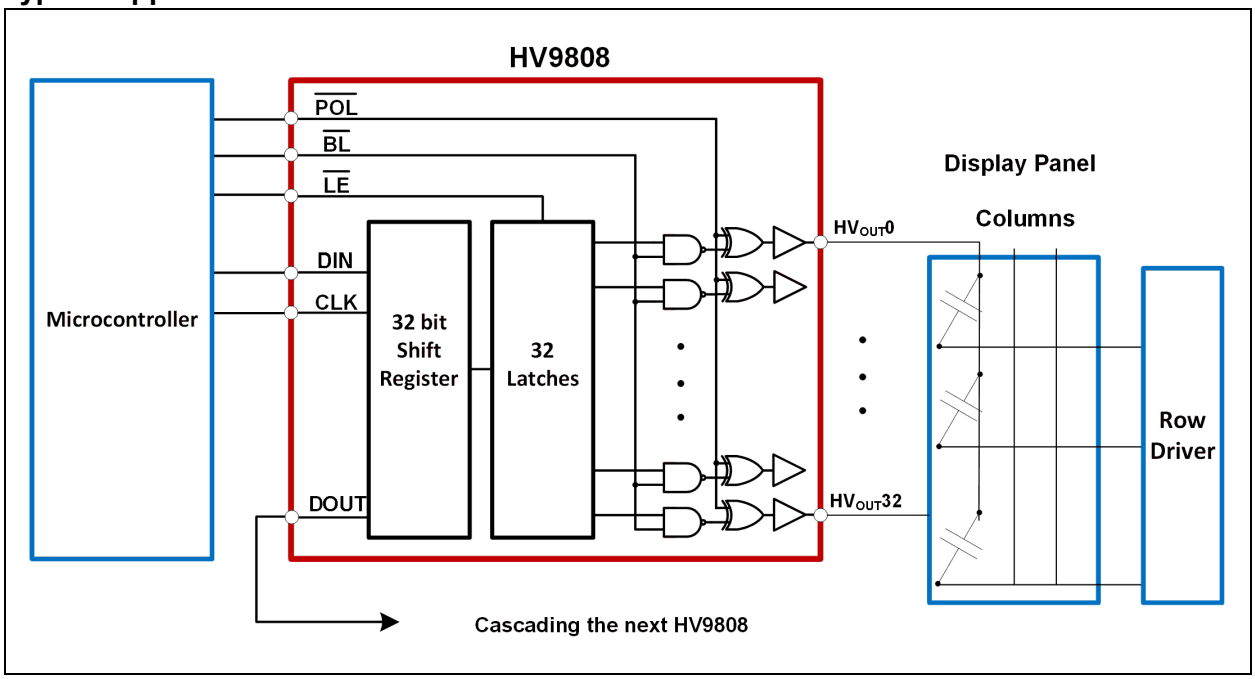


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} ..... –0.5V to +7V
Supply Voltage, V_{PP} ..... –0.5V to +90V
Logic Input Levels ..... –0.5V to V_{DD}+0.5V
Ground Current (**Note 1**) 1.5A
Operating Ambient Temperature, T_A ..... –40°C to +85°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
44-lead PLCC (**Note 2**) ..... 1200 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Duty cycle is limited by the total power dissipated in the package.
2: For operations above 25°C ambient, derate linearly to the maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High-Voltage Supply	V_{PP}	8	—	80	V	
High-Level Input Voltage	V_{IH}	V_{DD}–0.5	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.5	V	
Clock Frequency	f_{CLK}	—	—	8	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{PP} = 60V, V_{DD} = 5V, T_A = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{PP} Supply Current		I_{PP}	—	—	100	µA	HV_{OUT} high to low
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	100	µA	All V_{IN} = V_{DD} or GND
Operating V_{DD} Supply Current		I_{DD}	—	—	15	mA	V_{DD} = V_{DD} maximum, f_{CLK} = 8 MHz
High-Level Logic Input Current		I_{IH}	—	—	1	µA	V_{IN} = V_{DD}
Low-Level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IN} = GND
High-Level Output Voltage	HV_{OUT}	V_{OH}	52	—	—	V	I_O = –20 mA, 0°C to 70°C
	Data Out		V_{DD}–0.5	—	—	V	I_O = –100 µA
Low-Level Output Voltage	HV_{OUT}	V_{OL}	—	—	4	V	I_O = 5 mA, 0°C to 70°C
	Data Out		—	—	0.5	V	I_O = 100 µA
HV_{OUT} Clamp Diode Voltage		V_{OC}	—	—	–1.5	V	I_{OC} = –5 mA

AC ELECTRICAL CHARACTERISTICS

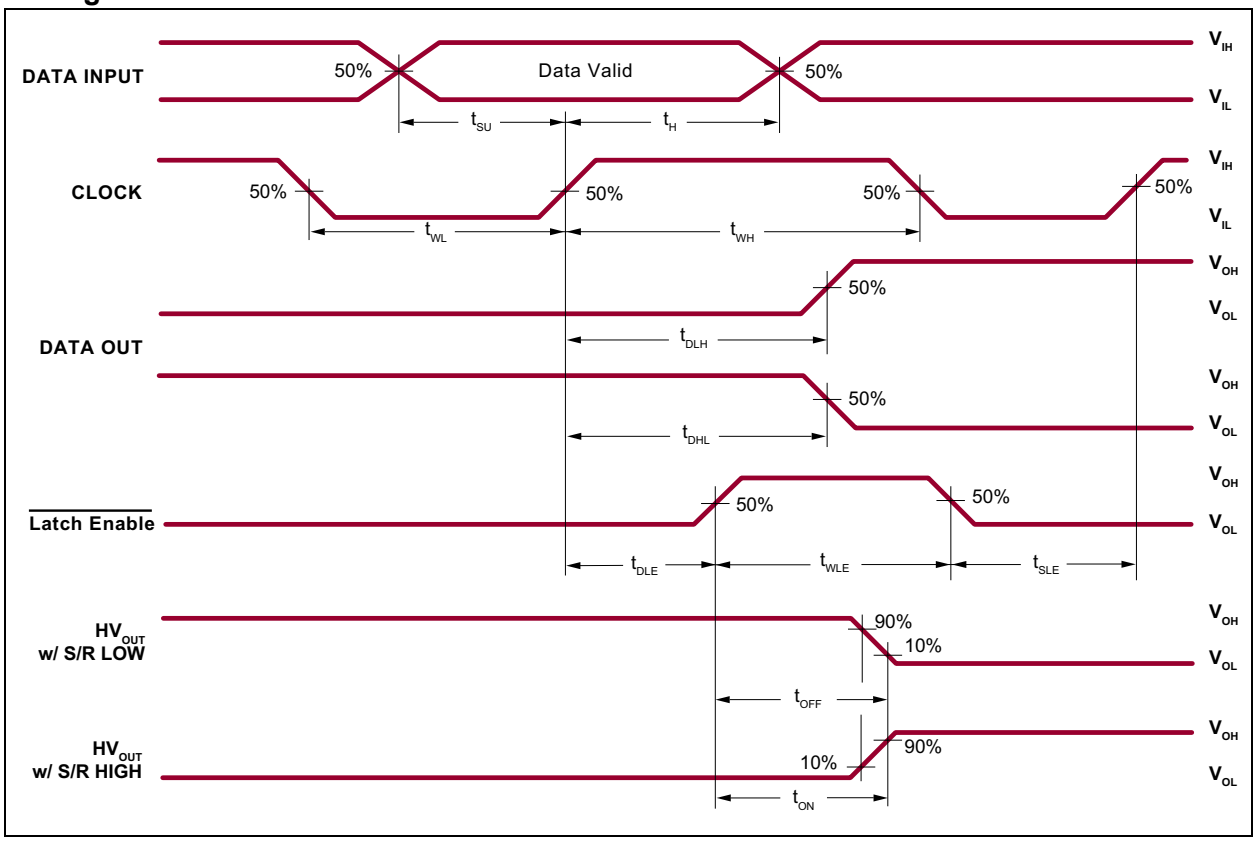
Electrical Specifications: V_{PP} = 60V, V_{DD} = 5V, T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	8	MHz	
Clock Width, High or Low	t_{WL}, t_{WH}	62	—	—	ns	
Data Set-Up Time before Clock Rises	t_{SU}	25	—	—	ns	
Data Hold Time after Clock Rises	t_H	10	—	—	ns	
Time from Latch Enable to HV_{OUT}	t_{ON}, t_{OFF}	—	—	500	ns	
Delay Time Clock to Data Low to High	t_{DLH}	—	—	110	ns	C_L = 15 pF
Delay Time Clock to Data High to Low	t_{DHL}	—	—	110	ns	C_L = 15 pF
Delay Time Clock to Latch Enable Low to High	t_{DLE}	50	—	—	ns	
Latch Enable Pulse Width	t_{WLE}	50	—	—	ns	
Latch Enable Set-Up Time before Clock Rises	t_{SLE}	50	—	—	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
44-lead PLCC	θ_{JA}	—	37	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV9808 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT16	High-voltage output
2	HVOUT17	High-voltage output
3	HVOUT18	High-voltage output
4	HVOUT19	High-voltage output
5	HVOUT20	High-voltage output
6	HVOUT21	High-voltage output
7	HVOUT22	High-voltage output
8	HVOUT23	High-voltage output
9	HVOUT24	High-voltage output
10	HVOUT25	High-voltage output
11	HVOUT26	High-voltage output
12	HVOUT27	High-voltage output
13	HVOUT28	High-voltage output
14	HVOUT29	High-voltage output
15	HVOUT30	High-voltage output
16	HVOUT31	High-voltage output
17	HVOUT32	High-voltage output
18	Data Out	Serial data output. Data output for cascading to the data input of the next device.
19	NC	No connection
20	NC	No connection
21	$\overline{\text{Polarity}}$	Polarity bar input logic
22	CLK	Data shift register clock. Inputs are shifted into the Shift register on the positive edge of the clock.
23	GND	Logic and high-voltage ground
24	VPP	High-voltage power rail
25	VDD	Low-voltage logic power rail
26	$\overline{\text{Latch Enable}}$	Latch enable input. When $\overline{\text{LE}}$ is high, Shift register data is transferred into a data latch. When $\overline{\text{LE}}$ is low, data is latched, and new data can be clocked into the Shift register.
27	Data In	Serial data input. Data needs to be present before each rising edge of the clock.
28	$\overline{\text{Blanking}}$	Blanking. A logic input low sets all HVOUTs low.
29	NC	No connection
30	HVOUT1	High-voltage output
31	HVOUT2	High-voltage output
32	HVOUT3	High-voltage output
33	HVOUT4	High-voltage output
34	HVOUT5	High-voltage output

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	HVOUT6	High-voltage output
36	HVOUT7	High-voltage output
37	HVOUT8	High-voltage output
38	HVOUT9	High-voltage output
39	HVOUT10	High-voltage output
40	HVOUT11	High-voltage output
41	HVOUT12	High-voltage output
42	HVOUT13	High-voltage output
43	HVOUT14	High-voltage output
44	HVOUT15	High-voltage output

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV9808.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove V_{PP}. (**Note 1**)
2	Apply V_{DD}.	2	Remove all inputs.
3	Set all inputs (Data, CLK, Enable, etc.) to a known state.	3	Remove V_{DD}.
4	Apply V_{PP}. (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} or float during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

Function	Inputs					Outputs				
						Shift Register		High-voltage Output		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...8	1	2...8	*
All On	X	X	X	L	L	*	*...*	H	H...H	*
All Off	X	X	X	L	H	*	*...*	L	L...L	*
Invert Mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*}$...$\overline{*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*...*	*	*...*	*
Load Latches	X	X	↑	H	H	*	*...*	*	*...*	*
	X	X	↑	H	L	*	*...*	$\overline{*}$	$\overline{*}$...$\overline{*}$	*
Transparent Latch Mode	L	↑	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	*...*	H	*...*	*

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↑ = Low-to-high transition
* = Dependent on the previous stage's state before the last CLK ↓ or last $\overline{LE}$ high

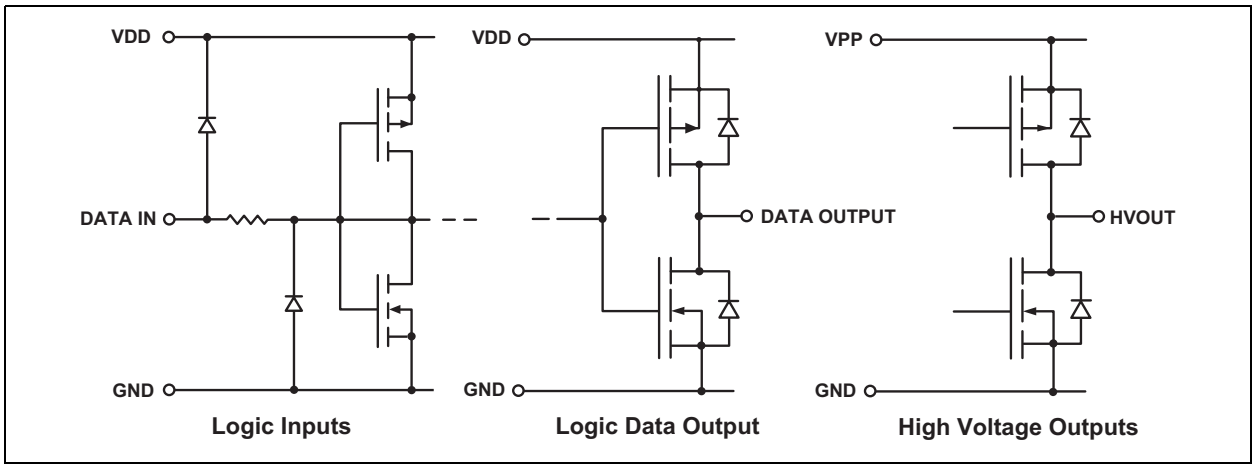
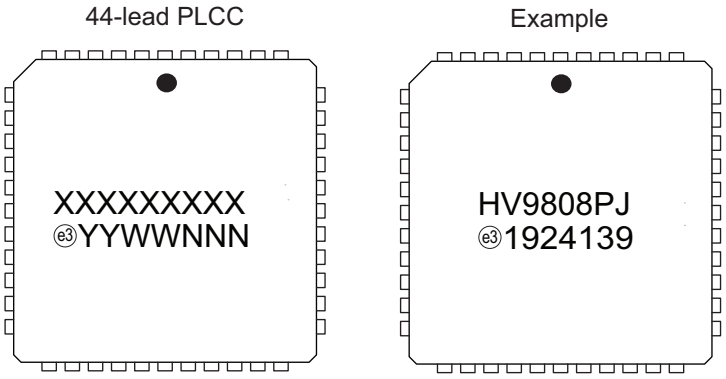


FIGURE 3-1: *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

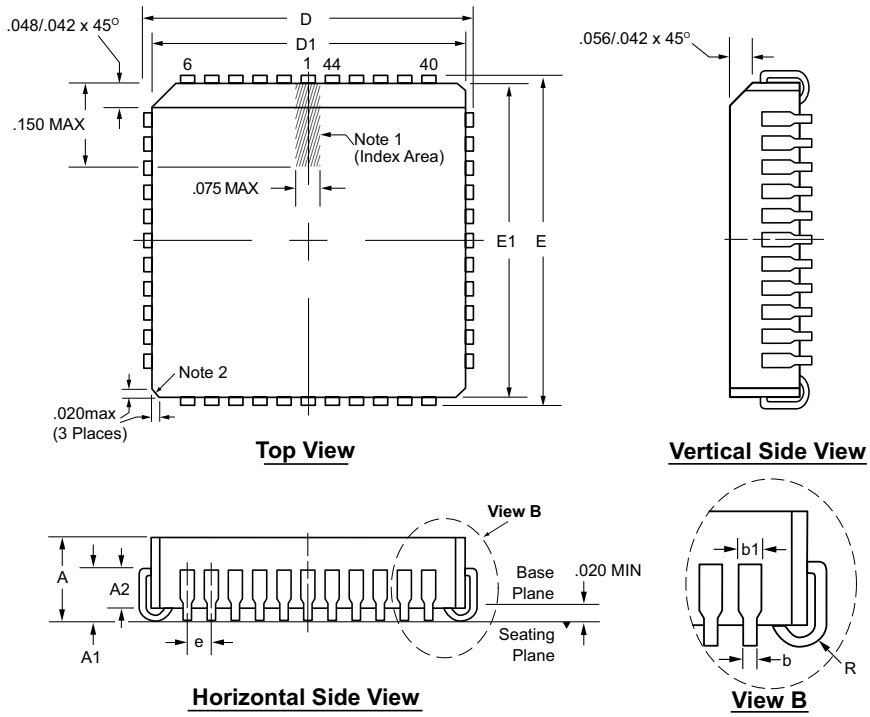
4.1 Packaging Information



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

44-Lead PLCC Package Outline (PJ)

.653x.653in body, .180in height (max), .050in pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2019)

- Converted Supertex Document # DSFP-HV9808 to DS20005914A
- Removed “Processed with HVCMOS® Technology” in the Features section
- Changed the package marking format
- Removed the 44-lead PLCC PJ M903 media type
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9808	=	32-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs
Package:	PJ	=	44-lead PLCC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	27/Tube for a PJ Package

Example:

a) HV9808PJ-G: 32-Channel Serial-to-Parallel Converter with High-Voltage Push-Pull Outputs, 44-lead PLCC, 27/Tube

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