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NTE74LS74A
Integrated Circuit
TTL, Dual D–Type Positive–Edge–Triggered Flip–Flop w/Preset and Clear

Description:

The NTE74LS74A contains two independent D–type positive–edge–triggered flip–flops in a 14–Lead DIP type package characterized for operating from 0° to +70°C. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive–going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Absolute Maximum Ratings: (T_A = 0° to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC} 7V
Input Voltage, V_{IN} 7V
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Voltage values are with respect to network GND terminal.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}		2	–	–	V
Low–Level Input Voltage	V_{IL}		–	–	0.8	V
High–Level Output Current	I_{OH}		–	–	–0.4	mA
Low–Level Output Current	I_{OL}		–	–	8	mA
Clock Frequency	f_{clock}		0	–	25	MHz
Pulse Duration CLK High	t_w		25	–	–	ns
$\overline{PRE}$ or $\overline{CLR}$ Low			25	–	–	ns
Setup Time Before CLK ↑	t_{su}		20	–	–	ns
Hold Time–Data After CLK ↑	t_h		5	–	–	ns
Operating Ambient Temperature	T_A		0	–	70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{I1} = −12mA		–	–	−1.5	V
Output High Voltage	V_{OH}	V_{CC} = Min, V_{IH} = 2V, V_{IL} = MAX, I_{0H} = -0.4mA		2.7	3.4	–	V
Output Low Voltage	V_{OL}	V_{CC} = Min, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	–	0.25	0.4	V
			I_{OL} = 8mA	–	0.35	0.5	V
Input Current D or CLK	I_I	V_{CC} = Max, V_I = 7V		–	–	0.1	mA
$\overline{CLR}$ or $\overline{PRE}$				–	–	0.2	mA
Input High Current D or CLK	I_{IH}	V_{CC} = Max, V_I = 2.7V		–	–	20	μA
$\overline{CLR}$ or $\overline{PRE}$				–	–	40	μA
Input Low Current D or CLK	I_{IL}	V_{CC} = Max, V_I = 0.4V		–	–	−0.4	mA
$\overline{CLR}$ or $\overline{PRE}$				–	–	−0.8	mA
Output Short Circuit Current	I_{OS}	V_{CC} = Max, Note 4, Note 5		−20	–	−100	mA
Power Supply Current	I_{CC}	V_{CC} = Max, Note 6		–	4	8	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Note 5. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.125V with the minimum and maximum limits reduced to one half of their stated values.

Note 6. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 2kΩ, C_L = 15pF	25	33	–	MHz
Propagation Delay Time (From $\overline{CLR}$, $\overline{PRE}$, or CLK Input to Q or $\overline{Q}$ Output)	t_{PLH}		–	13	25	ns
	t_{PHL}		–	25	40	ns

Function Table:

Inputs				Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 6)	H (Note 6)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Note 6. The output levels in this configuration are not guaranteed to meet the minimum levels in V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not presist when either preset or clear returns to its inactive (high) level.

Pin Connection Diagram