

August 1997

Monolithic CMOS Analog Switches

Features

- ON-Resistance <35Ω
- Low Power Consumption (P_D) <35μW
- Fast Switching Action
 - t_{ON} <150ns
 - t_{OFF} <100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI-5041
- DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051
- DG405 Dual DPST; DG184, HI-5045, IH5145
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- HI-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (<35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V_{p-p} signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Ordering Information

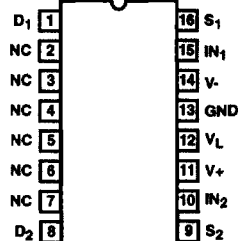
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG401AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG401DJ	-40 to 85	16 Ld PDIP	E16.3
DG401DY	-40 to 85	16 Ld SOIC	M16.15
DG401EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG401EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG403AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG403DJ	-40 to 85	16 Ld PDIP	E16.3
DG403DY	-40 to 85	16 Ld SOIC	M16.15
DG403EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG403EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15
DG405AK/883 (Note 2)	-55 to 125	16 Ld CERDIP	F16.3
DG405DJ	-40 to 85	16 Ld PDIP	E16.3
DG405DY	-40 to 85	16 Ld SOIC	M16.15
DG405EJ (Note 1)	-40 to 85	16 Ld PDIP	E16.3
DG405EY (Note 1)	-40 to 85	16 Ld SOIC	M16.15

NOTES:

1. Extended Processing Flow.
2. Refer to Military data sheet for complete specifications.

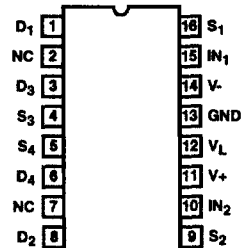
Pinouts

DG401 (CERDIP, PDIP, SOIC)
TOP VIEW



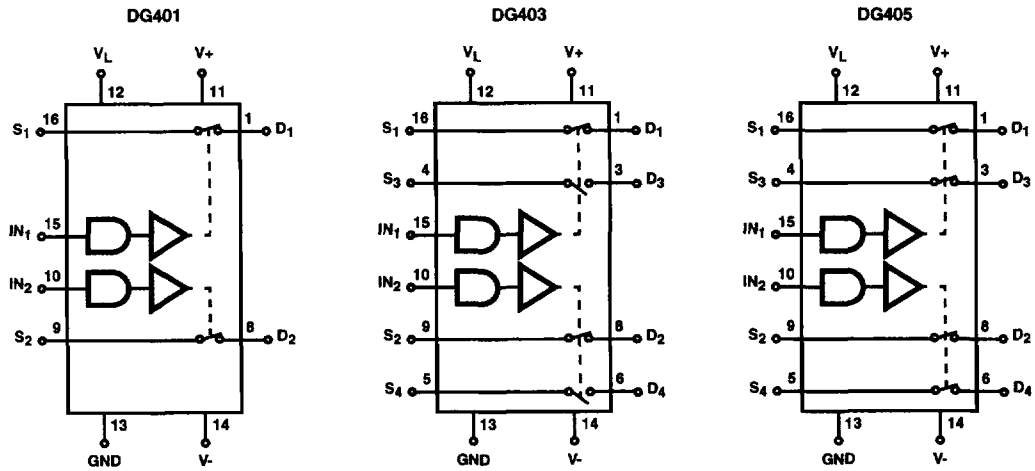
NOTE: (NC) No Connection

DG403, DG405 (CERDIP, PDIP, SOIC)
TOP VIEW

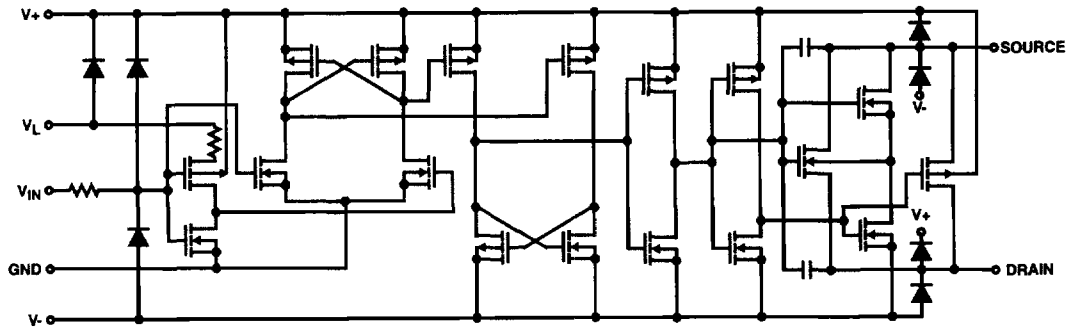


NOTE: (NC) No Connection

Functional Diagrams



Schematic Diagram



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" $\leq 0.8V$. Logic "1" $\geq 2.4V$.

DG401, DG403, DG405

Absolute Maximum Ratings

V+ to V-+44.0V
GND to V- 25V
V _L (GND - 0.3V) to (V _{C+}) +0.3V
Digital Inputs (Note 1), V _S , V _D (V-) -2V to (V+) + 2V or 30mA, Which ever Occurs First
Continuous (Any Terminal) Current, (Note 1) ±30mA
Peak Current, S or D (Note 1) (Pulsed 1ms, 10% Duty Cycle) ±100mA

Operating Conditions

Temperature (D and E Suffix)-40°C to 85°C
Voltage Range ±20V (Max)
Temperature Range-55°C to 125°C
Input Low Voltage 0.8V (Max)
Input High Voltage 2.4V (Min)
Input Rise and Fall Time 20ns

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3),
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C			UNITS
			(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t _{ON}	R _L = 300Ω, C _L = 35pF	Room	-	100	150	ns
Turn-OFF Time, t _{OFF}		Room	-	60	100	ns
Break-Before-Make, Time Delay (DG403), t _D	R _L = 300Ω, C _L = 35pF	Room	5	12	-	ns
Charge Injection, Q	C _L = 10,000pF, V _{GEN} = 0V, R _{GEN} = 0Ω	Room	-	60	-	pC
OFF Isolation Reject Ratio, OIRR	R _L = 100Ω, C _L = 5pF, f = 1MHz	Room	-	72	-	dB
Crosstalk (Channel-to-Channel), CCRR	R _L = 100Ω, C _L = 5pF, f = 1MHz	Room	-	90	-	dB
Source OFF Capacitance, C _{S(OFF)}	f = 1MHz, V _S = 0V	Room	-	12	-	pF
Drain OFF Capacitance, C _{D(OFF)}	f = 1MHz, V _S = 0V	Room	-	12	-	pF
Channel ON Capacitance, C _{D(ON)} + C _{S(ON)}	f = 1MHz, V _S = 0V	Room	-	39	-	pF
ANALOG SWITCH						
Analog Signal Range, V _{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, r _{DS(ON)}	V+ = 13.5V, V- = -13.5V, I _S = ±10mA, V _D = ±10V	Room	-	20	45	Ω
		Full	-	-	55	Ω
Drain-Source ON Resistance, Δr _{DS(ON)}	V+ = 16.5V, V- = -16.5V, I _S = -10mA, V _D = 5, 0, -5V	Room	-	3	3	Ω
		Full	-	-	5	Ω
Switch OFF Leakage Current, I _{S(OFF)}	V+ = 16.5V, V- = -16.5 V _D = ±15.5V, V _S = ±15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Switch OFF Leakage Current, I _{D(OFF)}	V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = ±15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ _{JA} (°C/W)	θ _{JC} (°C/W)
PDIP Package	90	N/A
SOIC Package	115	N/A
CERDIP Package	75	22
Maximum Junction Temperature (Plastic Package) 150°C	
Maximum Junction Temperature (Hermetic Package) 175°C	
Maximum Storage Temperature Range (D and E Suffix)-65°C to 125°C	
Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only) 300°C	

DG401, DG403, DG405

Electrical Specifications Test Conditions: $V_+ = +15V$, $V_- = -15V$, $V_{IN} = 2.4V, 0.8V, V_L = 5V$ (Note 3),
Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP (°C)	D SUFFIX -40°C TO 85°C			UNITS
			(NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	
Channel ON Leakage Current, $I_{D(ON)}$	$V_{\pm} = \pm 16.5V$, $V_D = V_S = \pm 15.5V$	Room	-1	-0.04	1	nA
		Full	-10	-	10	nA
DIGITAL CONTROL						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	μA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	μA
POWER SUPPLIES						
Positive Supply Current, I_+	$V_+ = 16.5V$, $V_- = -16.5V$, $V_{IN} = 0V$ or $5V$	Room	-	0.01	1	μA
		Full	-	-	5	μA
Negative Supply Current, I_-		Room	-1	-0.01	-	μA
		Full	-5	-	-	μA
Logic Supply Current, I_L		Room	-	0.01	1	μA
		Full	-	-	5	μA
Ground Current, I_{GND}	Room	-1	-0.01	-	μA	
	Full	-5	-	-	μA	

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

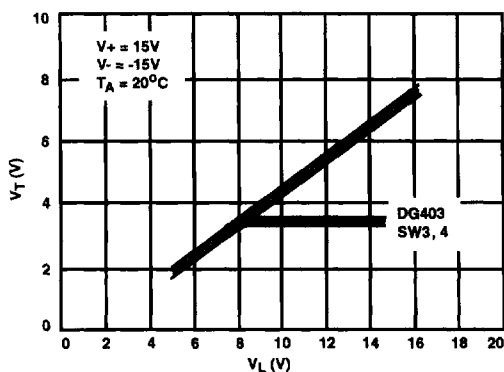


FIGURE 1. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

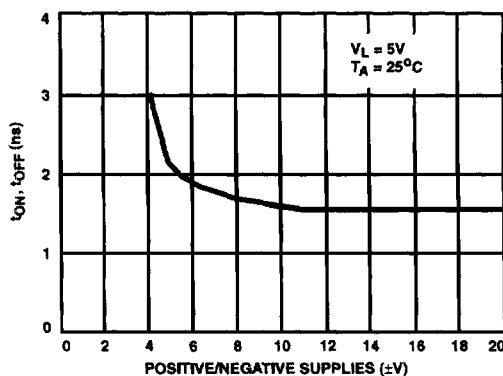


FIGURE 2. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

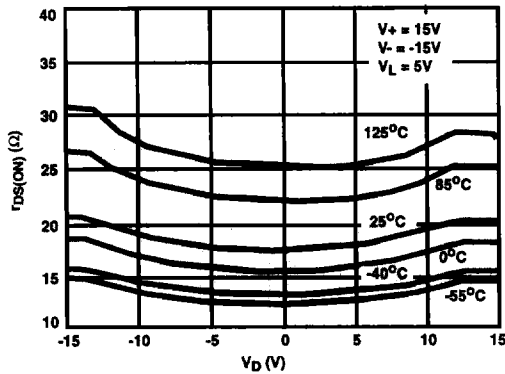


FIGURE 3. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

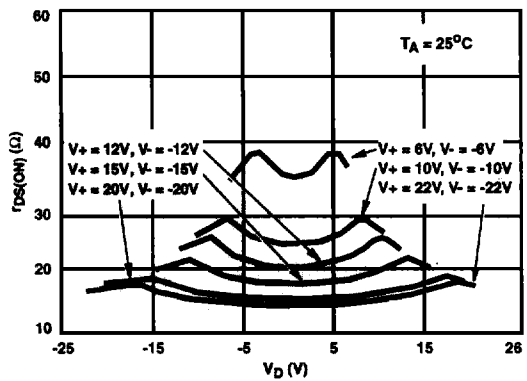


FIGURE 4. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

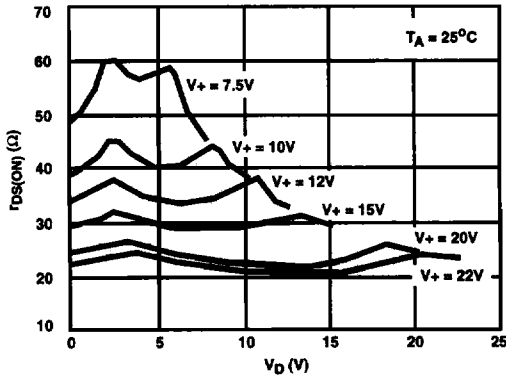


FIGURE 5. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE, $V_- = -0V$

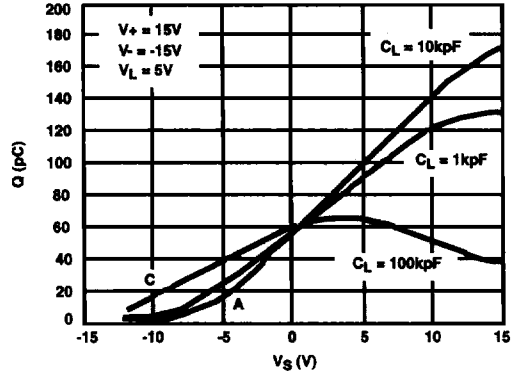


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

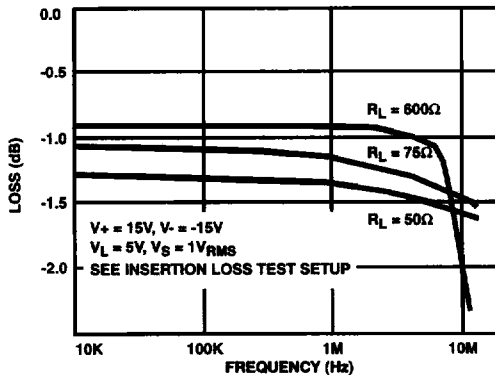


FIGURE 7. INSERTION LOSS vs FREQUENCY

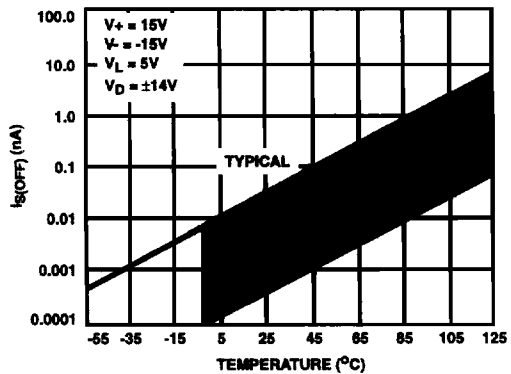


FIGURE 8. $I_{S(OFF)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

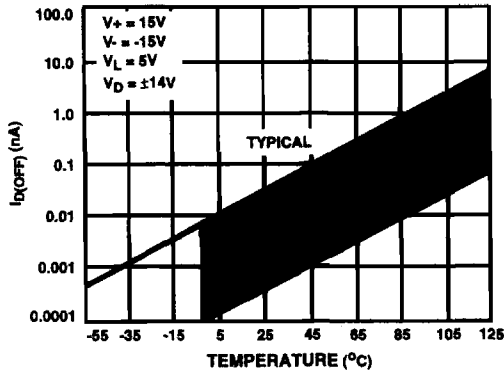


FIGURE 9. $I_{D(OFF)}$ vs TEMPERATURE

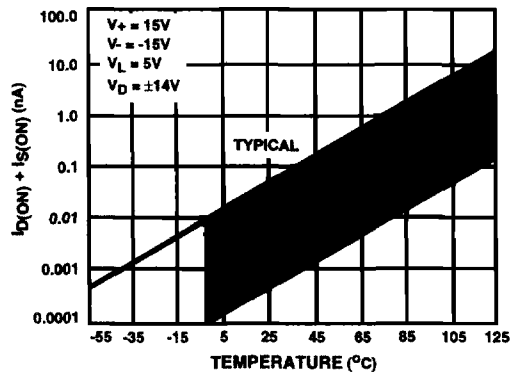


FIGURE 10. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

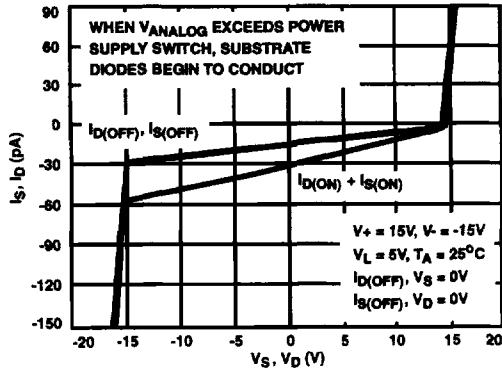


FIGURE 11. LEAKAGE CURRENT vs ANALOG VOLTAGE

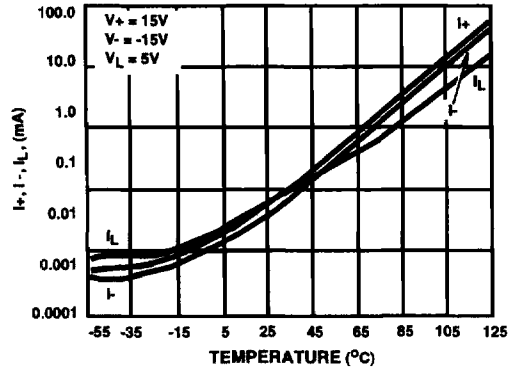


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

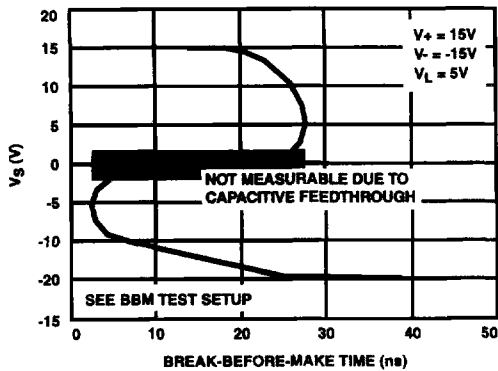


FIGURE 13. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

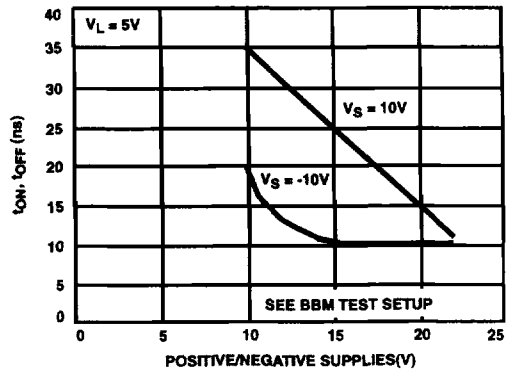


FIGURE 14. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

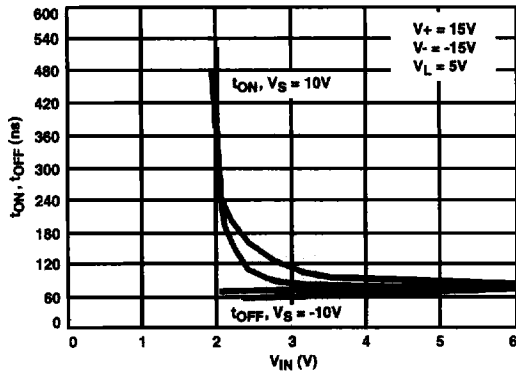


FIGURE 15. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

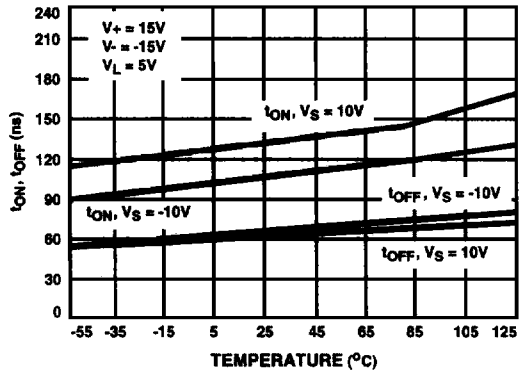


FIGURE 16. SWITCHING TIME vs TEMPERATURE (NOTE 1)

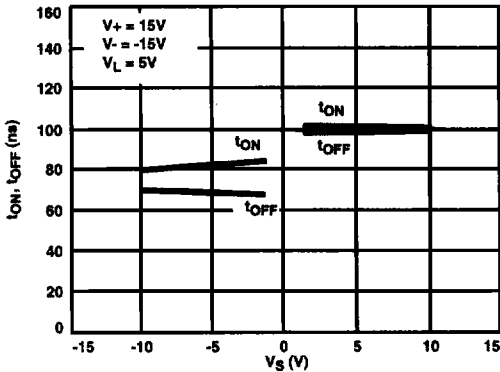


FIGURE 17. SWITCHING TIME vs ANALOG VOLTAGE (NOTE 1)

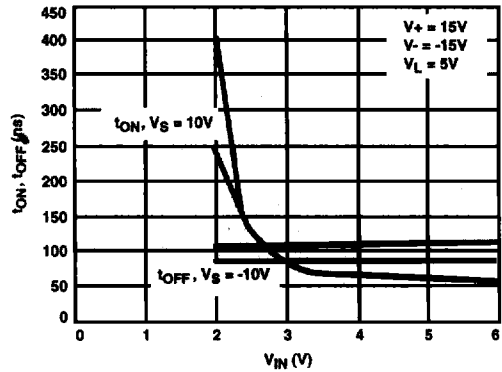


FIGURE 18. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

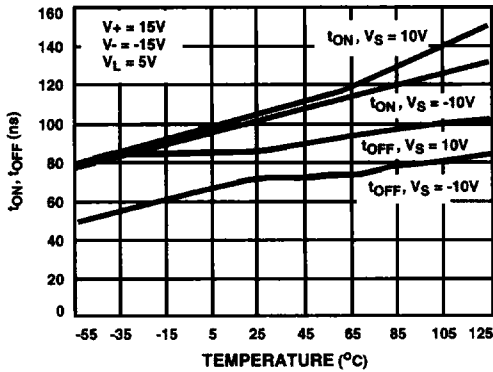


FIGURE 19. SWITCHING TIME vs TEMPERATURE (NOTE 1)

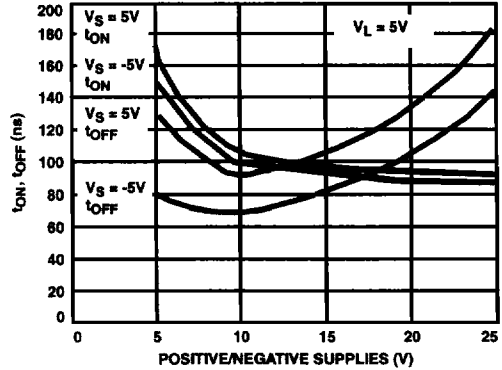


FIGURE 20. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 1)

Typical Performance Curves (Continued)

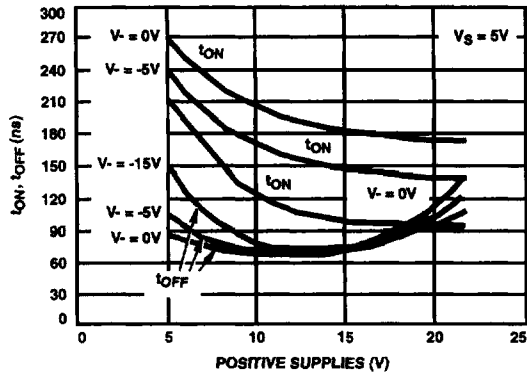


FIGURE 21. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

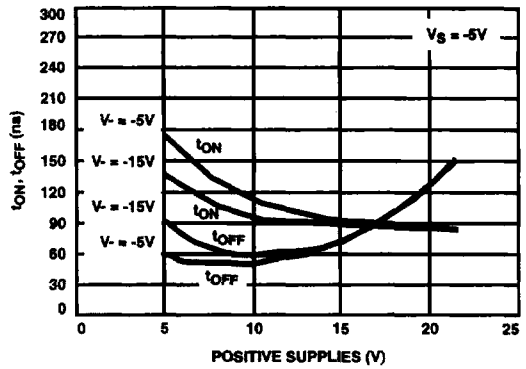


FIGURE 22. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

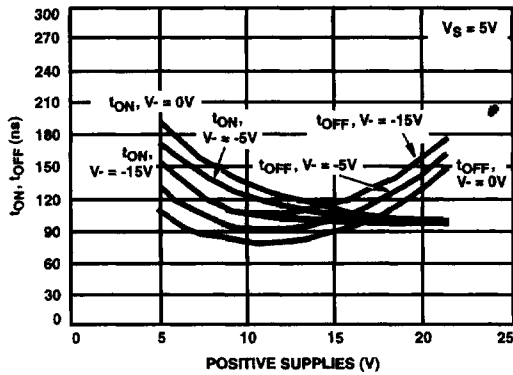


FIGURE 23. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

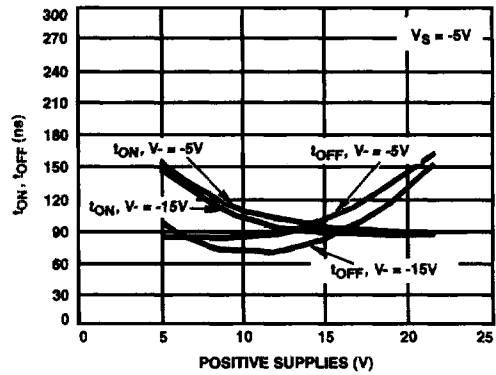
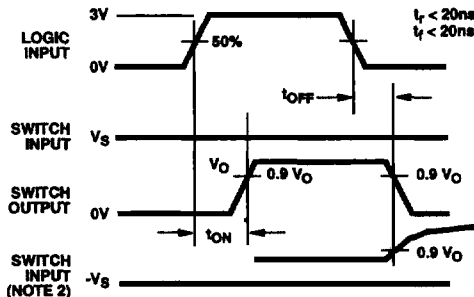


FIGURE 24. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

NOTE:

1. Refer to Figure 1 for test conditions.

Test Circuits and Waveforms

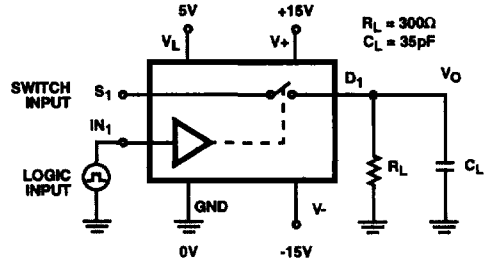


NOTES:

1. Logic input waveform is inverted for switches that have the opposite logic sense.
2. $V_S = 10V$ for t_{ON} , $V_S = -10V$ for t_{OFF} .

FIGURE 25A.

FIGURE 25. SWITCHING TIME



Repeat test for IN_2 and S_2 .

For load conditions, see Specifications. C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 25B.

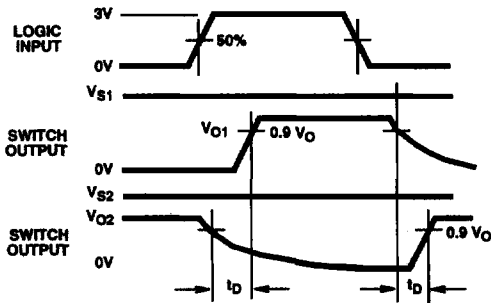
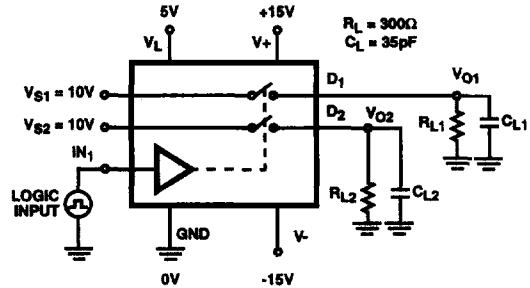


FIGURE 26A.

FIGURE 26. BREAK-BEFORE-MAKE



C_L (includes fixture and stray capacitance).

FIGURE 26B.

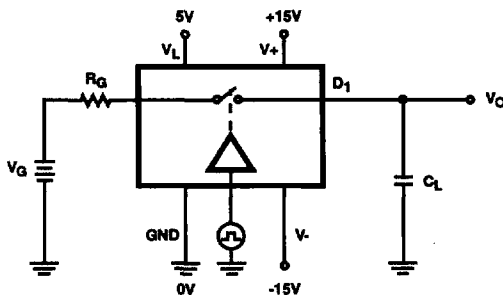
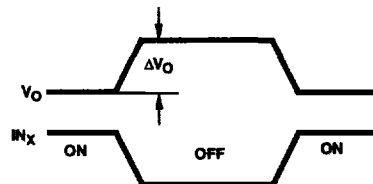


FIGURE 27A.

FIGURE 27. CHARGE INJECTION



$$Q = \Delta V_O \times C_L$$

FIGURE 27B.

Test Circuits and Waveforms (Continued)

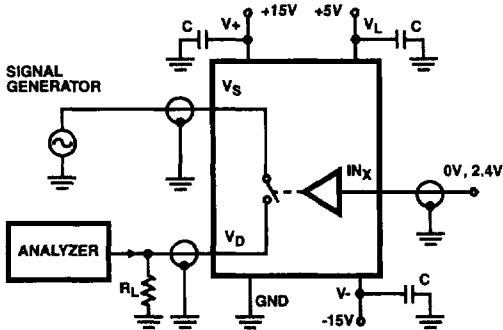


FIGURE 28. OFF ISOLATION

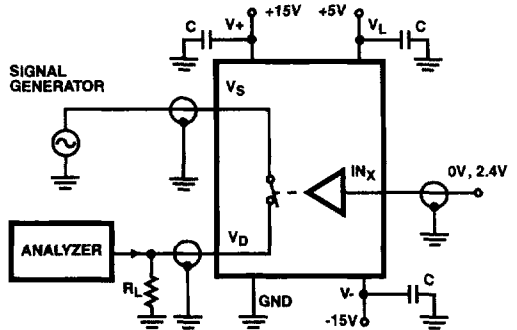


FIGURE 29. INSERTION LOSS

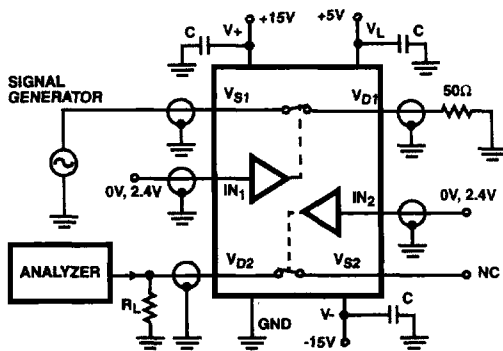


FIGURE 30. CROSSTALK

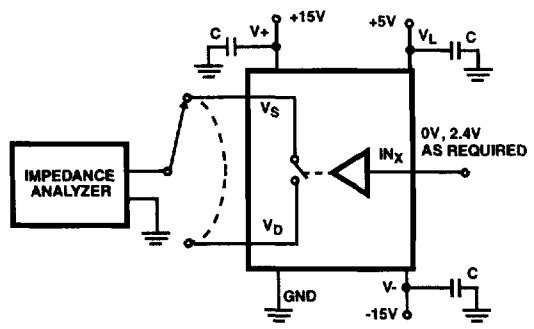


FIGURE 31. CAPACITANCES

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2 . Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

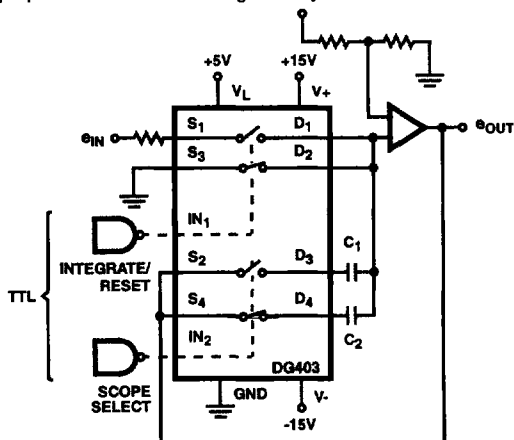


FIGURE 32. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1 . The output of A_2 is fed back to A_3 and compared to the analog input e_{IN} . If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT} of A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

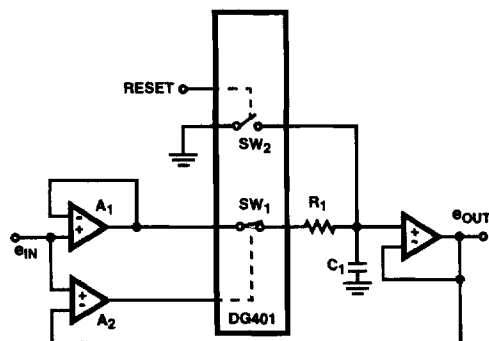


FIGURE 33. POSITIVE PEAK DETECTOR