Freescale Semiconductor
Data Sheet: Technical Data

Document Number: DSP56367
Rev. 2.1, 1/2007

DSP56367

24-Bit Audio Digital Signal Processor

1 Overview

This document briefly describes the DSP56367 24-bit digital signal processor (DSP). The DSP56367 is a member of the DSP56300 family of programmable CMOS DSPs. The DSP56367 is targeted to applications that require digital audio compression/decompression, sound field processing, acoustic equalization and other digital audio algorithms. The DSP56367 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.8 V and 100 million instructions per second (MIPS) using an internal 100 MHz clock at 1.5 V.

Contents

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	**Signal/Symbol**	**Logic State**	**Signal State**	**Voltage***
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

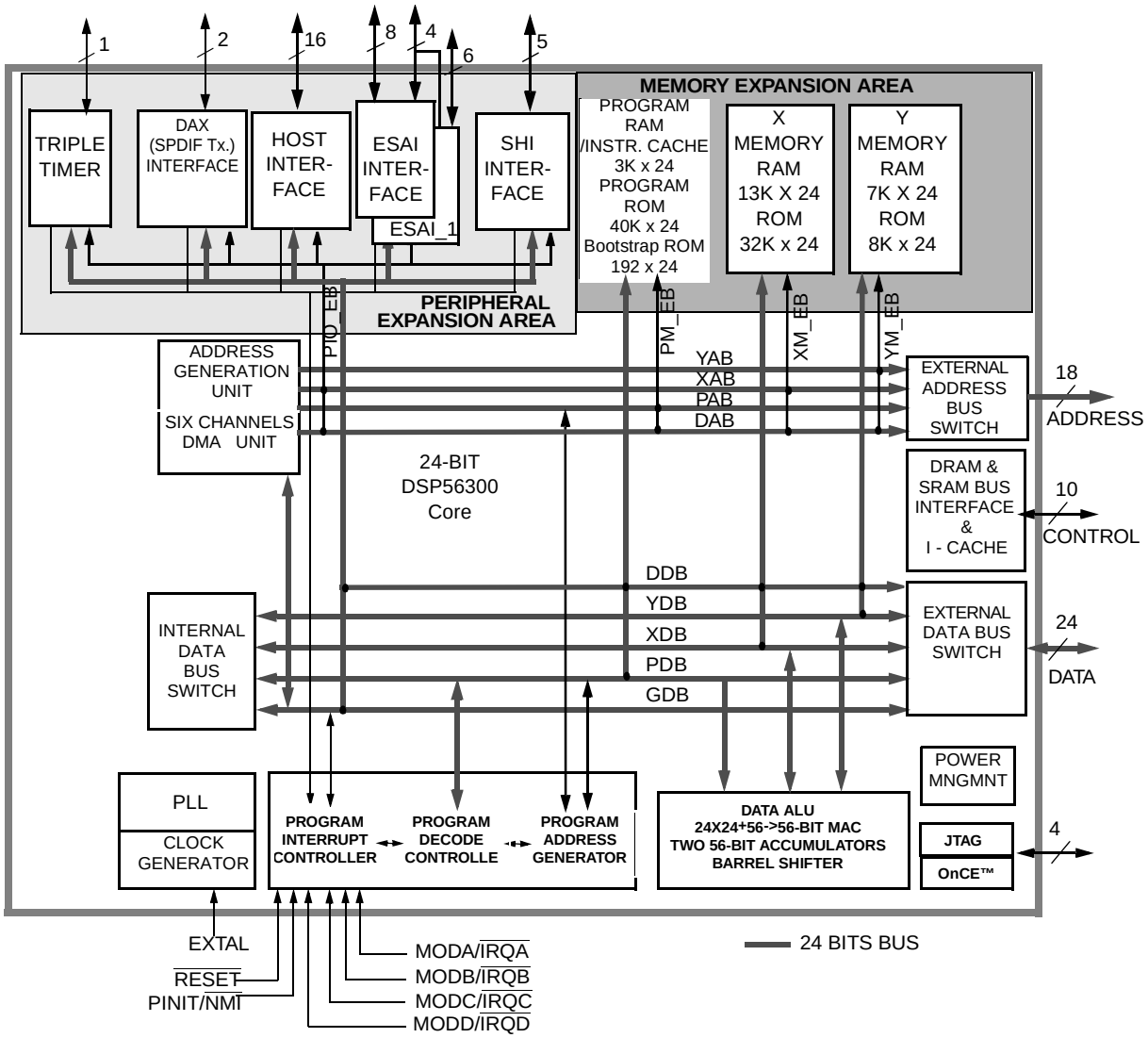


Figure 1-1 DSP56367 Block Diagram

1.1 Features

Core features are described fully in the *DSP56300 Family Manual*.

1.2 DSP56300 modular chassis

- 150 Million Instructions Per Second (MIPS) with a 150 MHz clock at internal logic supply (QVCCL) of 1.8V.
- 100 Million Instructions Per Second (MIPS) with a 100 MHz clock at internal logic supply (QVCCL) of 1.5V.
- Object Code Compatible with the 56K core.
- Data ALU with a 24 × 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE¥ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

1.3 On-chip Memory Configuration

- 7K × 24 Bit Y-Data RAM and 8K × 24 Bit Y-Data ROM.
- 13K × 24 Bit X-Data RAM and 32K × 24 Bit X-Data ROM.
- 40K × 24 Bit Program ROM.
- 3K × 24 Bit Program RAM and 192x24 Bit Bootstrap ROM. 1K of Program RAM may be used as Instruction Cache or for Program ROM patching.
- 2K × 24 Bit from Y Data RAM and 5K × 24 Bit from X Data RAM can be switched to Program RAM resulting in up to 10K × 24 Bit of Program RAM.

1.4 Off-chip memory expansion

- External Memory Expansion Port.
- Off-chip expansion up to two 16M x 24-bit word of Data memory.
- Off-chip expansion up to 16M x 24-bit word of Program memory.
- Simultaneous glueless interface to SRAM and DRAM.

1.5 Peripheral modules

- Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Sony, AC97, network and other programmable protocols.

- Serial Audio Interface I(ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Sony, AC97, network and other programmable protocols
  The ESAI_1 shares four of the data pins with ESAI, and ESAI_1 does NOT support HCKR and HCKT (high frequency clocks)
- Serial Host Interface (SHI): SPI and I^2C protocols, multi master capability, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Byte-wide parallel Host Interface (HDI08) with DMA support.
- Triple Timer module (TEC).
- Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
- Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

1.6 144-pin plastic LQFP package

1.7 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56367 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56367 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56367 Product Brief	Brief description of the chip	DSP56367P
DSP56367 User's Manual	DSP56367 User's Manual	DSP56367UM
DSP56367 Technical Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56367
IBIS Model	Input Output Buffer Information Specification	For software or simulation models, contact sales or go to www.freescale.com.

2 Signal/Connection Descriptions

2.1 Signal Groupings

The input and output signals of the DSP56367 are organized into functional groups, which are listed in Table 2-1 and illustrated in Figure 2-1.

The DSP56367 is operated from a 1.8V supply; however, some of the inputs can tolerate 3.3V. A special notice for this feature is added to the signal descriptions of those inputs.

Remember, the DSP56367 offers 150 million instructions per second (MIPS) using an internal 150 MHz clock at 1.8 V and 100 million instructions per second (MIPS) using an internal 100 MHz clock at 1.3.3V.

Table 2-1 DSP56367 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{CC})		20	Table 2-2
Ground (GND)		18	Table 2-3
Clock and PLL		3	Table 2-4
Address bus	Port A[1]	18	Table 2-5
Data bus		24	Table 2-6
Bus control		10	Table 2-7
Interrupt and mode control		5	Table 2-8
HDI08	Port B[2]	16	Table 2-9
SHI		5	Table 2-10
ESAI	Port C[3]	12	Table 2-11
ESAI_1	Port E[4]	6	Table 2-12
Digital audio transmitter (DAX)	Port D[5]	2	Table 2-13
Timer		1	Table 2-14
JTAG/OnCE Port		4	Table 2-15

1 Port A is the external memory interface port, including the external address bus, data bus, and control signals.
2 Port B signals are the GPIO port signals which are multiplexed with the HDI08 signals.
3 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
4 Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.
5 Port D signals are the GPIO port signals which are multiplexed with the DAX signals.

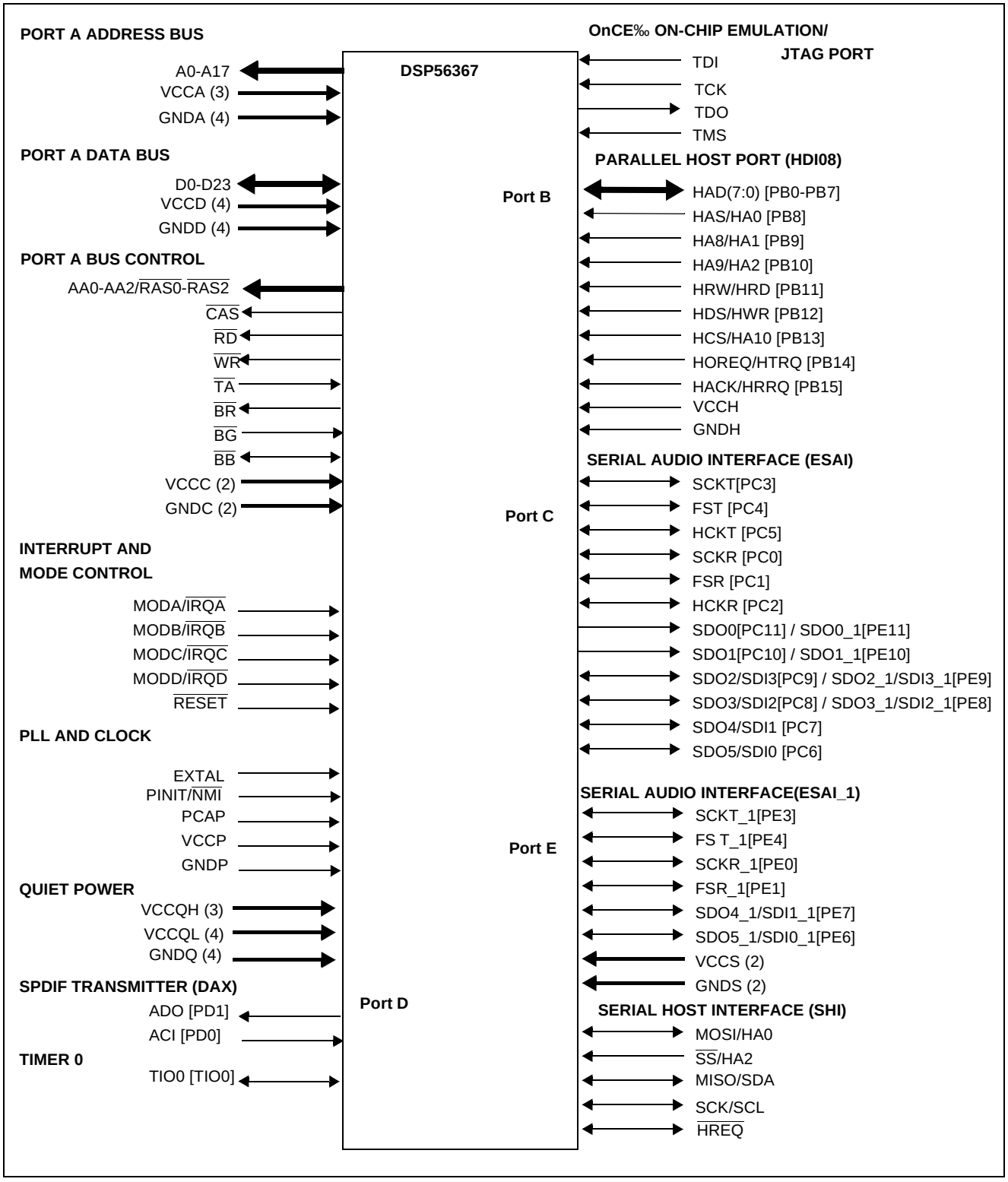


Figure 2-1 Signals Identified by Functional Group

2.2 Power

Table 2-2 Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL} (4)	**Quiet Core (Low) Power—**V_{CCQL} is an isolated power for the internal processing logic. This input must be tied externally to all other V_{CCQL} power pins and the V_{CCP} power pin only. Do not tie with other power pins. The user must provide adequate external decoupling capacitors. There are four V_{CCQL} inputs.
V_{CCQH} (3)	**Quiet External (High) Power**—V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs.The user must provide adequate decoupling capacitors. There are three V_{CCQH} inputs.
V_{CCA} (3)	**Address Bus Power**—V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three V_{CCA} inputs.
V_{CCD} (4)	**Data Bus Power**—V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs.
V_{CCC} (2)	**Bus Control Power**—V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCC} inputs.
V_{CCH}	**Host Power**—V_{CCH} is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input.
V_{CCS} (2)	**SHI, ESAI, ESAI_1, DAX and Timer Power** —V_{CCS} is an isolated power for the SHI, ESAI, ESAI_1, DAX and Timer. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs.

2.3 Ground

Table 2-3 Grounds

Ground Name	Description
GND_P	**PLL Ground**—GND_P is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 µF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_Q (4)	**Quiet Ground**—GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections.
GND_A (4)	**Address Bus Ground**—GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.
GND_D (4)	**Data Bus Ground**—GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_D connections.

Table 2-3 Grounds (continued)

Ground Name	Description
GND_C (2)	**Bus Control Ground**—GND_C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_C connections.
GND_H	**Host Ground**—GND_h is an isolated ground for the HD08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_H connection.
GND_S (2)	**SHI, ESAI, ESAI_1, DAX and Timer Ground**—GND_S is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_S connections.

2.4 Clock and PLL

Table 2-4 Clock and PLL Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL.
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock.

2.5 External Memory Expansion Port (Port A)

When the DSP56367 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant port A signals: A0–A17, D0–D23, AA0/$\overline{\text{RAS0}}$–AA2/$\overline{\text{RAS2}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

2.6 External Address Bus

Table 2-5 External Address Bus Signals

Signal Name	Type	State During Reset	Signal Description
A0–A17	Output	Tri-Stated	**Address Bus**—When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed.

2.7 External Data Bus

Table 2-6 External Data Bus Signals

Signal Name	Type	State during Reset	Signal Description
D0–D23	Input/Output	Tri-Stated	**Data Bus**—When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated.

2.8 External Bus Control

Table 2-7 External Bus Control Signals

Signal Name	Type	State During Reset	Signal Description
AA0–AA2/ $\overline{\text{RAS0}}$–$\overline{\text{RAS2}}$	Output	Tri-Stated	**Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity.
$\overline{\text{CAS}}$	Output	Tri-Stated	**Column Address Strobe**— When the DSP is the bus master, $\overline{\text{CAS}}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the bus mastership enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.
$\overline{\text{RD}}$	Output	Tri-Stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D0-D23). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-Stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D0-D23). Otherwise, $\overline{\text{WR}}$ is tri-stated.
$\overline{\text{TA}}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP is the bus master and there is no external bus activity, or the DSP is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) may be added to the wait states inserted by the BCR by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to the internal system clock. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion, otherwise improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR). $\overline{\text{TA}}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.

Table 2-7 External Bus Control Signals (continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{BR}$	Output	Output (deasserted)	**Bus Request**—$\overline{BR}$ is an active-low output, never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56367 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56367 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—$\overline{BG}$ is an active-low input. $\overline{BG}$ is asserted by an external bus arbitration circuit when the DSP56367 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56367 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. For proper $\overline{BG}$ operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set.
$\overline{BB}$	Input/ Output	Input	**Bus Busy**—$\overline{BB}$ is a bidirectional active-low input/output. $\overline{BB}$ indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without rearbitration until another device requires the bus. The deassertion of $\overline{BB}$ is done by an “active pull-up” method (i.e., $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). For proper $\overline{BB}$ operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set. $\overline{BB}$ requires an external pull-up resistor.

2.9 Interrupt and Mode Control

The interrupt and mode control signals select the chip’s operating mode as it comes out of hardware reset. After $\overline{RESET}$ is deasserted, these inputs are hardware interrupt request lines.

Table 2-8 Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. *This input is 3.3V tolerant*.
MODB/IRQB	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 3.3V tolerant.
MODC/IRQC	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 3.3V tolerant.
MODD/IRQD	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/IRQD is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/IRQD selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 3.3V tolerant.
RESET	Input	Input	**Reset—**RESET is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted during power up. A stable EXTAL signal must be supplied while RESET is being asserted. *This input is 3.3V tolerant*.

2.10 Parallel Host Interface (HDI08)

The HDI08 provides a fast, 8-bit, parallel data port that may be connected directly to the host bus. The HDI08 supports a variety of standard buses and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

Table 2-9 Host Interface

Signal Name	Type	State During Reset	Signal Description
H0–H7	Input/ Output	GPIO Disconnected	**Host Data—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, tri-state data bus.
HAD0–HAD7	Input/ Output		**Host Address/Data—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the address/data bidirectional, multiplexed, tri-state bus.
PB0–PB7	Input, Output, or Disconnected		**Port B 0–7**—When the HDI08 is configured as GPIO, these signals are individually programmable as input, output, or internally disconnected. The default state after reset for these signals is GPIO disconnected. These inputs are 3.3V tolerant.
HA0	Input	GPIO Disconnected	**Host Address Input 0**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable, but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input, Output, or Disconnected		**Port B 8**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.
HA1	Input	GPIO Disconnected	**Host Address Input 1**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input, Output, or Disconnected		**Port B 9**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State During Reset	Signal Description
HA2	Input	GPIO Disconnected	**Host Address Input 2**—When the HDI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input, Output, or Disconnected		**Port B 10**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.
HRW	Input	GPIO Disconnected	**Host Read/Write**—When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input.
$\overline{\text{HRD}}$/ HRD	Input		**Host Read Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host read data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input, Output, or Disconnected		**Port B 11**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.
$\overline{\text{HDS}}$/ HDS	Input	GPIO Disconnected	**Host Data Strobe—**When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/ HWR	Input		**Host Write Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input, Output, or Disconnected		**Port B 12**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State During Reset	Signal Description
HCS	Input	GPIO Disconnected	**Host Chip Select—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{\text{HCS}}$) after reset.
HA10	Input		**Host Address 10**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input, Output, or Disconnected		**Port B 13**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.
$\overline{\text{HOREQ}}$/ HOREQ	Output	GPIO Disconnected	**Host Request**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host request (HOREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HOREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/ HTRQ	Output		**Transmit Host Request—**When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input, Output, or Disconnected		**Port B 14**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.
$\overline{\text{HACK}}$/ HACK	Input	GPIO Disconnected	**Host Acknowledge**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/ HRRQ	Output		**Receive Host Request**—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input, Output, or Disconnected		**Port B 15**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 3.3V tolerant.

2.11 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 2-10 Serial Host Interface Signals

Signal Name	Signal Type	State During Reset	Signal Description
SCK	Input or Output	Tri-Stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or Output		**I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant.
MISO	Input or Output	Tri-Stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or Open-Drain Output		**I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant.

Table 2-10 Serial Host Interface Signals (continued)

Signal Name	Signal Type	State During Reset	Signal Description
MOSI	Input or Output	Tri-Stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		**I^{2}C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for I^{2}C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant.
$\overline{SS}$	Input	Tri-Stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I^{2}C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^{2}C mode. When configured for the I^{2}C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^{2}C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 3.3V tolerant.
$\overline{HREQ}$	Input or Output	Tri-Stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. This input is 3.3V tolerant.

2.12 Enhanced Serial Audio Interface

Table 2-11 Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or Output	GPIO Disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, Output, or Disconnected		**Port C 2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
HCKT	Input or Output	GPIO Disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, Output, or Disconnected		**Port C 5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
FSR	Input or Output	GPIO Disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, Output, or Disconnected		**Port C 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FST	Input or Output	GPIO Disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, Output, or Disconnected		**Port C 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SCKR	Input or Output	GPIO Disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, Output, or Disconnected		**Port C 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SCKT	Input or output	GPIO Disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, Output, or Disconnected		**Port C 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SDO5	Output	GPIO Disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, Output, or Disconnected		**Port C 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO4	Output	GPIO Disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		**Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, Output, or Disconnected		**Port C 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SDO3/ SDO3_1	Output	GPIO Disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 3.
SDI2/ SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 2.
PC8/PE8	Input, Output, or Disconnected		**Port C 8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 8 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SDO2/ SDO2_1	Output	GPIO Disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 2.
SDI3/ SDI3_1	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 3.
PC9/PE9	Input, Output, or Disconnected		**Port C 9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 9 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
SDO1/ SDO1_1	Output	GPIO Disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 1.
PC10/ PE10	Input, Output, or disconnected		**Port C 10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 10 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO0/ SDO0_1	Output	GPIO Disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 0.
PC11/ PE11	Input, Output, or Disconnected		**Port C 11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 11 signal. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

2.13 Enhanced Serial Audio Interface_1

Table 2-12 Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or Output	GPIO Disconnected	**Frame Sync for Receiver_1**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, Output, or Disconnected		**Port E 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V.
FST_1	Input or Output	GPIO Disconnected	**Frame Sync for Transmitter_1**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PE4	Input, Output, or Disconnected		**Port E 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V.

Table 2-12 Enhanced Serial Audio Interface_1 Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or Output	GPIO Disconnected	**Receiver Serial Clock_1**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, Output, or Disconnected		**Port E 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V.
SCKT_1	Input or Output	GPIO Disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, Output, or Disconnected		**Port E 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V.
SDO5_1	Output	GPIO Disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		**Serial Data Input 0_1**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, Output, or Disconnected		**Port E 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 3.3V.
SDO4_1	Output	GPIO Disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		**Serial Data Input 1_1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, Output, or Disconnected		**Port E 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

2.14 SPDIF Transmitter Digital Audio Interface

Table 2-13 Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI	Input	GPIO Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively).
PD0	Input, Output, or Disconnected		**Port D 0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.
ADO	Output	GPIO Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format.
PD1	Input, Output, or Disconnected		**Port D 1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 3.3V tolerant.

2.15 Timer

Table 2-14 Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to Vcc through a pull-up resistor in order to ensure a stable logic level at this input. This input is 3.3 V tolerant.

2.16 JTAG/OnCE Interface

Table 2-15 JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. This input is 3.3V tolerant.
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 3.3V tolerant.
TDO	Output	Tri-Stated	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 3.3V tolerant.

NOTES

3 Specifications

3.1 Introduction

The DSP56367 is a high density CMOS device with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Finalized specifications may be published after further characterization and device qualifications are completed.

3.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{CC}). The suggested value for a pull-up or pull-down resistor is 10 k .

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification will never occur in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CCQL}, V_{CCP}	0.3 to + 2.0	V
	V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, V_{CCS},	0.3 to + 4.0	V
All “3.3V tolerant” input voltages	V_{IN}	GND 0.3 to V_{CC} + 0.7	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range[3]	T_J	40 to + 95	°C
Storage temperature	T_{STG}	55 to +125	°C

1 GND = 0 V, VCCP, VCCQL = 1.8 V ±5%, TJ = –40×C to +95×C, CL = 50 pF
All other VCC = 3.3 V ± 5%, TJ = –40×C to +95×C, CL = 50 pF

2 Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

3 Temperatures below -0°C are qualified for consumer applications.

3.3 Thermal Characteristics

Table 3-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	R_{JA} or $_{JA}$	45.0	°C/W
Junction-to-case thermal resistance[3]	R_{JC} or $_{JC}$	10.0	°C/W
Natural Convection, Thermal characterization parameter[4]	$_{JT}$	3.0	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4 DC Electrical Characteristics

Table 3-3 DC Electrical Characteristics[1]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (V_{CCQL}) • PLL(V_{CCP})	V_{CC}	1.71	1.8	1.89	V
Supply voltages • V_{CCQH} • V_{CCA} • V_{CCD} • V_{CCC} • V_{CCH} • V_{CCS}	V_{CC}	3.14	3.3	3.46	V
Input high voltage					V
• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1 (except SDO4_1)	V_{IH}	2.0	—	V_{CCQH}	
• MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI_1/Timer/HDI08/DAX/(only SDO4_1)/SHI(SPI mode)	V_{IHP}	2.0	—	V_{CCQH} + 03 max for both V_{IHP}	
• SHI(I2C mode)	V_{IHP}	1.5	—	V_{CCQH} + 03 max for both V_{IHP}	
• EXTAL	V_{IHX}	0.8 × V_{CCQH}	—	0.8 × V_{CCQH}	
Input low voltage					V
• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1(except SDO4_1)	V_{IL}	–0.3	—	0.8	
• MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1(only SDO4_1)/SHI(SPI mode)	V_{ILP}	–0.3	—	0.8	
• SHI(I2C mode)	V_{ILP}	–0.3	—	0.3 x V_{CC}	
• EXTAL	V_{ILX}	–0.3	—	0.2 x V_{CCQH}	
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[3]	V_{OH}	2.4	—	—	V
Output low voltage[3]	V_{OL}	—	—	0.4	V
Internal supply current[4] at internal clock of 150MHz					mA
• In Normal mode	I_{CCI}	—	58.0	115	
• In Wait mode	I_{CCW}	—	7.3	20	
• In Stop mode[5]	I_{CCS}	—	2.0	4	
PLL supply current		—	1	2.5	mA
Input capacitance[6]	C_{IN}	—	—	10	pF

1 V_{CCQL} = 1.8 V ± 5%, T_J = –40°C to +95°C, C_L = 50 pF
All other V_{CC} = 3.3 V ± 5%, T^J = –40°C to +95°C, C_L = 50 pF

2 Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$, and MODD/$\overline{IRQD}$ pins.

3 This characteristic does not apply to PCAP.

4 The Appendix A, "Power Consumption Benchmark" section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CCQL} = 1.8V, $V_{CC(other)}$ = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CCQL} = 1.89V, $V_{CC(other)}$ = 3.46V at T_J = 95°C.

5 In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

6 Periodically sampled and not 100% tested

3.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.4 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56367 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

3.6 Internal Clocks

Table 3-4 Internal Clocks

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency with PLL enabled	f	—	(Ef × MF)/(PDF × DF)	—
Internal operation frequency with PLL disabled	f	—	Ef/2	—
Internal clock high period	T_H			
• With PLL disabled		—	ET_C	—
• With PLL enabled and MF 4		$0.49 \times ET_C \times PDF \times DF/MF$	—	$0.51 \times ET_C \times PDF \times DF/MF$
• With PLL enabled and MF > 4		$0.47 \times ET_C \times PDF \times DF/MF$	—	$0.53 \times ET_C \times PDF \times DF/MF$
Internal clock low period	T_L			
• With PLL disabled		—	ET_C	—
• With PLL enabled and MF 4		$0.49 \times ET_C \times PDF \times DF/MF$	—	$0.51 \times ET_C \times PDF \times DF/MF$
• With PLL enabled and MF > 4		$0.47 \times ET_C \times PDF \times DF/MF$	—	$0.53 \times ET_C \times PDF \times DF/MF$
Internal clock cycle time with PLL enabled	T_C	—	$ET_C \times PDF \times DF/MF$	—

Table 3-4 Internal Clocks (continued)

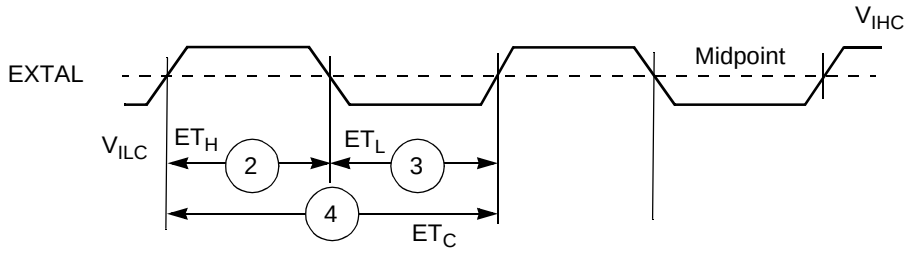
Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal clock cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

1 DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle

2 Refer to the DSP56300 Family Manual for a detailed discussion of the PLL.

3.7 External Clock Operation

The DSP56367 system clock is an externally supplied square wave voltage source connected to EXTAL(Figure 3-1).



Note: The midpoint is 0.5 (V_{IHC} + V_{ILC}).

Figure 3-1 External Clock Timing

Table 3-5 Clock Operation

No.	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 2 ns maximum.	Ef	2.0 ns	150.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_H	 3.11 ns 2.83 ns	 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_L	 3.11 ns 2.83 ns	 157.0 µs

Table 3-5 Clock Operation (continued)

No.	Characteristics	Symbol	Min	Max
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 6.7 ns 6.7 ns	 273.1 µs
7	Instruction cycle time = I_{CYC} = T_C[4] • With PLL disabled • With PLL enabled	I_{CYC}	 13.33 ns 6.67 ns	 8.53 µs

1 Measured at 50% of the input transition.

2 The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.

3 The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

4 The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.

3.8 Phase Lock Loop (PLL) Characteristics

Table 3-6 PLL Characteristics

Characteristics	Min	Max	Unit
V_{CO} frequency when PLL enabled (MF × E_f × 2/PDF)	30	300	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1)] • @ MF 4 • @ MF > 4	 (MF × 580) 100 MF × 830	 (MF × 780) 140 MF × 1470	pF

1 C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(MF x 680)-120, for MF 4, or
MF x 1100, for MF > 4.

3.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1]

No.	Characteristics	Expression	Min	Max	Unit
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[2]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[3]				
	• Power on, external clock generator, PLL disabled	$50 \times ET_C$	333.4	—	ns
	• Power on, external clock generator, PLL enabled	$1000 \times ET_C$	6.7	—	µs
	• Power on, Internal oscillator	$75000 \times ET_C$	500	—	µs
	• During STOP, XTAL disabled	$75000 \times ET_C$	500	—	µs
	• During STOP, XTAL enabled	$2.5 \times T_C$	16.7	—	ns
	• During normal operation	$2.5 \times T_C$	16.7	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[4]				ns
	• Minimum	3.25 × TC + 2.0	23.7	—	
	• Maximum	20.25 × TC + 10	—	145.0	
11	Syn reset setup time from RESET				ns
	• Maximum	T_C	—	6.7	
12	Syn reset deassert delay time				ns
	• Minimum	$3.25 \times T_C + 1.0$	22.7	—	
	• Maximum	$20.25 \times T_C + 5.0$	—	140.0	
13	Mode select setup time		30.0	—	ns
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		4.4	—	ns
16	Minimum edge-triggered interrupt request deassertion width		4.4	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid				ns
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	30.3	—	
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	50.3	—	
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	71.7	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[5, 6, 7]	$(WS + 3.75) \times T_C - 10.94$	—	Note 8	ns
20	Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts[5, 6, 7]	$(WS + 3.25) \times T_C - 10.94$	—	Note 8	ns

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression	Min	Max	Unit
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[5, 6, 7]				ns
	• DRAM for all WS	(WS + 3.5) × T_C – 10.94	—	Note 8	
	• SRAM WS = 1	N/A	—	Note 8	
	• SRAM WS = 2, 3	1.75 × T_C – 4.0	—	Note 8	
	• SRAM WS 4	2.75 × T_C – 4.0	—	Note 8	
22	Synchronous int setup time from IRQs NMI assertion to the CLKOUT trans.	0.6 × T_C – 0.1	3.9	—	ns
23	Synch. int delay time from the CLKOUT trans2 to the first external address out valid caused by first inst fetch				ns
	• Minimum	9.25 × T_C + 1.0	62.7	—	
	• Maximum	24.75 × T_C + 5.0	—	170.0	
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state	0.6 × T_C 0.1	3.9	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 8]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	PLC × ET_C × PDF + (128 K PLC/2) × T_C	—	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	PLC × ET_C × PDF + (23.75 +/- 0.5) × T_C	—	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	(8.25 0.5) × T_C	51.7	58.3	ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 8]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	PLC × ET_C × PDF + (128 K PLC/2) × T_C	—	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	PLC × ET_C × PDF + (20.5 +/- 0.5) × T_C	—	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	5.5 × T_C	36.7	—	ns
27	Interrupt Requests Rate				ns
	• HDI08, ESAI, ESAI_1, SHI, DAX, Timer	12T_C	—	80.0	
	• DMA	8T_C	—	53.0	
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	8T_C	—	53.0	
	• $\overline{IRQ}$ (level trigger)	12T_C	—	80.0	

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression	Min	Max	Unit
28	DMA Requests Rate				ns
	• Data read from HDI08, ESAI, ESAI_1, SHI, DAX	$6T_C$	—	40.0	
	• Data write to HDI08, ESAI, ESAI_1, SHI, DAX	$7T_C$	—	46.7	
	• Timer	$2T_C$		13.3	
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3T_C$	—	20.0	
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	30.3	—	ns

1 V_{CCQH} = 3.3 V ± 5%; V_{CC}= 1.8V ± 5%; T_J = –40°C to + 95°C, C_L = 50 pF

2 Periodically sampled and not 100% tested.

3 $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid. When the V_{CC} is valid, but the other “required $\overline{\text{RESET}}$ duration” conditions (as specified above) have not been yet met, the device circuitry will not be in an initialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

4 If PLL does not lose lock.

5 When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

6 WS = number of wait states (measured in clock cycles, number of T_C).

7 Use expression to compute maximum value.

8 This timing depends on several settings:

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs: the stop delay counter completes count or PLL lock procedure completion.

PLC value for PLL disable is 0.

The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 150 MHz it is 4096/150 MHz = 27.3 µs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.

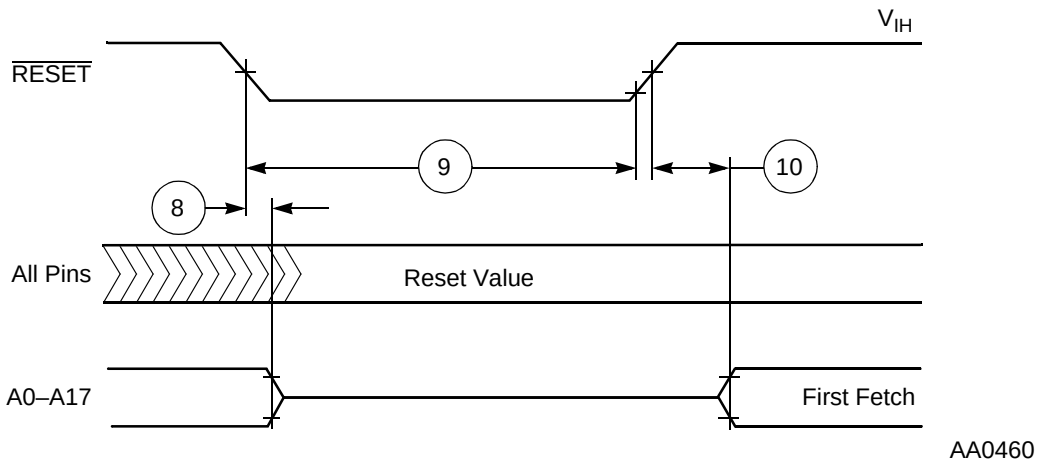
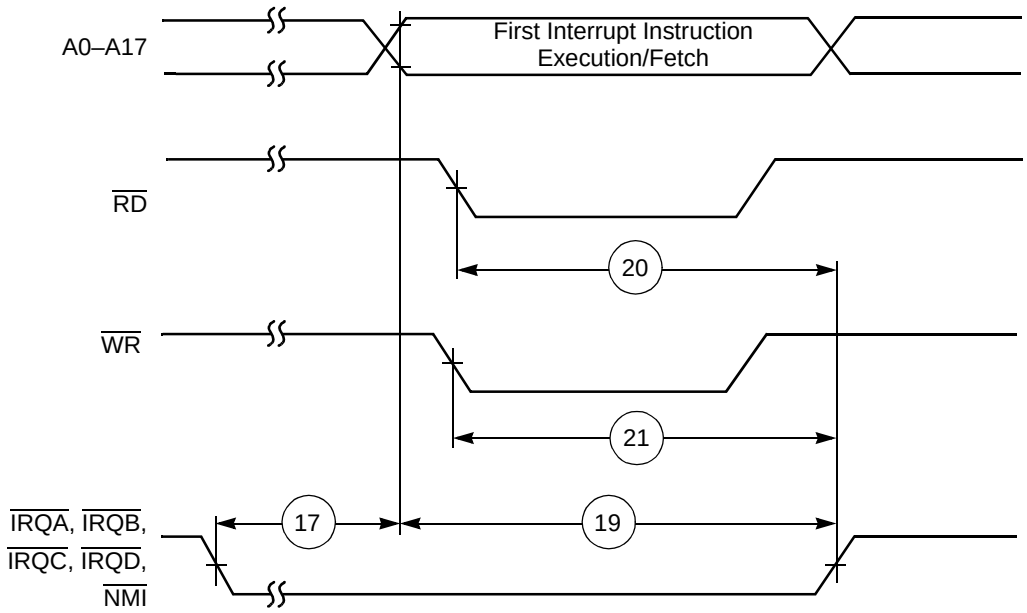
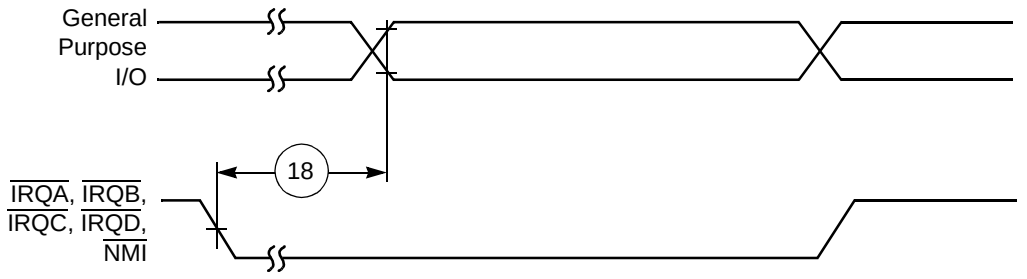


Figure 3-2 Reset Timing



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 3-3 External Fast Interrupt Timing

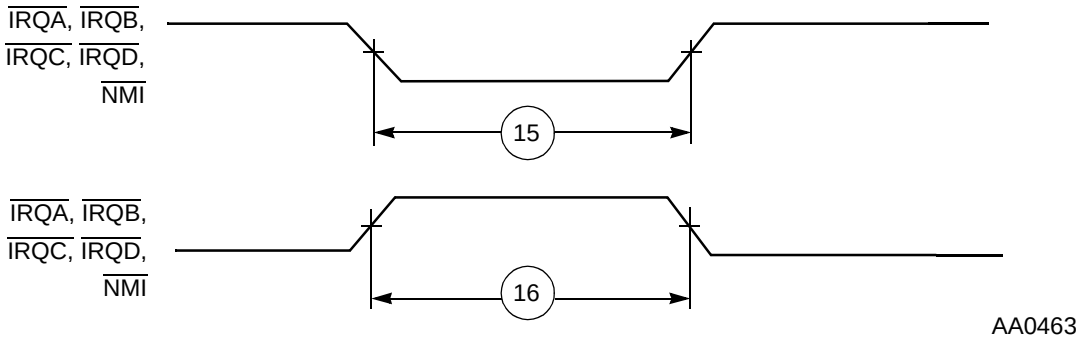


Figure 3-4 External Interrupt Timing (Negative Edge-Triggered)

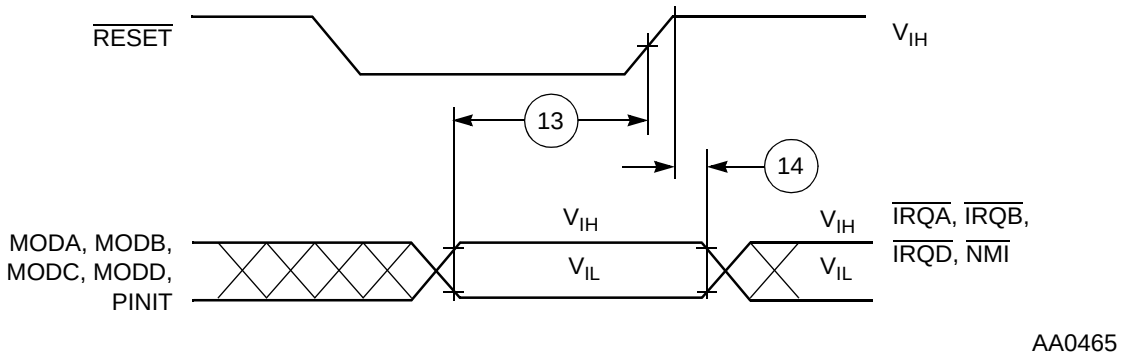


Figure 3-5 Operating Mode Select Timing

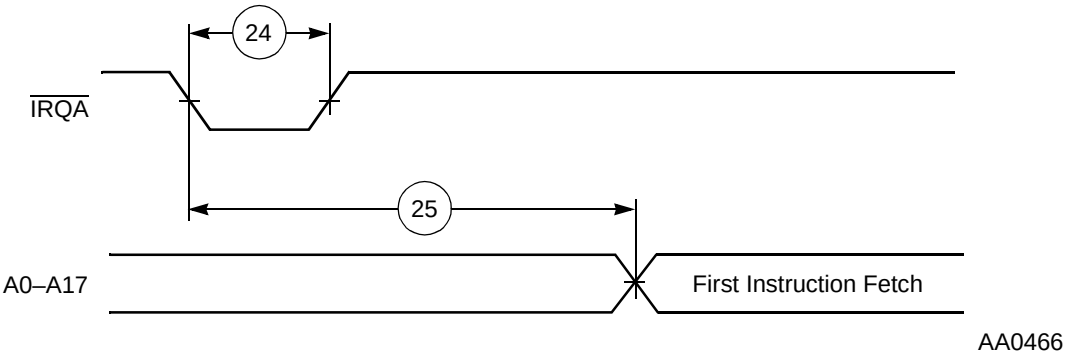


Figure 3-6 Recovery from Stop State Using IRQA Interrupt Service

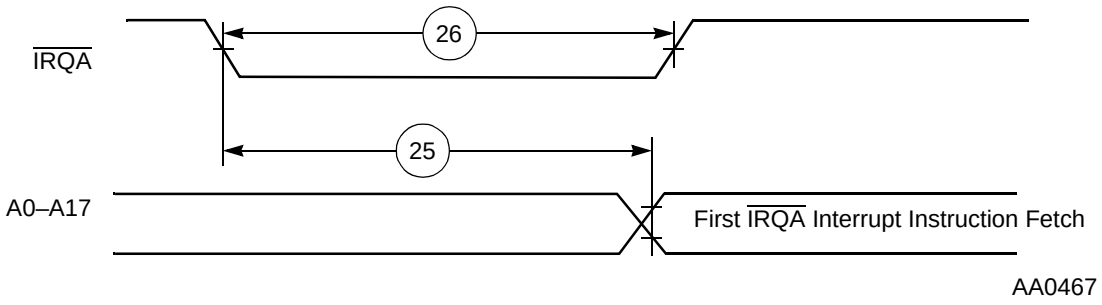


Figure 3-7 Recovery from Stop State Using IRQA Interrupt Service

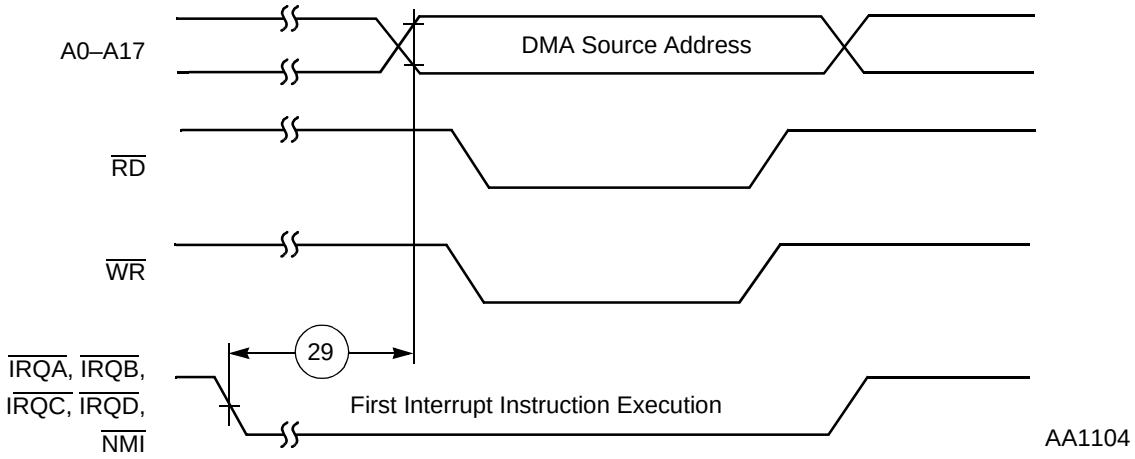


Figure 3-8 External Memory Access (DMA Source) Timing

3.10 External Memory Expansion Port (Port A)

3.10.1 SRAM Timing

Table 3-8 SRAM Read and Write Accesses

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	(WS + 2) × T_C 4.0 [2 WS 7]	22.7	—	ns
			(WS + 3) × T_C 4.0 [WS 8]	69.3	—	ns
101	Address and AA valid to WR assertion	t_{AS}	0.75 × T_C 2.0[2 WS 3]	3.0	—	ns
			1.25 × T_C 2.0[WS 4]	6.3	—	ns
102	WR assertion pulse width	t_{WP}	WS × T_C 4.0 [2 WS 3]	9.3	—	ns
			(WS 0.5) × T_C 4.0[WS 4]	19.3	—	ns
103	WR deassertion to address not valid	t_{WR}	1.25 × T_C 4.0[2 WS 7]	4.3	—	ns
			2.25 × T_C 4.0[WS 8]	11.0	—	ns

Table 3-8 SRAM Read and Write Accesses (continued)

No.	Characteristics	Symbol	Expression[1]	150 MHz		Unit
				Min	Max	
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C 5.0 [WS 2]	—	13.3	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C 5.0 [WS 2]	—	10.0	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C 4.0 [WS 2]	14.3	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	(WS 0.25) × T_C 3.0 [WS 2]	8.7	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	1.25 × T_C 2.0[2 WS 7] 2.25 × T_C 2.0 [WS 8]	6.3 13.0	— —	ns ns
110	$\overline{WR}$ assertion to data active	—	0.25 × T_C 3.7 [2 WS 3] 0.25 × T_C 3.7 [WS 4]	-2.0 -5.4	— —	ns ns
111	$\overline{WR}$ deassertion to data high impedance	—	0.25 × T_C + 0.2 [2 WS 3] 1.25 × T_C + 0.2 [4 WS 7] 2.25 × T_C + 0.2 [WS 8]	— — —	1.9 8.5 15.2	ns ns ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	1.25 × T_C 4.0 [2 WS 3] 2.25 × T_C 4.0 [4 WS 7] 3.25 × T_C 4.0 [WS 8]	4.3 11.0 17.7	— — —	ns ns ns
113	$\overline{RD}$ deassertion time		1.75 × T_C 4.0 [2 WS 7] 2.75 × T_C 4.0 [WS 8]	7.7 14.3	— —	ns ns
114	$\overline{WR}$ deassertion time		2.0 × T_C 4.0 [2 WS 3] 2.5 × T_C 4.0 [4 WS 7] 3.5 × T_C 4.0 [WS 8]	9.3 12.7 19.3	— — —	ns ns ns
115	Address valid to $\overline{RD}$ assertion		0.5 × T_C 2.0	1.3	—	ns
116	$\overline{RD}$ assertion pulse width		(WS + 0.25) × T_C 4.0	11.0	—	ns
117	$\overline{RD}$ deassertion to address not valid		1.25 × T_C 2.0 [2 WS 7] 2.25 × T_C 2.0 [WS 8]	6.3 13.0	— —	ns ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[3]		0.25 × T_C + 2.0	3.7	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0.0	—	ns

1 WS is the number of wait states specified in the BCR. The value is given for the minimum for a given category. (For example, for a category of [2 WS 7] timing is specified for 2 wait states.) Two wait states is the minimum otherwise.

2 Timings 100, 107 are guaranteed by design, not tested.

3 In the case of $\overline{TA}$ negation: timing 118 is relative to the deassertion edge of $\overline{RD}$ or WR were $\overline{TA}$ to remain active.

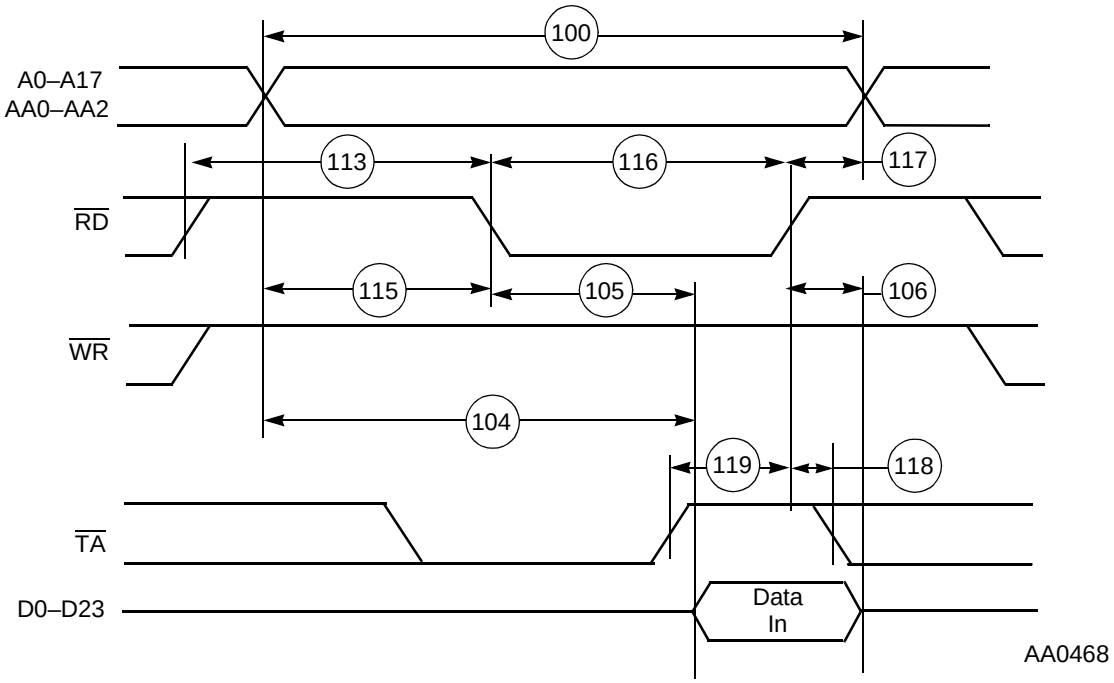


Figure 3-9 SRAM Read Access

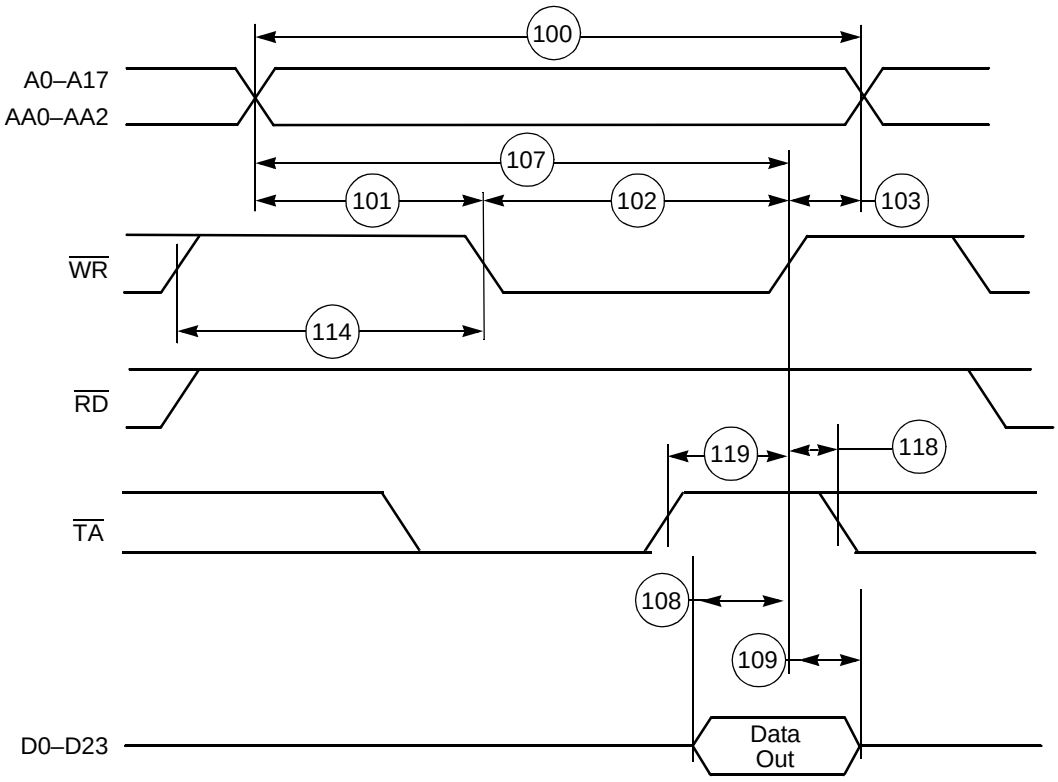


Figure 3-10 SRAM Write Access

3.10.2 DRAM Timing

The selection guides provided in Figure 3-11 and Figure 3-14 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

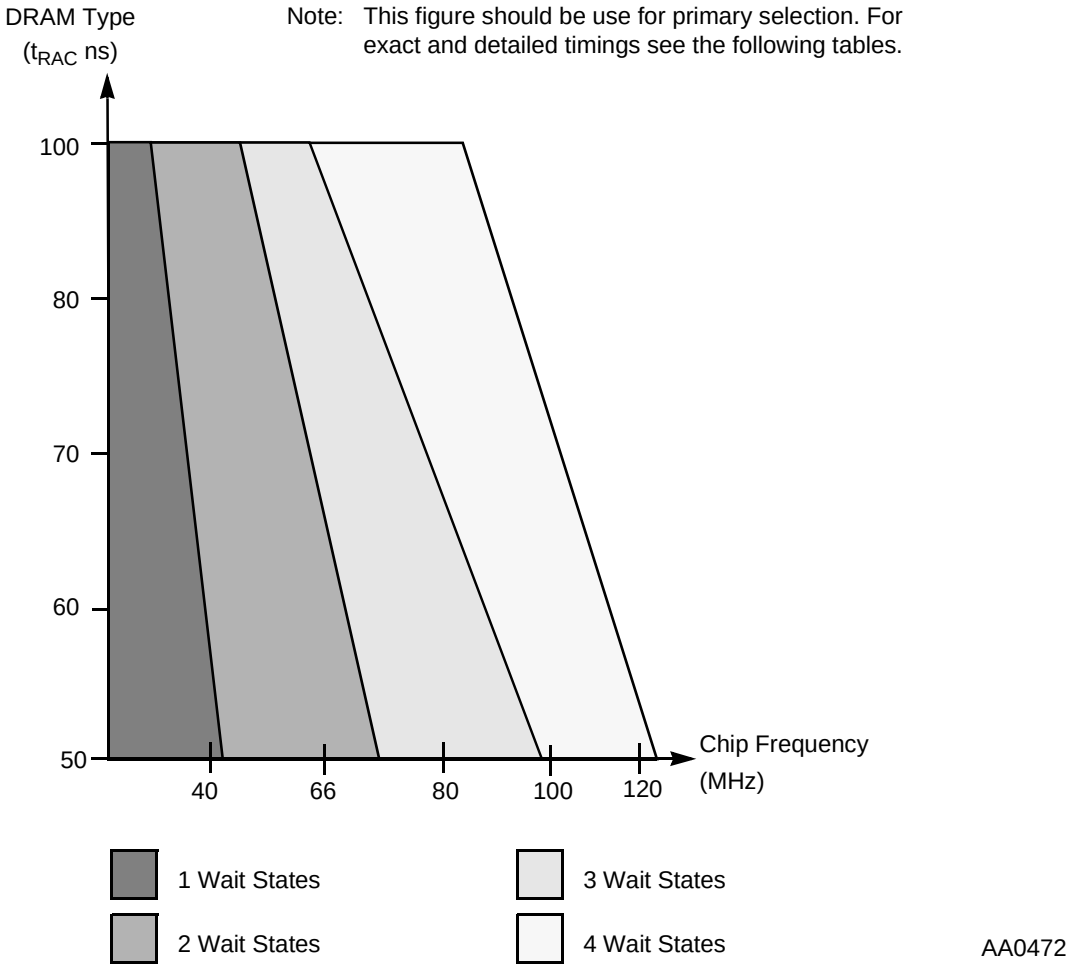


Figure 3-11 DRAM Page Mode Wait States Selection Guide

Table 3-9 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses	t_{PC}	$2 \times T_C$ $1.25 \times T_C$	20.0 12.5	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C$ 7.0	—	13.0	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C$ 7.0	—	23.0	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C$ 4.0	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C$ 4.0	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C$ 4.0	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1:0] = 00, 01— not applicable • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $4.75 \times T_C$ 6.0 $6.75 \times T_C$ 6.0	 41.5 61.5	 — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C$ 4.0	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	T_C 4.0	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C$ 4.0	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C$ 4.0	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C$ 4.0	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C$ 4.0	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C$ 4.2	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C$ 4.5	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C$ 4.3	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C$ 4.3	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C$ 4.0	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C$ 4.0	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C$ 4.3	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C$ 4.0	31.0	—	ns

Table 3-9 DRAM Page Mode Timings, Three Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C$ 7.0	—	18.0	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C$ 0.3	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56367.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals 4 × TC for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.

6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-10 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses	t_{PC}	 $5 \times T_C$ $4.5 \times T_C$	 50.0 45.0	 — —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.75 \times T_C$ 5.7	—	21.8	ns
133	Column address valid to data valid (read)	t_{AA}	$3.75 \times T_C$ 5.7	—	31.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C$ 4.0	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C$ 4.0	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C$ 4.0	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1–0] = 00, 01—Not applicable • BRW[1–0] = 10 • BRW[1–0] = 11	t_{CRP}	 — $5.25 \times T_C$ 6.0 $7.25 \times T_C$ 6.0	 — 46.5 66.5	 — — —	 — ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C$ 4.0	16.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	T_C 4.0	6.0	—	ns

Table 3-10 DRAM Page Mode Timings, Four Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	100 MHz		Unit
				Min	Max	
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C$ 4.0	31.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C$ 4.0	46.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C$ 4.0	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 3.7$	8.8	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C$ 4.2	28.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C$ 4.5	40.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C$ 4.3	43.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C$ 4.3	33.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.5$	0.5	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C$ 4.0	31.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C$ 4.3	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C$ 4.0	41.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$3.25 \times T_C$ 5.7	—	26.8	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56367.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences). An expressions is used to calculate the maximum or minimum value listed, as appropriate.

5 BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

6 $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

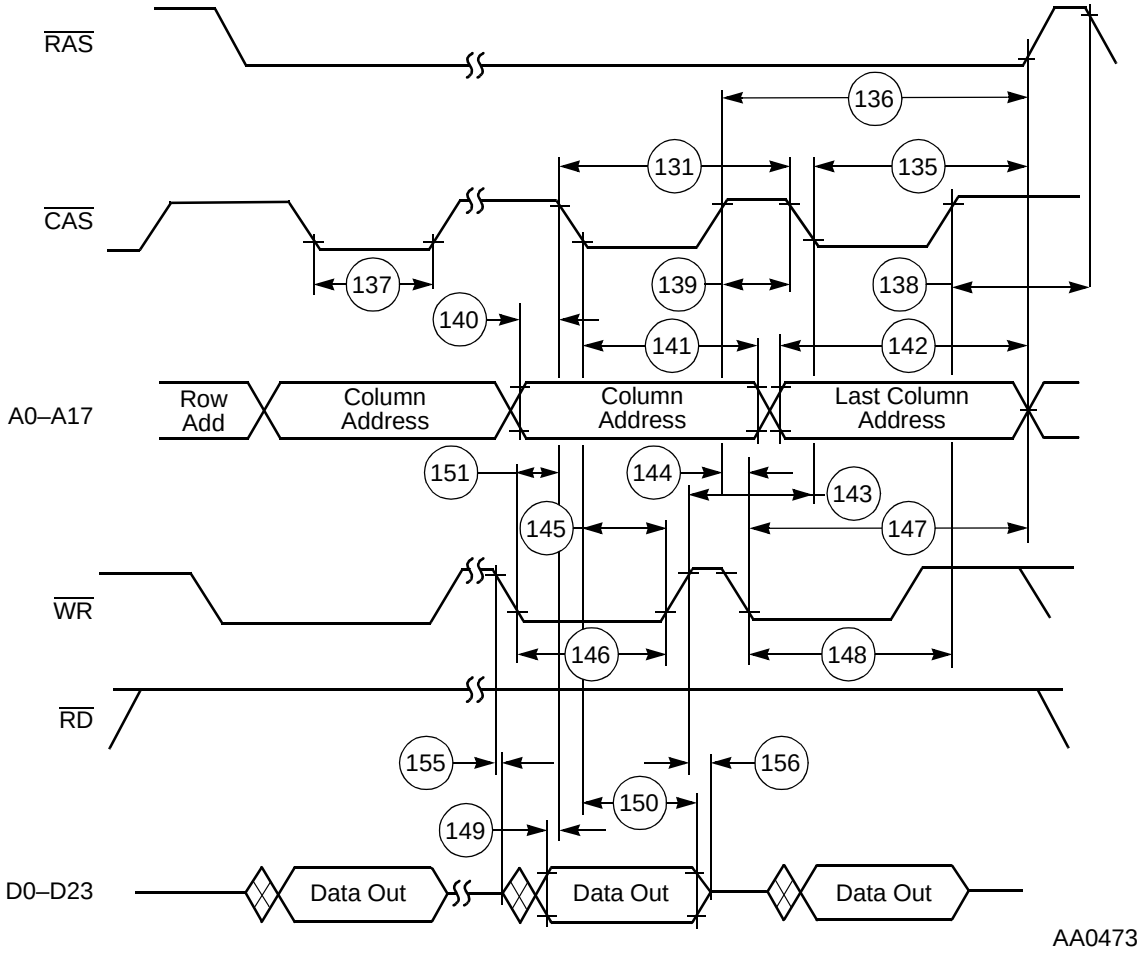


Figure 3-12 DRAM Page Mode Write Accesses

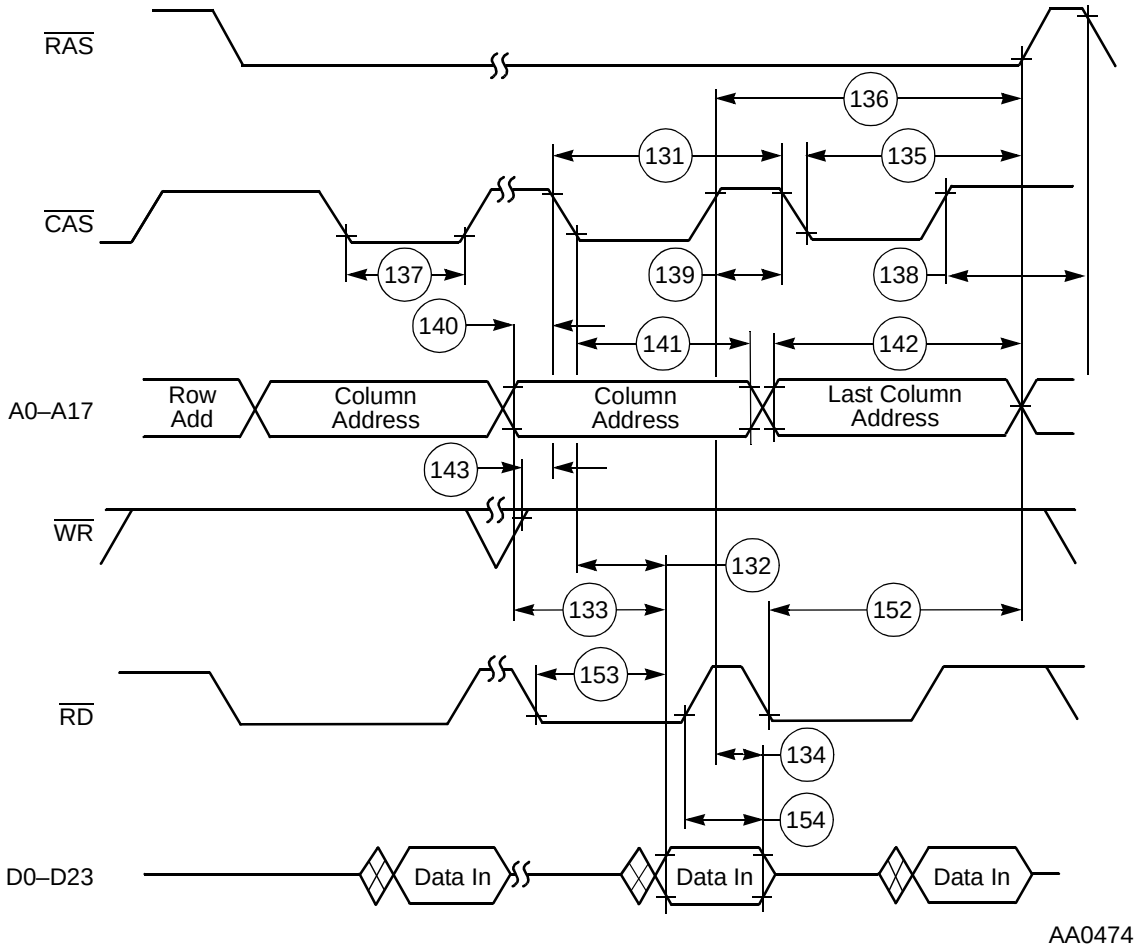


Figure 3-13 DRAM Page Mode Read Accesses

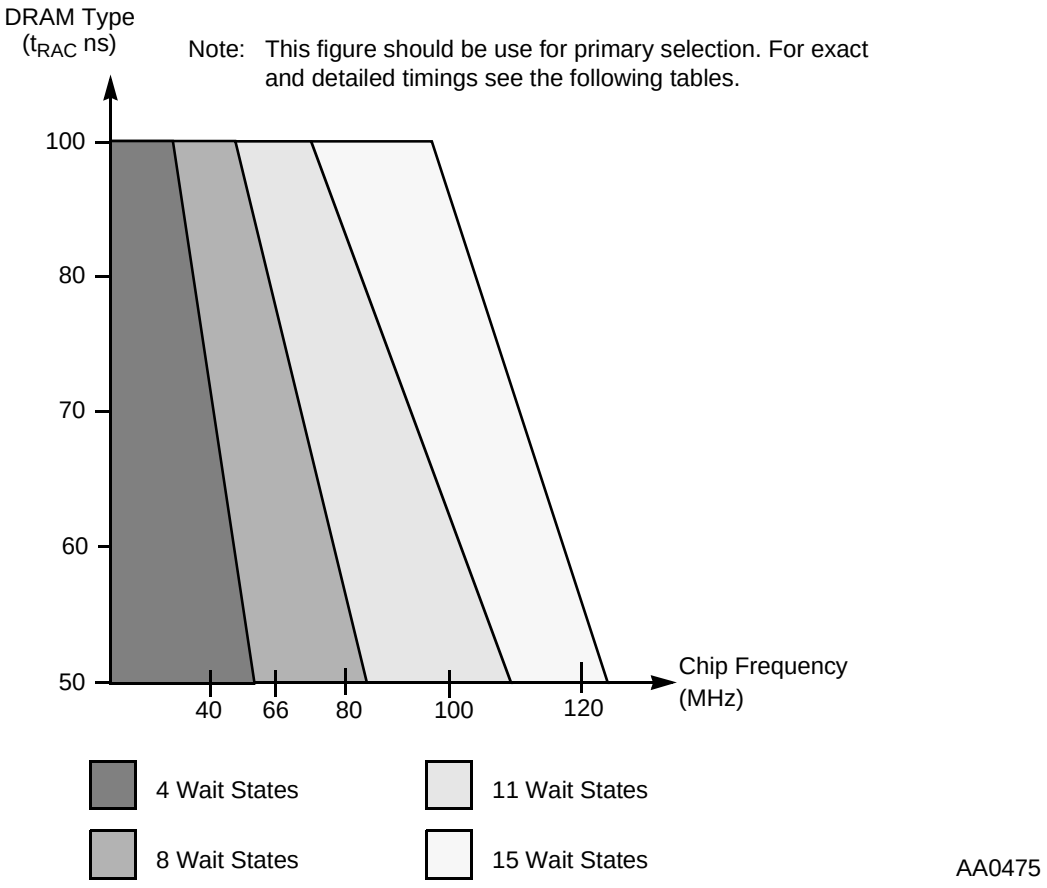


Figure 3-14 DRAM Out-of-Page Wait States Selection Guide

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C$ 7.5	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C$ 7.5	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C$ 7.5	—	67.5	—	42.5	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C$ 4.0	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C$ 4.0	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C$ 4.0	83.5	—	54.3	—	ns

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	2.75 × T_C 4.0	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	1.25 × T_C 4.0	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	1.5 × T_C 2	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	1.25 × T_C 2	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	2.25 × T_C 4.0	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	1.75 × T_C 4.0	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	1.75 × T_C 4.0	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	1.25 × T_C 4.0	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	0.25 × T_C 4.0	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	1.75 × T_C 4.0	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	3.25 × T_C 4.0	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	2 × T_C 4.0	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	1.5 × T_C 3.8	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	0.75 × T_C 3.7	33.8	—	21.3	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	0.25 × T_C 3.7	8.8	—	4.6	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	1.5 × T_C 4.2	70.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	3 × T_C 4.2	145.8	—	95.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	4.5 × T_C 4.5	220.5	—	145.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	4.75 × T_C 4.3	233.2	—	154.0	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	4.25 × T_C 4.3	208.2	—	137.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	2.25 × T_C 4.0	108.5	—	71.0	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	1.75 × T_C 4.0	83.5	—	54.3	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	3.25 × T_C 4.0	158.5	—	104.3	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	3 × T_C 4.3	145.7	—	95.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	0.5 × T_C 4.0	21.0	—	12.7	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	1.25 × T_C 4.0	58.5	—	37.7	—	ns

Table 3-11 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics	Symbol	Expression	20 MHz[3]		30 MHz[3]		Unit
				Min	Max	Min	Max	
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	4.5 × T_C 4.0	221.0	—	146.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	4 × T_C 7.5	—	192.5	—	125.8	ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		0.75 × T_C 0.3	37.2	—	24.7	—	ns
195	$\overline{WR}$ deassertion to data high impedance		0.25 × T_C	—	12.5	—	8.3	ns

1 The number of wait states for out of page access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (Figure 3-14).

4 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-12 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	12 × T_C	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	6.25 × T_C 7.0	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	3.75 × T_C 7.0	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	4.5 × T_C 7.0	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	4.25 × T_C 4.0	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	7.75 × T_C 4.0	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	5.25 × T_C 4.0	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	6.25 × T_C 4.0	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	3.75 × T_C 4.0	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	2.5 × T_C 4.0	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	1.75 × T_C 4.0	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	5.75 × T_C 4.0	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	4.25 × T_C 4.0	38.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	4.25 × T_C 4.0	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	1.75 × T_C 4.0	13.5	—	ns

Table 3-12 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression	100 MHz		Unit
				Min	Max	
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	0.75 × T_C 4.0	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	5.25 × T_C 4.0	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	7.75 × T_C 4.0	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	6 × T_C 4.0	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	3.0 × T_C 4.0	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	1.75 × T_C 4.0	13.5	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	0.25 × T_C 2.0	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	5 × T_C 4.2	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	7.5 × T_C 4.2	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	11.5 × T_C 4.5	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	11.75 × T_C 4.3	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	10.25 × T_C 4.3	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	5.75 × T_C 4.0	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	5.25 × T_C 4.0	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	7.75 × T_C 4.0	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	6.5 × T_C 4.3	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	1.5 × T_C 4.0	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	2.75 × T_C 4.0	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	11.5 × T_C 4.0	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	10 × T_C 7.0	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[5]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		0.75 × T_C 0.3	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		0.25 × T_C	—	2.5	ns

1 The number of wait states for out-of-page access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56367.

4 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

5 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-13 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$8.25 \times T_C$ 5.7	—	76.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$4.75 \times T_C$ 5.7	—	41.8	ns
160	Column address valid to data valid (read)	t_{AA}	$5.5 \times T_C$ 5.7	—	49.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C$ 4.0	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C$ 4.0	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C$ 4.0	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C$ 4.0	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C$ 4.0	43.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C$ 2	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C$ 2	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C$ 4.0	73.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 6.0$	56.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C$ 4.0	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C$ 4.0	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C$ 4.0	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C$ 4.0	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C$ 4.0	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C$ 4.0	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C$ 3.8	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RRH}	$0.25 \times T_C$ 2.0	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C$ 4.2	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C$ 4.2	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C$ 4.5	150.5	—	ns

Table 3-13 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (continued)

No.	Characteristics	Symbol	Expression[3]	100 MHz		Unit
				Min	Max	
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C$ 4.3	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C$ 4.3	138.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C$ 4.0	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C$ 4.0	58.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C$ 4.0	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C$ 4.3	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C$ 4.0	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C$ 4.0	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C$ 4.0	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$14 \times T_C$ 5.7	—	134.3	ns
193	$\overline{RD}$ deassertion to data not valid[5]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 1.5$	6.0	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for an out-of-page access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 An expression is used to compute the maximum or minimum value listed (or both if the expression includes ±).

4 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

5 $\overline{RD}$ deassertion always occurs after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

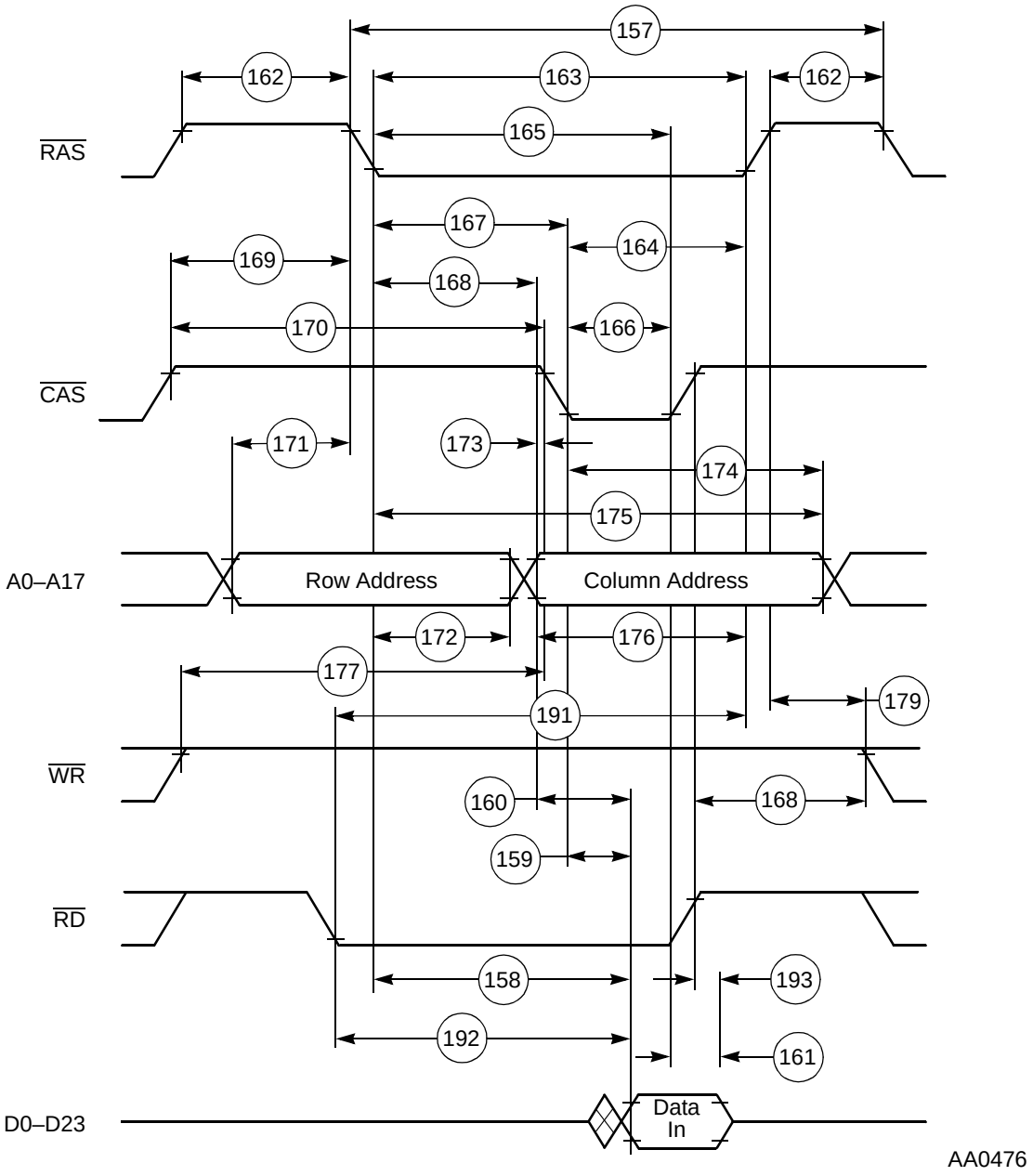


Figure 3-15 DRAM Out-of-Page Read Access

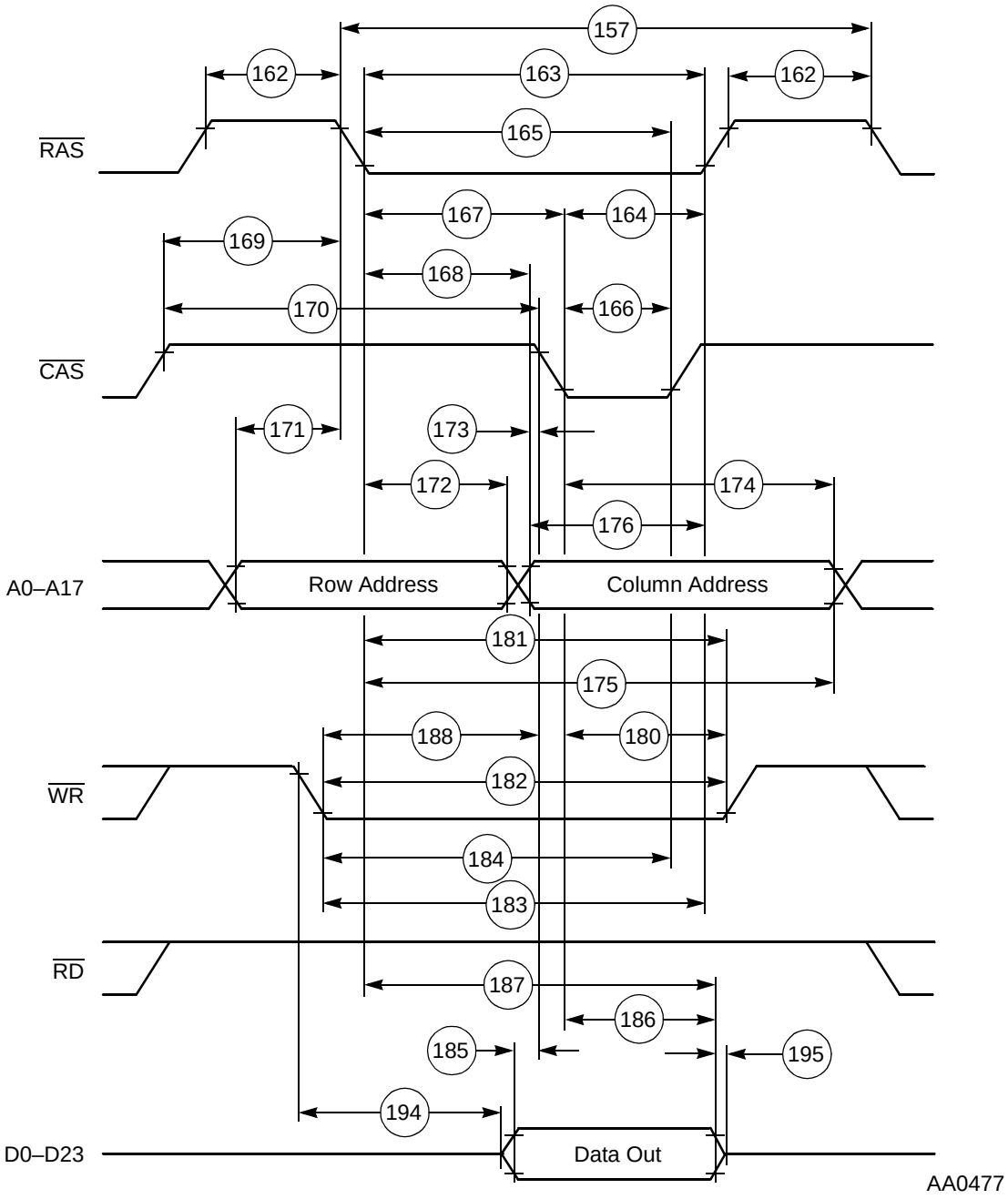


Figure 3-16 DRAM Out-of-Page Write Access

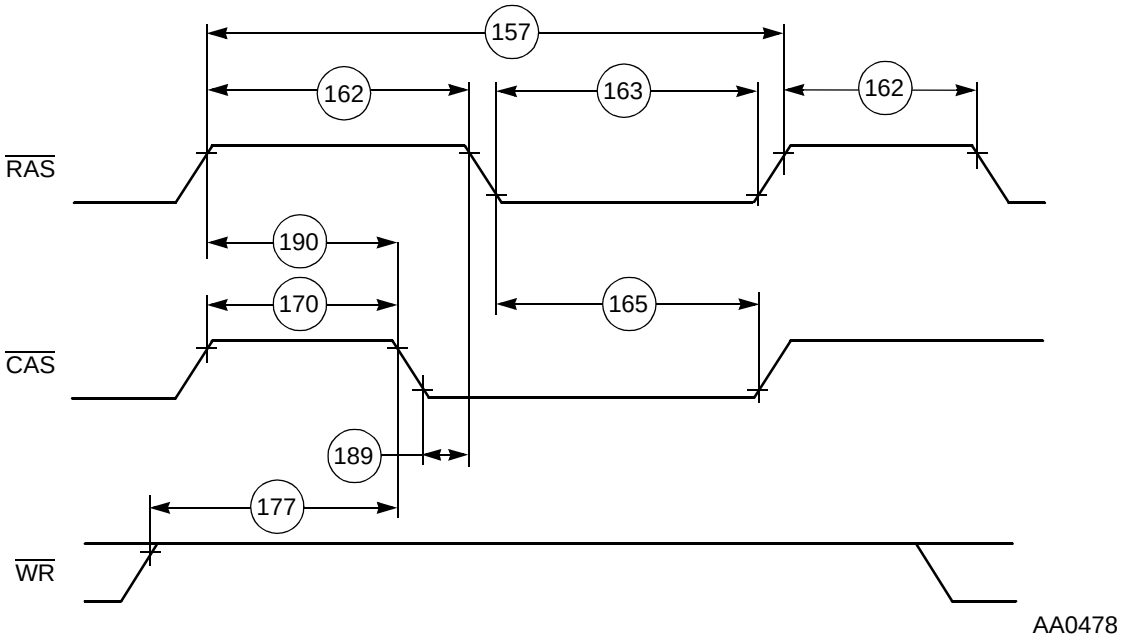


Figure 3-17 DRAM Refresh Access

3.10.3 Arbitration Timings

Table 3-14 Asynchronous Bus Arbitration Timing[1, 2, 3]

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input negation.	2 .5* Tc + 5	—	21.7	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 * Tc + 5	18.3	—	ns

1 Bit 13 in the OMR register must be set to enter Asynchronous Arbitration mode.

2 If Asynchronous Arbitration mode is active, none of the timings in Table 3-14 is required.

3 In order to guarantee timings 250, and 251, it is recommended to assert $\overline{BG}$ inputs to different 56300 devices (on the same bus) in a non overlap manner as shown in Figure 3-18.

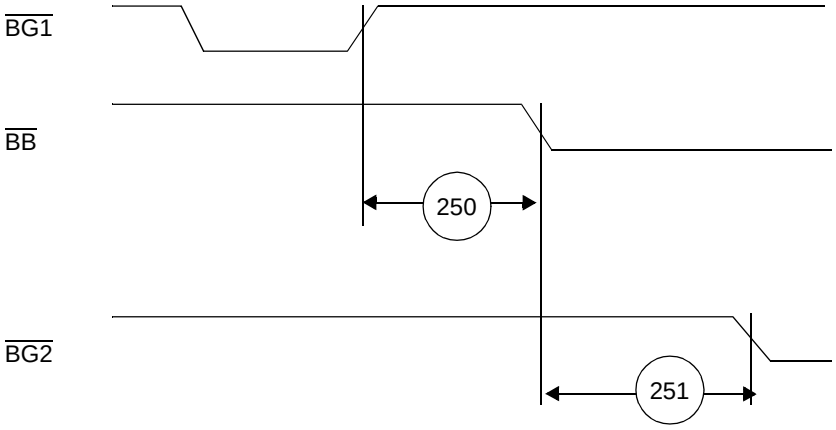


Figure 3-18 Asynchronous Bus Arbitration Timing

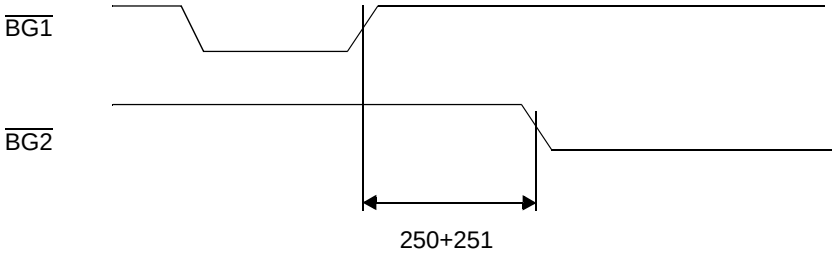


Figure 3-19 Asynchronous Bus Arbitration Timing

3.10.4 Background explanation for Asynchronous Bus Arbitration:

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a 56300 part may assume mastership and assert $\overline{BB}$ for some time after $\overline{BG}$ is negated. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other 56300 components which are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, a situation of $\overline{BG}$ asserted, and $\overline{BB}$ negated, may cause another 56300 component to assume mastership at the same time. Therefore some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that such a situation is avoided.

3.11 Parallel Host Interface (HDI08) Timing

Table 3-15 Host Interface (HDI08) Timing[1, 2, 3]

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[4] $\overline{\text{HACK}}$ read assertion width	$T_C + 9.9$	16.7	—	ns
318	Read data strobe deassertion width[4] $\overline{\text{HACK}}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[4] after "Last Data Register" reads[5, 6], or between two consecutive CVR, ICR, or ISR reads[7] $\overline{\text{HACK}}$ deassertion width after "Last Data Register" reads[5, 6]	$2.5 \times T_C + 6.6$	23.3	—	ns
320	Write data strobe assertion width[8] $\overline{\text{HACK}}$ write assertion width	—	13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{\text{HACK}}$ write deassertion width • after ICR, CVR and "Last Data Register" writes[5] • after IVR writes, or • after TXH:TXM writes (with HBE=0), or • after TXL:TXM writes (with HBE=1)	$2.5 \times T_C + 6.6$	 23.3 16.5	 — —	ns
322	$\overline{\text{HAS}}$ assertion width	—	9.9	—	ns
323	$\overline{\text{HAS}}$ deassertion to data strobe assertion[9]	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[8] Host data input setup time before $\overline{\text{HACK}}$ write deassertion	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[8] Host data input hold time after $\overline{\text{HACK}}$ write deassertion	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[4] $\overline{\text{HACK}}$ read assertion to output data active from high impedance	—	3.3	—	ns
327	Read data strobe assertion to output data valid[4] $\overline{\text{HACK}}$ read assertion to output data valid	—	—	24.2	ns
328	Read data strobe deassertion to output data high impedance[4] $\overline{\text{HACK}}$ read deassertion to output data high impedance	—	—	9.9	ns
329	Output data hold time after read data strobe deassertion[4] Output data hold time after $\overline{\text{HACK}}$ read deassertion	—	3.3	—	ns
330	$\overline{\text{HCS}}$ assertion to read data strobe deassertion[4]	$T_C + 9.9$	16.7	—	ns
331	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[8]	—	9.9	—	ns

Table 3-15 Host Interface (HDI08) Timing[1, 2, 3] (continued)

No.	Characteristics	Expression	150 MHz		Unit
			Min	Max	
332	$\overline{HCS}$ assertion to output data valid	—	—	19.1	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[9]	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[9] • Read • Write	— —	 0 4.7	 — —	ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[9]	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[4, 5, 10]	T_C	6.7	—	ns
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5, 8, 10]	$2 \times T_C$	13.4	—	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[5, 9, 10]	—	—	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[5, 9, 10, 11]	—	—	300.0	ns
342	Delay from DMA $\overline{HACK}$ deassertion to HOREQ assertion • For “Last Data Register” read[5] • For “Last Data Register” write[5] • For other cases	 $2 \times T_C + 19.1$ $1.5 \times T_C + 19.1$	 32.5 29.2 0.0	 — — —	ns
343	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion • HROD = 0[5]	—	—	20.2	ns
344	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[5, 11]	—	—	300.0	ns

1 See Host Port Usage Considerations in the DSP56367 User’s Manual.

2 In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.

3 V_{CC} = 1.8 V ± 5%; T_J = –40°C to +95°C, C_L = 50 pF

4 The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.

5 The “last data register” is the register at address $7, which is the last location to be read or written in data transfers.

6 This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.

7 This timing is applicable only if two consecutive reads from one of these registers are executed.

8 The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.

9 The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.

10 The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.

11 In this calculation, the host request signal is pulled up by a 4.7 k resistor in the open-drain mode.

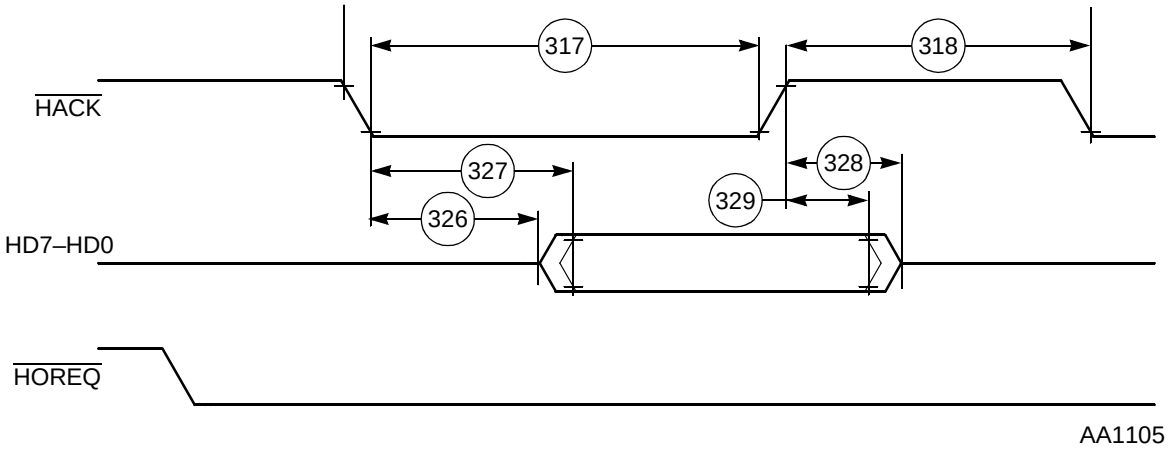


Figure 3-20 Host Interrupt Vector Register (IVR) Read Timing Diagram

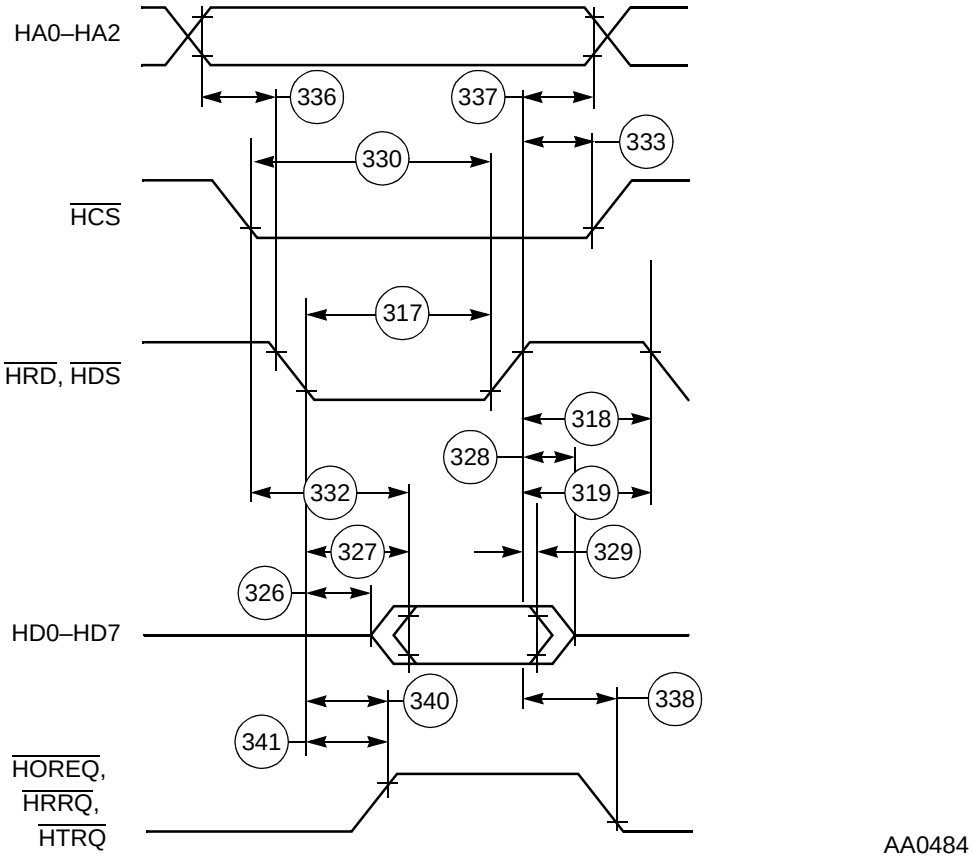


Figure 3-21 Read Timing Diagram, Non-Multiplexed Bus

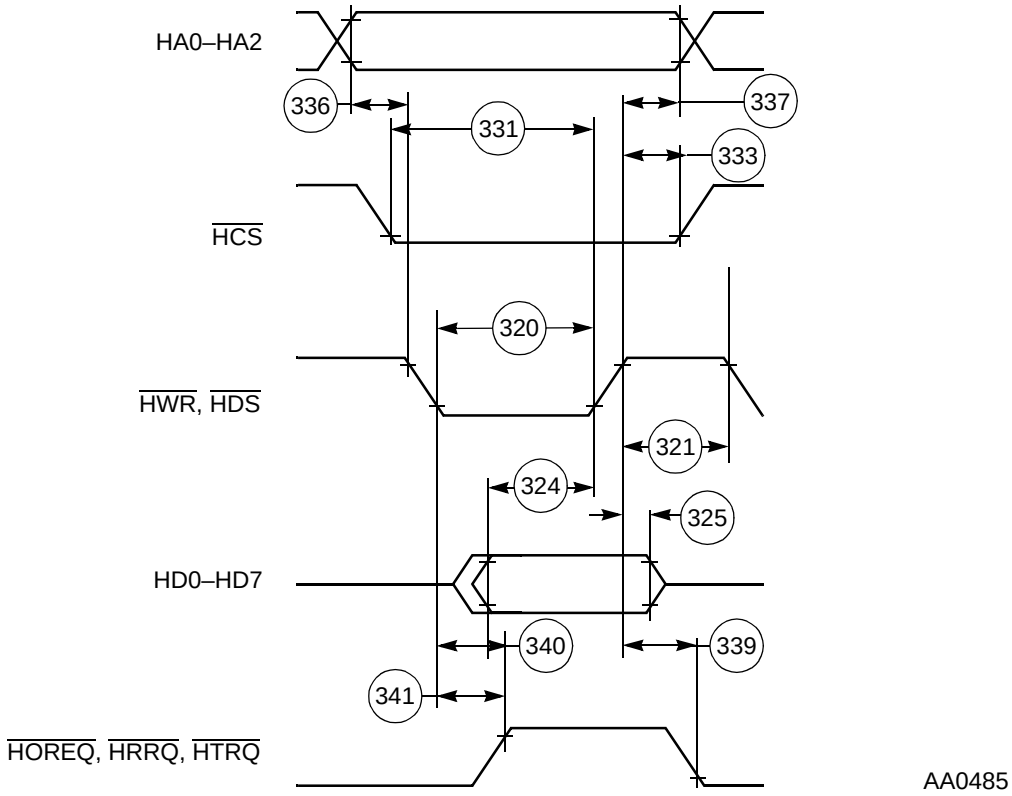


Figure 3-22 Write Timing Diagram, Non-Multiplexed Bus

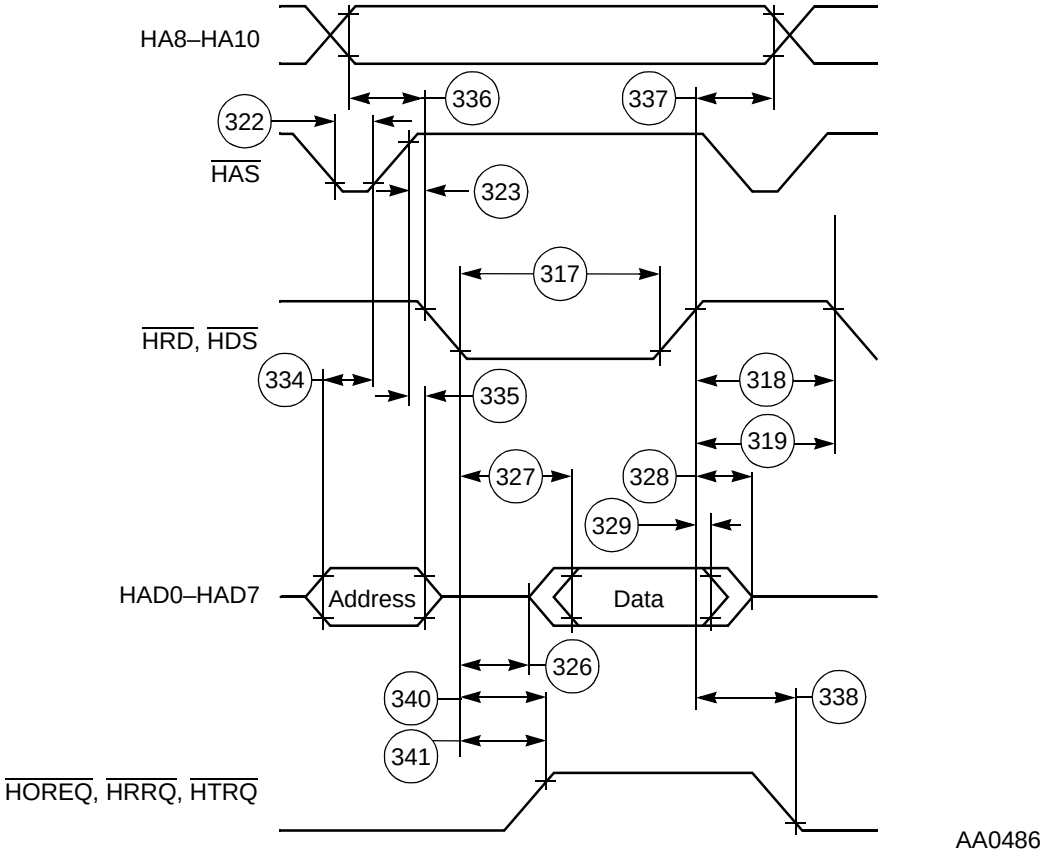


Figure 3-23 Read Timing Diagram, Multiplexed Bus

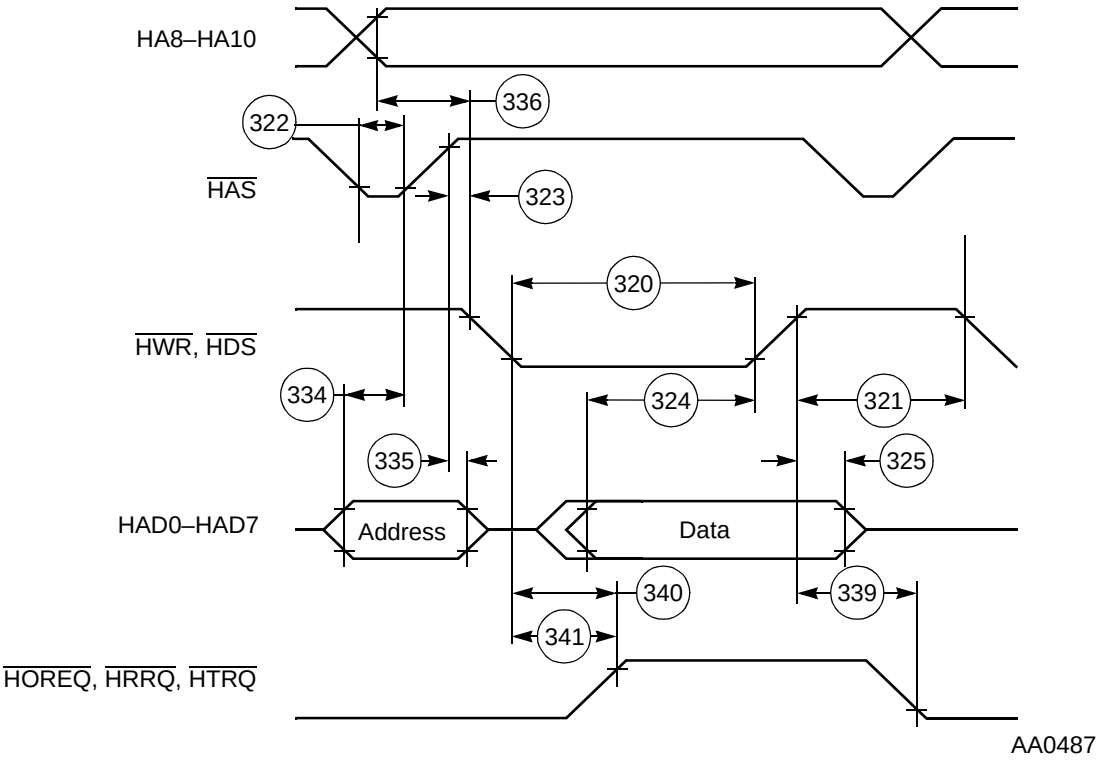


Figure 3-24 Write Timing Diagram, Multiplexed Bus

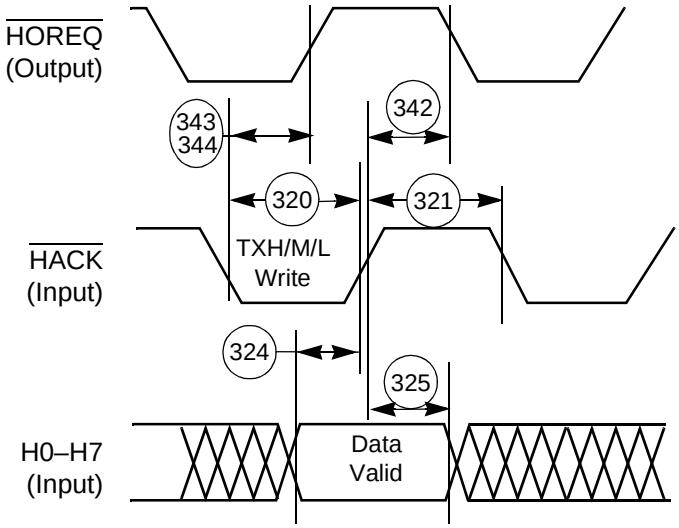


Figure 3-25 Host DMA Write Timing Diagram

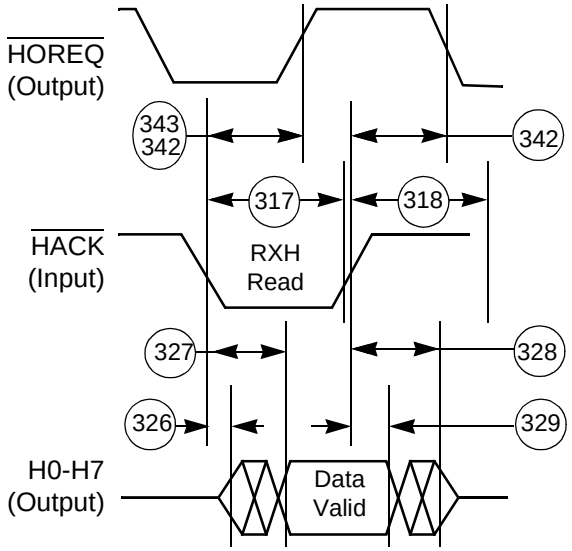


Figure 3-26 Host DMA Read Timing Diagram

3.12 Serial Host Interface SPI Protocol Timing

Table 3-16 Serial Host Interface SPI Protocol Timing

No.	Characteristics[1]	Mode	Filter Mode	Expression[2]	Min	Max	Unit
140	Tolerable spike width on clock or data in	—	Bypassed	—	—	0	ns
			Narrow	—	—	50	
			Wide	—	—	100	
141	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	6 × TC+46	86.2	—	ns
			Narrow	6 × T_C+152	192.2	—	
			Wide	6 × T_C+223	263.2	—	
142	Serial clock high period	Master	Bypassed	0.5 × t_{SPICC} –10	38	—	ns
			Narrow	0.5 × t_{SPICC} –10	91	—	
			Wide	0.5 × t_{SPICC} –10	126.5	—	
		Slave	Bypassed	2.5 × T_C + 12	28.8	—	ns
			Narrow	2.5 × T_C + 102	118.8	—	
			Wide	2.5 × T_C + 189	205.8	—	
143	Serial clock low period	Master	Bypassed	0.5 × t_{SPICC} –10	38	—	ns
			Narrow	0.5 × t_{SPICC} –10			
			Wide	0.5 × t_{SPICC} –10			
		Slave	Bypassed	2.5 × T_C + 12	28.8	—	ns
			Narrow	2.5 × T_C + 102	118.8	—	
			Wide	2.5 × T_C + 189	205.8	—	

Table 3-16 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1]	Mode	Filter Mode	Expression[2]	Min	Max	Unit
144	Serial clock rise/fall time	Master Slave	— —	— —	— —	10 2000	ns
146	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed Narrow Wide	$3.5 \times T_C + 15$ 0 0	38.5 0 0	— — —	ns
	CPHA = 1	Slave	Bypassed Narrow Wide	10 0 0	10 0 0	— — —	ns
147	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed Narrow Wide	12 102 189	12 102 189	— — —	ns
148	Data input valid to SCK edge (data input set-up time)	Master/ Slave	Bypassed Narrow Wide	0 $MAX\{(20-T_C), 0\}$ $MAX\{(40-T_C), 0\}$	0 13.3 33.3	— — —	ns
149	SCK last sampling edge to data input not valid	Master/ Slave	Bypassed Narrow Wide	$2.5 \times T_C + 10$ $2.5 \times T_C + 30$ $2.5 \times T_C + 50$	26.8 46.8 66.8	— — —	ns
150	$\overline{SS}$ assertion to data out active	Slave	—	2	2	—	ns
151	$\overline{SS}$ deassertion to data high impedance[3]	Slave	—	9	—	9	ns
152	SCK edge to data out valid (data out delay time)	Master/ Slave	Bypassed Narrow Wide	$2 \times T_C + 33$ $2 \times T_C + 123$ $2 \times T_C + 210$	— — —	46.4 136.4 223.4	ns
153	SCK edge to data out not valid (data out hold time)	Master/ Slave	Bypassed Narrow Wide	$T_C + 5$ $T_C + 55$ $T_C + 106$	11.7 61.7 112.7	— — —	ns
154	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	$T_C + 33$	—	39.7	ns
157	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed Narrow Wide	$2.5 \times T_C + 30$ $2.5 \times T_C + 120$ $2.5 \times T_C + 217$	— — —	46.8 136.8 233.8	ns
158	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed Narrow Wide	$2.5 \times T_C + 30$ $2.5 \times T_C + 80$ $2.5 \times T_C + 136$	46.8 96.8 152.8	— — —	ns
159	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$2.5 \times T_C + 30$	46.8	—	ns

Table 3-16 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1]	Mode	Filter Mode	Expression[2]	Min	Max	Unit
160	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	$T_C + 6$	12.7	—	ns
161	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed Narrow Wide	$0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$ $0.5 \times t_{SPICC} + 2.5 \times T_C + 43$	97.8 160.8 196.8	— — —	ns
162	$\overline{HREQ}$ in deassertion to last SCK sampling edge ($\overline{HREQ}$ in set-up time) (CPHA = 1)	Master	—	0	0	—	ns
163	First SCK edge to $\overline{HREQ}$ in not asserted ($\overline{HREQ}$ in hold time)	Master	—	0	0	—	ns

1 V_{CC} = 1.8 V ± 5%; T_J = –40°C to +95°C, C_L = 50 pF

2 The timing values calculated are based on simulation data at 150MHz. Tester restrictions limit SHI testing to lower clock frequencies.

3 Periodically sampled, not 100% tested

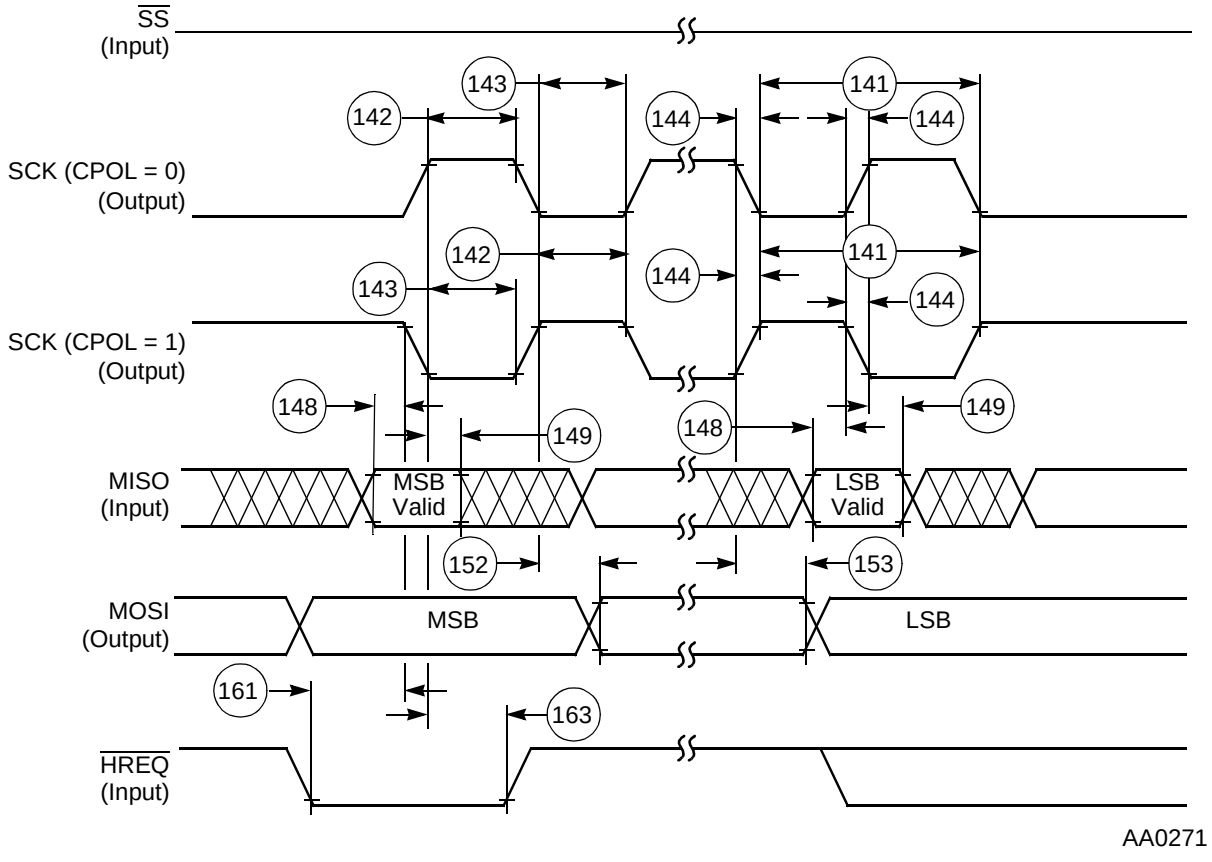


Figure 3-27 SPI Master Timing (CPHA = 0)

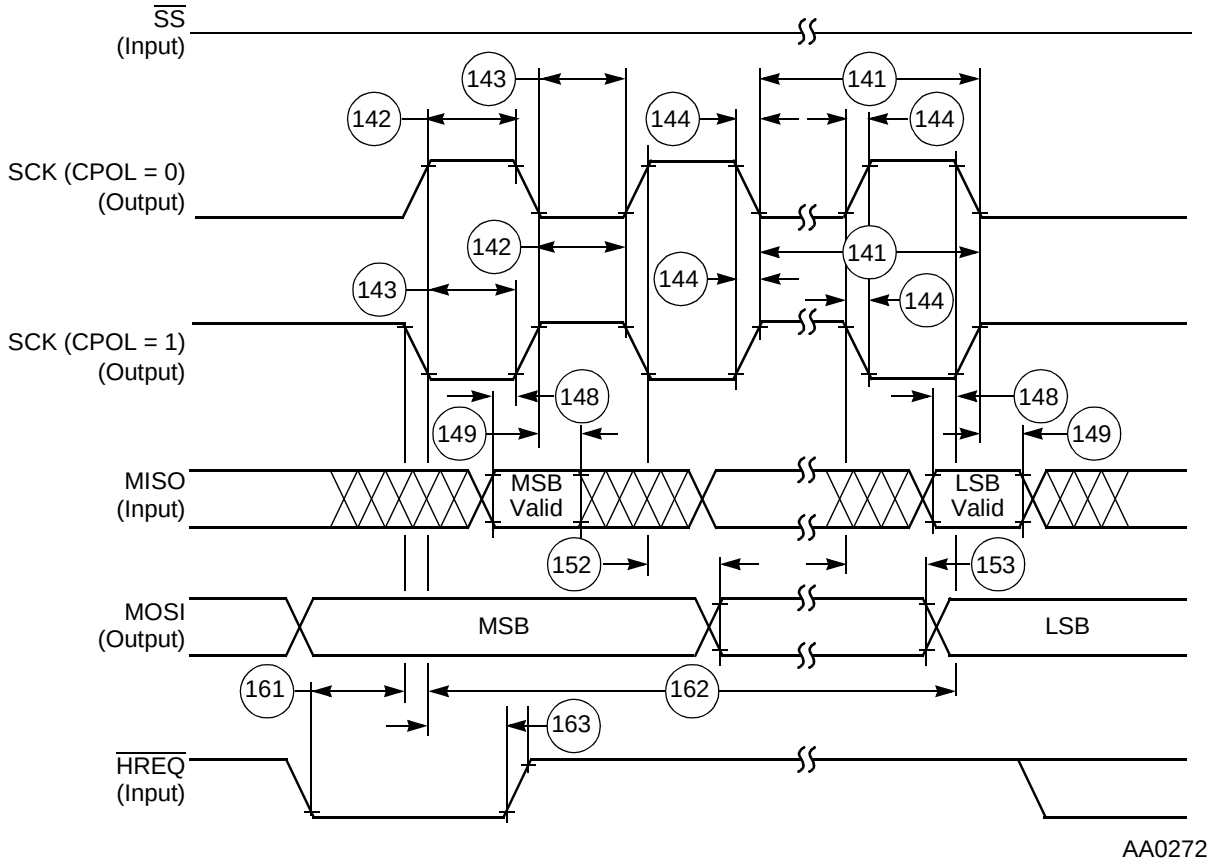


Figure 3-28 SPI Master Timing (CPHA = 1)

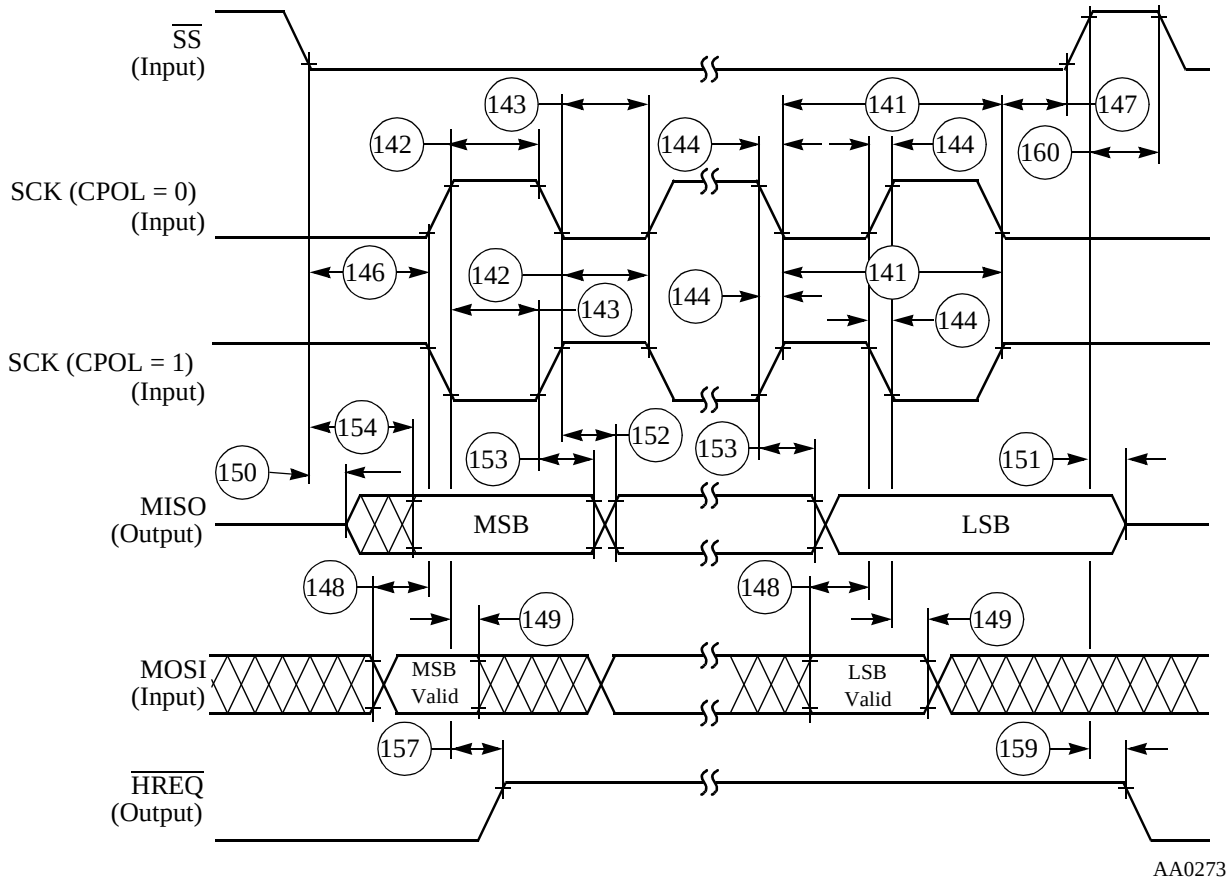


Figure 3-29 SPI Slave Timing (CPHA = 0)

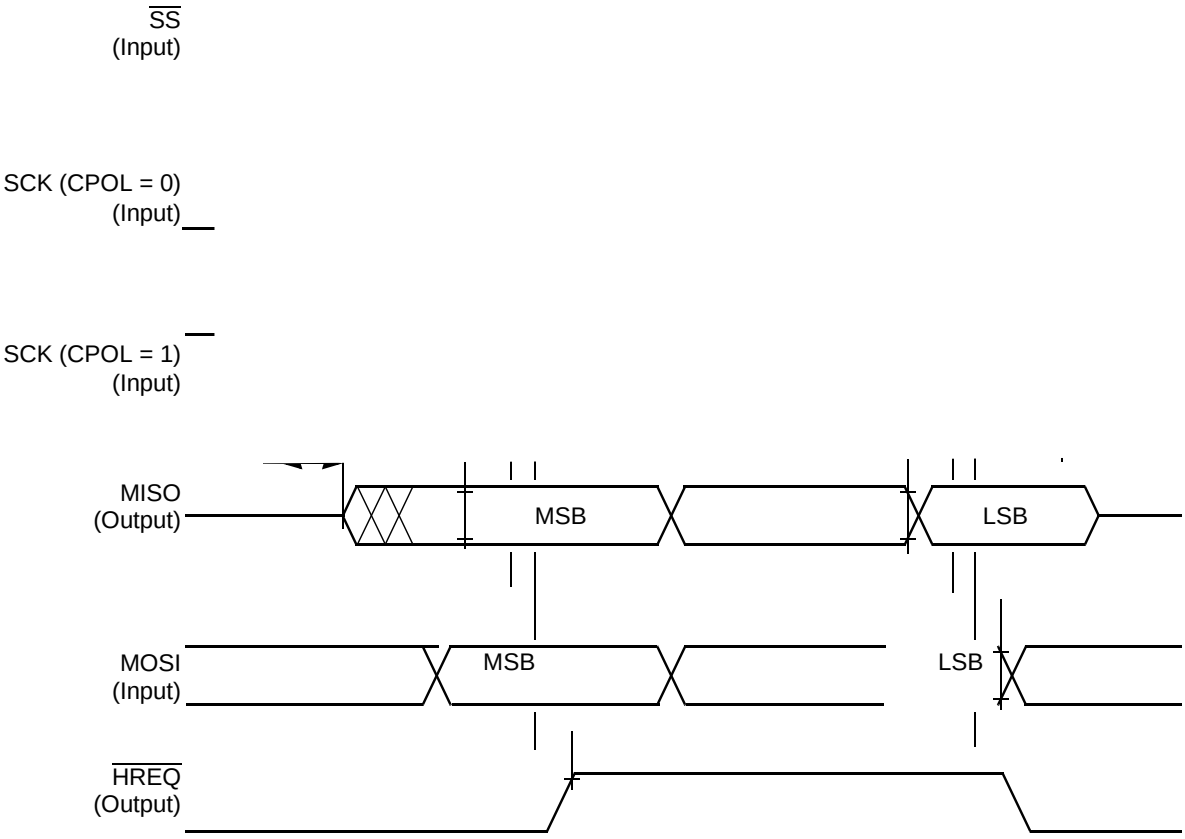


Figure 3-30 SPI Slave Timing (CPHA = 1)

3.13 Serial Host Interface (SHI) I²C Protocol Timing

Table 3-17 SHI I²C Protocol Timing

Standard I²C							
No.	Characteristics[1, 2, 3]	Symbol/ Expression	Standard[4, 5]		Fast-Mode[5, 6]		Unit
			Min	Max	Min	Max	
	Tolerable spike width on SCL or SDA • Filters bypassed • Narrow filters enabled • Wide filters enabled	—	 — — —	 0 50 100	 — — —	 0 50 100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
171	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs