
PIC12LF1840T39A Product Brief

High-Performance RISC CPU:

- Only 49 Instructions to Learn:
 - All single-cycle instructions except branches
- Operating Speed:
 - DC – 32 MHz oscillator/clock input
 - DC – 125 ns instruction cycle
- Interrupt Capability with Automatic Context Saving
- 16-Level Deep Hardware Stack with Optional Overflow/Underflow Reset
- Direct, Indirect and Relative Addressing modes:
 - Two full 16-bit File Select Registers (FSRs)
 - FSRs can read program and data memory

Flexible Oscillator Structure:

- Precision 32 MHz Internal Oscillator Block:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequencies range of 31 kHz to 32 MHz
- 31 kHz Low-Power Internal Oscillator
- Four Crystal modes up to 32 MHz
- Three External Clock modes up to 32 MHz
- 4x Phase Lock Loop (PLL)
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up
- Reference Clock module:
 - Programmable clock output frequency and duty-cycle

Special Microcontroller Features:

- 1.8V-3.6V Operation
- Self-Reprogrammable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Enhanced Low-Voltage Programming (LVP)
- Programmable Code Protection
- Power-Saving Sleep mode

Low-Power Features:

- Standby Current:
 - 30 nA @ 3.0V, typical, RF off
 - 530 nA @ 3.0V, typical, RF Sleep
- Operating Current:
 - 0.67 mA @ 8 MHz, 3.0V, RF off, typical
 - 9.67 mA @ 8 MHz, 3.0V, RF on at 0 dBm, typical
 - 15.67 mA @ 8 MHz, 3.0V, RF on at +10 dBm, typical
- Low-Power Watchdog Timer Current:
 - 500 nA @ 3.0V, typical

RF Transmitter:

- Fully Integrated Transmitter
- FSK Operation up to 100 kbps
- OOK Operation up to 10 kbps
- Frequency-Agile Operation in 310, 433, 868 and 915 MHz Bands
- +10 dBm or 0 dBm Configurable Output Power

Analog Features:

- Analog-to-Digital Converter (ADC) module:
 - 10-bit resolution, 4 channels
 - Conversion available during Sleep
- Analog Comparator module:
 - One rail-to-rail analog comparator
 - Power mode control
 - Software controllable hysteresis
- Voltage Reference module:
 - Fixed Voltage Reference (FVR) with 1.024V and 2.048V output levels
 - 5-bit rail-to-rail resistive DAC with positive and negative reference selection

Peripheral Features:

- 5 I/O Pins and 1 Input-only Pin:
 - High current sink/source 25 mA/25 mA
 - Programmable weak pull-ups
 - Programmable interrupt-on-change pins
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
 - Dedicated, low-power 32 kHz oscillator driver
- Timer2: 8-Bit Timer/Counter with 8-Bit Period Register, Prescaler and Postscaler

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- Enhanced CCP (ECCP) module:
 - Software selectable time bases
 - Auto-shutdown and auto-restart
 - PWM steering
- Master Synchronous Serial Port (MSSP) with SPI and I²C™ with:
 - 7-bit address masking
 - SMBus/PMBus™ compatibility
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module:
 - RS-232, RS-485 and LIN compatible
 - Auto-Baud Detect
- Capacitive Sensing (CPS) module (mTouch™):
 - 4 input channels
- Data Signal Modulator module:
 - Selectable modulator and carrier sources
- SR Latch:
 - Multiple Set/Reset input options
 - Emulates 555 Timer applications

TABLE 1: PIC12LF1840T39A FEATURE SUMMARY

| Device | Program Memory Flash (words) | Data Memory EEPROM (Bytes) | Data Memory SRAM (Bytes) | I/Os ⁽¹⁾ | 10-bit ADC (ch) | CapSense (ch) | Comparators | Timers (8/16-bit) | EUSART | MSSP (I ² C™/SPI) | ECCP (Half-Bridge) | SR Latch | RF Transmitter | Debug ⁽²⁾ |
|-----------------|------------------------------|----------------------------|--------------------------|---------------------|-----------------|---------------|-------------|-------------------|--------|------------------------------|--------------------|----------|----------------|----------------------|
| PIC12LF1840T39A | 4K | 256 | 256 | 6 | 4 | 4 | 1 | 2/1 | 1 | 1 | 1 | Yes | Yes | I |

Note 1: One pin is input-only.

Note 2: I – Debugging, Integrated on Chip; H – Debugging, Debug Header Available

Note: Pin details are subject to change.

FIGURE 1: 14-PIN DIAGRAM, PIC12LF1840T39A (TSSOP)

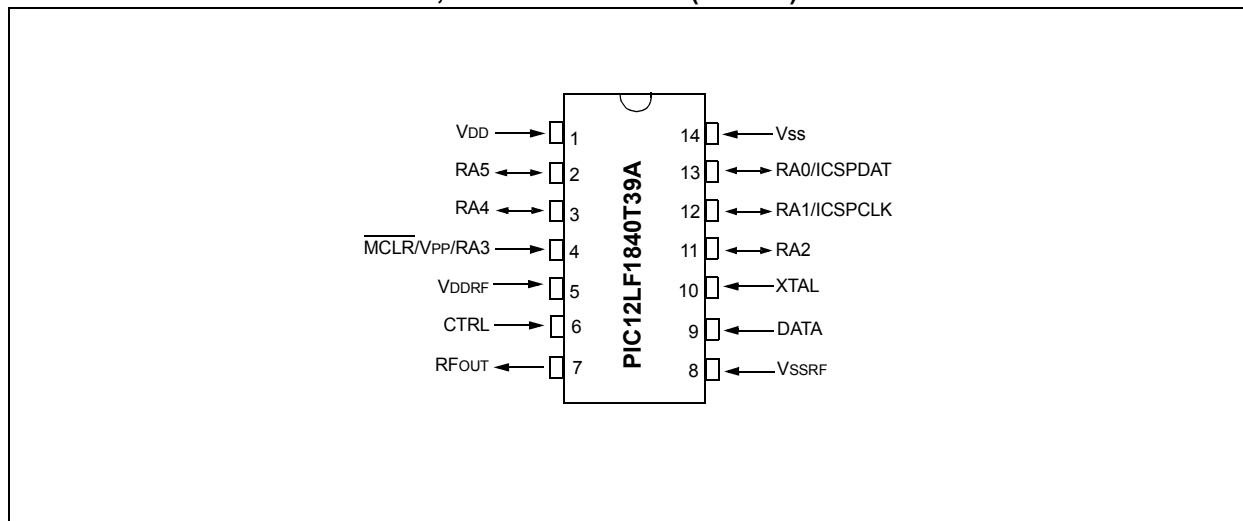


TABLE 2: 14-PIN ALLOCATION TABLE (PIC12LF1840T39A)

| I/O | 14-Pin TSSOP | A/D | Reference | CapSense | Comparator | SR Latch | Timers | ECCP | EUSART | MSSP | Interrupt | Modulator | Pull-up | Basic | RF Transmitter |
|-------|--------------|-----|-----------|----------|------------|----------|-----------------------------|---|--|---|------------|-----------|---------|------------------------|----------------|
| RA0 | 13 | AN0 | DACOUT | CPS0 | C1IN+ | — | — | P1B ⁽¹⁾ | TX ⁽¹⁾ CK ⁽¹⁾ | SDO ⁽¹⁾ SS ⁽¹⁾ | IOC | MDOUT | Y | ICSPDAT ICDDAT | — |
| RA1 | 12 | AN1 | VREF | CPS1 | C1IN0- | SRI | — | — | RX ⁽¹⁾ DT ⁽¹⁾ | SCL SCK | IOC | MDMIN | Y | ICSPCLK | — |
| RA2 | 11 | AN2 | — | CPS2 | C1OUT | SRQ | T0CKI | CCP1 ⁽¹⁾ P1A ⁽¹⁾ FLT0 | — | SDA SDI | INT IOC | MDCOM1 | Y | — | — |
| RA3 | 4 | — | — | — | — | — | T1G ⁽²⁾ | — | — | SS ⁽¹⁾ | IOC | — | Y | MCLR VPP | — |
| RA4 | 3 | AN3 | — | CPS3 | C1IN1- | — | T1G ⁽¹⁾ T1OSO | P1B ⁽¹⁾ | TX ⁽¹⁾ CK ⁽¹⁾ | SDO ⁽¹⁾ | IOC | MDCIN2 | Y | OSC2 CLKOUT CLKR | — |
| RA5 | 2 | — | — | — | — | SRNQ | T1CKI T1OSI | CCP1 ⁽¹⁾ P1A ⁽¹⁾ | RX ⁽¹⁾ DT ⁽¹⁾ | — | IOC | — | Y | OSC1 CLKIN | — |
| VDD | 1 | — | — | — | — | — | — | — | — | — | — | — | — | VDD | — |
| VSS | 14 | — | — | — | — | — | — | — | — | — | — | — | — | VSS | — |
| CTRL | 6 | — | — | — | — | — | — | — | — | — | — | — | — | — | CTRL |
| RFOUT | 7 | — | — | — | — | — | — | — | — | — | — | — | — | — | RFOUT |
| DATA | 9 | — | — | — | — | — | — | — | — | — | — | — | — | — | DATA |
| XTAL | 10 | — | — | — | — | — | — | — | — | — | — | — | — | — | XTAL |
| VDDRF | 5 | — | — | — | — | — | — | — | — | — | — | — | — | — | VDDRF |
| VSSRF | 8 | — | — | — | — | — | — | — | — | — | — | — | — | — | VSSRF |

Note 1: Pin function is selectable via the APFCON register.

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APPENDIX A: REVISION HISTORY

Revision A (03/2012)

Initial release of this document.

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