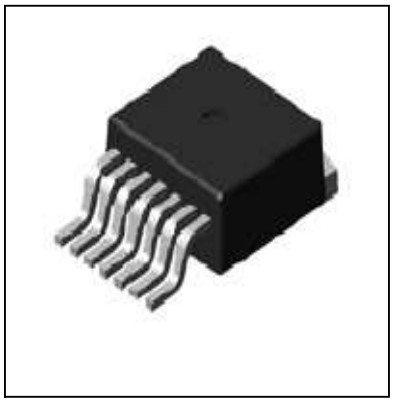
FAN7093_F085

High Current PN Half Bridge Rectifier 47 A, Max path resistance 30.5 mΩ at 150 °C

FAIRCHILD SEMICONDUCTOR®

FAN7093_F085
High Current PN Half Bridge
December 2011

1 Features



TO263-7L

- Path resistance of max. 30.5 mΩ at 150 °C
- Low quiescent current of max. 270 µA
- PWM capability of up to 60 kHz combined with active freewheeling
- Switched mode current limitation for reduced power dissipation in over current
- Current limitation level of typical 46 A
- Status flag diagnosis with low and high side current sense capability
- Over temperature shut down with latch behavior
- Shorted load protection with latch behavior
- Over voltage lock out
- Under voltage shut down
- Driver circuit with logic level inputs
- Typical slew rate of 1 V/µs with open SR pin
- Adjustable slew rates for optimized EMI

2 Brief functional Description

The FAN7093_F085 is an integrated high current half bridge for electric motor drive applications. It contains one P-channel high-side MOSFET and one N-channel low-side MOSFET with an integrated control IC in one package. With the P-channel high-side switch the need for a charge pump is eliminated and therefore minimizing EMI. Pins IN and $\overline{INH}$ are logic level inputs and control the half bridge outputs. The diagnostic current output pin IS outputs a proportional current through the half bridge MOSFETS. The IS pin output represents current for either the P-Chan or the N-Chan depending on which is active. The part is protected against short to Battery or ground, over current, over-temperature, over voltage and under voltage. The FAN7093_F085 provides a cost optimized solution for protected high current PWM motor drives with very low board space consumption.

3 Block Diagram

The FAN7093_F085 is a high current half-bridge and contains three separate chips in one package: One P-channel high-side MOSFET and one N-channel low-side MOSFET together with a control IC. All three chips are mounted on one common lead frame, using chip on chip and chip by chip technology. The power FETs are vertical MOS transistors to ensure minimum on state resistance. Using a P-channel high-side switch eliminates a charge pump and reduces EMI. A microcontroller is able to control the logic level inputs IN and $\overline{INH}$ of the half-bridge. The diagnostic pin IS is a current output stage which delivers a proportional current through the P-channel and N-channel MOSFETS depending on which is being activated with IN/$\overline{INH}$ pin forcing conditions. In case of a short to VBATT or ground the IS pin acts as an error Flag, which can be detected as a logic high level through an attached microcontroller. In an over current situation the control IC turns off the MOSFETS and retries to turn them back on after a cool down time of typical 140us. The control IC protects the MOSFETS also against over voltage, under voltage and over temperature. The dead time to prevent shoot through between P- and N- channel MOSFET is generated by the control IC too. The slew rate of the outputs can be adjusted through an external resistor connected to the SR pin. The FAN7093_F085 can be combined with other FAN7093_F085 to form Full-bridge and also 3-phase drive configurations.

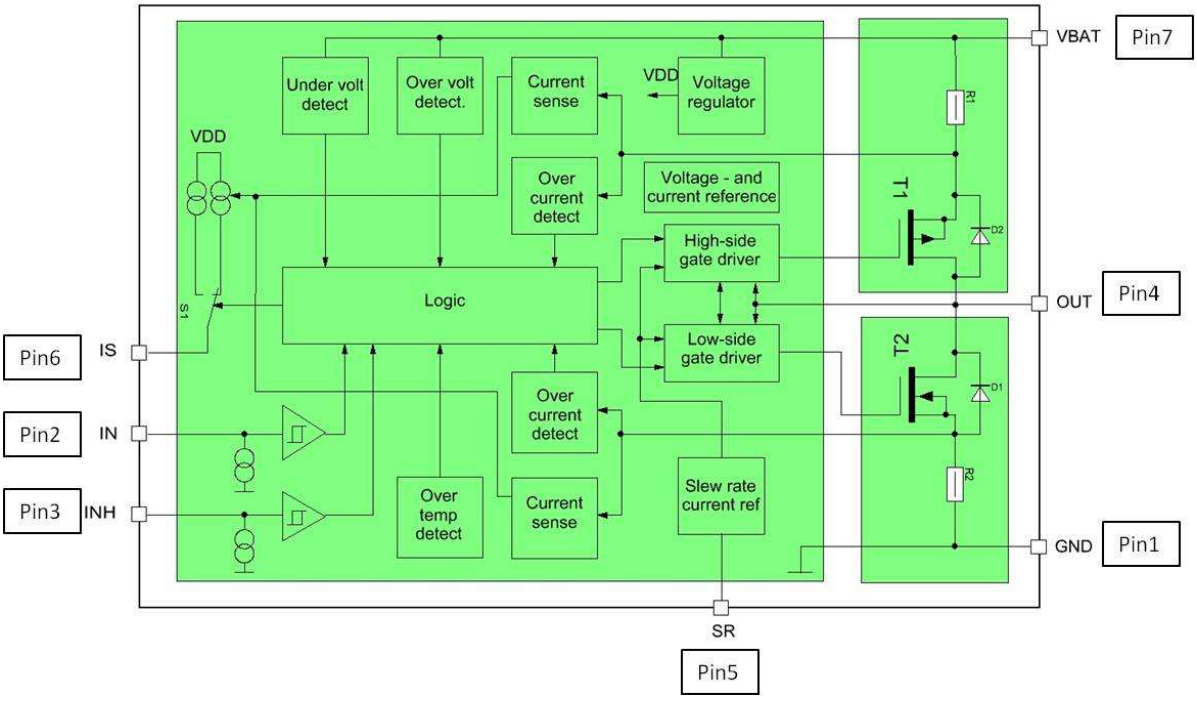


Figure 1 FAN7093_F085 Block diagram

4 Pin configuration

4.1 Pin assignment

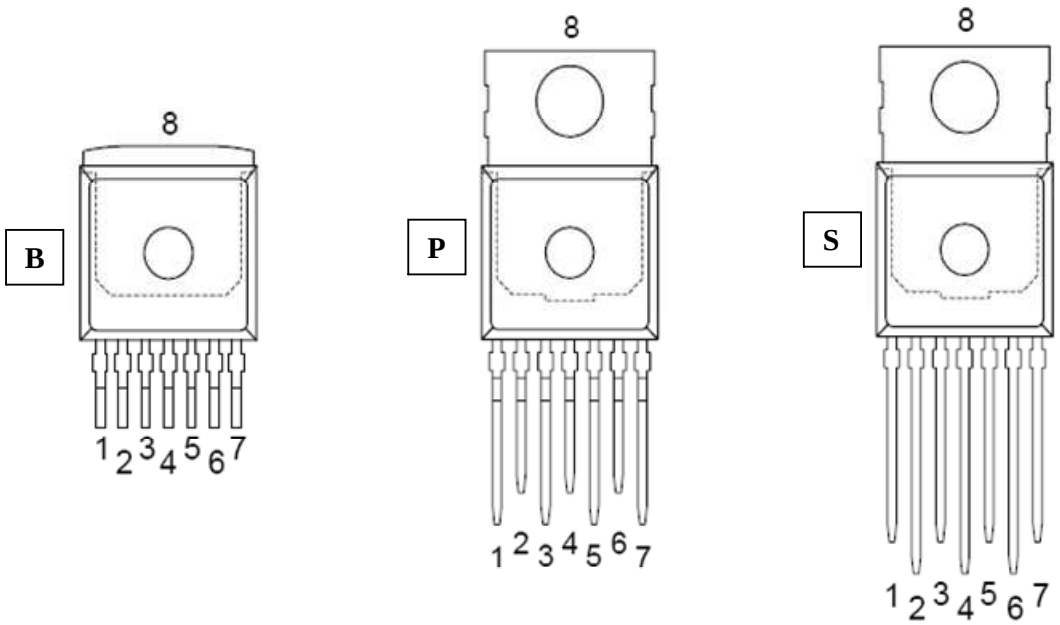


Figure 2 Pin assignment for FAN7093_F085B, FAN7093_F085P and FAN7093_F085S

4.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
1	**GND**	-	Ground
2	IN	I	Input Defines whether high- or lowside switch is activated
3	$\overline{INH}$	I	Inhibit When set to low device goes in sleep mode and resets over temperature and HS and LS short latch
4,8	**OUT**	**O**	Power output of the bridge
5	SR	I	Slew Rate The slew rate of the power switches can be adjusted by connecting a resistor between SR and GND
6	IS	O	Current Sense and Diagnostics
7	**V_{BATT}**	-	Supply

Bold type pins need power wiring

Note: See truth table in section 7.3.5 on page 14 for details

5 General Product Characteristics

5.1 *Absolute Maximum Ratings*

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	*Symbol*	Min.	Typ.	Max.	Unit	Conditions
5.1.1	Supply Voltage	V_{BATT}	-0.3		45	V	–
5.1.2	Logic Input Voltage	$V_{IN\ (H)}$	-0.3		45	V	–
5.1.3	Voltage at SR Pin	V_{SR}	-0.3		1.5	V	–
5.1.4	Voltage at IS Pin	V_{IS}	-0.3		7.5	V	–
5.1.5	HS/LS Continuous Drain Current [2)]	$I_{D(HS)}$ $I_{D(LS)}$		-46/46		A	T_C < 85°C
5.1.6	HS/LS Pulsed Drain Current [2)]	$I_{D(HS)}$ $I_{D(LS)}$		-90/90		A	T_C < 85°C single pulse < 5us
5.1.7	HS/LS PWM Current [2)]	$I_{D(HS)}$ $I_{D(LS)}$		-55/55		A	T_C < 125°C f = 1kHz, DC = 50%

Temperatures

5.1.8	Junction Temperature	T_j	-40		150	°C	–
5.1.9	Storage Temperature	T_{stg}	-55		150	°C	–

ESD Susceptibility

5.1.10	IN, $\overline{INH}$, SR, IS	V_{ESD}	-2		2	kV	HBM [3)]
5.1.11	OUT, GND, V_{BATT}	V_{ESD}	-6		6	kV	HBM [3)]

1) Not subject to production test, specified by design

2) Maximum reachable current may be smaller depending on current limitation level

3) ESD susceptibility, HBM according to AEC_Q100-004C /JESD22-A114-B (1.5 kΩ, 100 pF)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation

5.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
5.2.1	Supply Voltage Range for nominal operation	$V_{BATT(nom)}$	7	18	V	–
5.2.2	Supply Voltage Range for extended operation	$V_{VBATT(ext)}$	5.5	28	V	Parameter deviations possible
5.2.3	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

5.3 Thermal Resistance [4]

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
5.3.1	Thermal Resistance Junction-Case, Low Side Switch Rthjc(LS) = ΔTj(LS)/ Pv(LS)	$R_{thjc(LS)}$		0.8		°C/W	
5.3.3	Thermal Resistance Junction-Case, High Side Switch Rthjc(HS) = ΔTj(HS)/ Pv(HS)	$R_{thjc(HS)}$		0.45		°C/W	
5.3.1	Thermal Resistance Junction Ambient	R_{thJA}		40		°C/W	(1sq. inch cooling area)

4) Not subject to production test, specified by design

6 Block Description and Characteristics

6.1 Supply Characteristics

VBATT = 7 V to 18 V, T_j = -40 C to +150 C, I_L = 0 A, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
6.1.1	Supply Current	$I_{VBATT(on)}$	–	--	5.0	mA	V_{INH} = 5 V, V_{IN} = 5V, R_{SR} = 0 Ω, DC-mode, no fault condition
6.1.2	Quiescent Current	$I_{VBATT(off)}$	–	--	450	µA	V_{INH} = 0 V, V_{IN} = 0V,

7 Power Stages

The power stages of the FAN7093_F085 consist of a p-channel vertical DMOS transistor for the high side switch and a n-channel vertical DMOS transistor for the low side switch. All protection and diagnostic functions are located in the control die. Both switches can be operated up to 60 kHz, allowing active freewheeling and thus minimizing power dissipation in the forward operation of the

integrated diodes.
The on state resistance $R_{ds(on)}$ is dependent on the supply voltage *VBATT* as well as on the junction temperature T_j.

7.1 Power Stages - Static Characteristics

VBATT = 7 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

High Side Switch - Static Characteristics

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
7.1.1	ON State High Side Resistance[5)] I_{OUT} = -20 A; *VBATT* = 14 V	$R_{DS(ON)\ HS}$			12.3	mΩ	FAN7093_F085B (TO-263-7L, D^2PAK)
7.1.2	Leakage Current	$I_{Leak(HS)}$			50.0	µA	V_{INH} = 0 V; V_{OUT} = 0 V
7.1.3	Reverse Diode Forward-Voltage[6)]				1.5	V	I_{OUT} = -9 A

Low Side Switch - Static Characteristics

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
7.1.4	ON State Low Side Resistance[5)] I_{OUT} = 20 A; *VBATT* = 14 V	$R_{DS(ON)\ LS}$			18.2	mΩ	FAN7093_F085B
7.1.5	Leakage Current	$I_{Leak(LS)}$			10.0	µA	V_{INH} = 0 V; V_{OUT} = *VBATT*
7.1.6	Reverse Diode Forward-Voltage[6)]				-1.5	V	I_{OUT} = 9 A

5) Specified $R_{ds(on)}$ value is related to normal soldering points; Rds(on) values is specified for FAN7093_F085B: pin 1,7 to pin 8 (tab, backside) and for FAN7093_F085P/FAN7093_F085S: pin 1,7 to pin4

6) Due to active freewheeling, diode is conducting only for a few µs, depending on R_{SR}

7.1.1 Switching Times

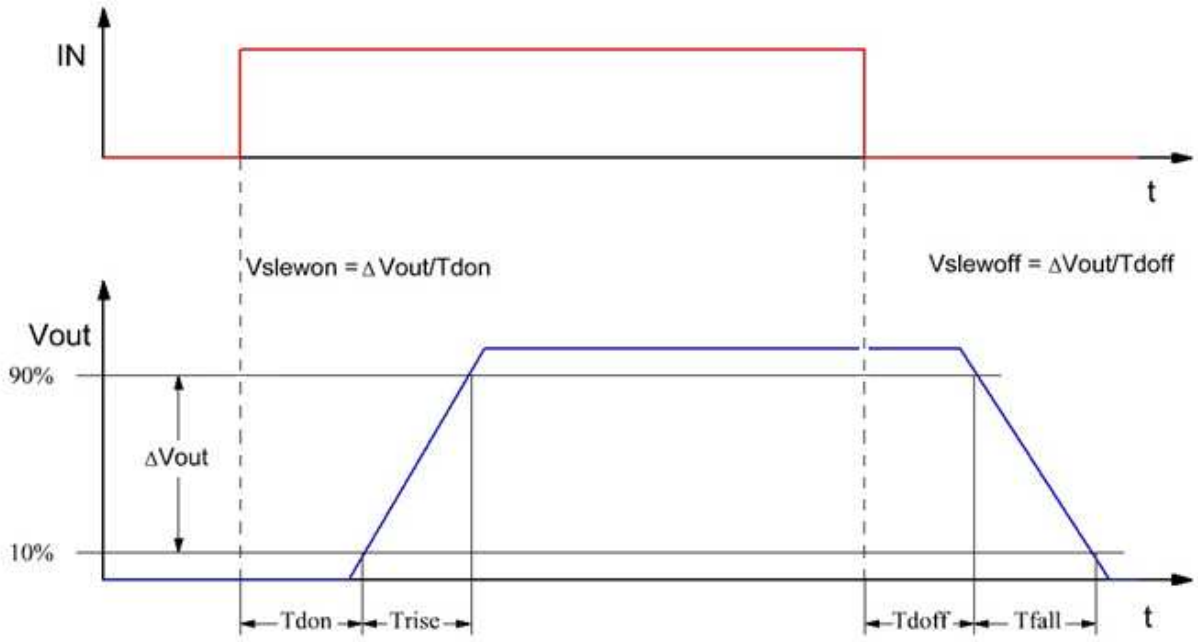


Figure 3 Timing diagram

Due to the timing differences for the rising and the falling edge there will be a slight difference between the length of the input pulse and the length of the output pulse.

7.1.2 Power Stages - Dynamic Characteristics

VBATT = 7V - 14 V, T_j = -40 °C to +150 °C, R_{load} = 2Ω all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

High Side Switch Dynamic Characteristics

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
7.1.7	Slew Rate (Note 1)	$V_{Slew(ON)}$	15 12 5 0.8	19 15 6 1	24 17 7 1.2	V/µs	RSR = 0 Ω RSR = 5.1 kΩ RSR = 51 kΩ RSR = open Rload to GND
7.1.8	Turn On delay time	$T_{d(ON)}$	0.45	2.1	4.2	µs	

Low Side Switch Dynamic Characteristics

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
7.1.9	Slew Rate (Note 1)	$V_{Slew(OFF)}$	18 13 5 0.8	21 17 6 1	24 19 7 1.2	V/µs	RSR = 0 Ω RSR = 5.1 kΩ RSR = 51 kΩ RSR = open Rload to VBATT
7.1.10	Turn On delay time	$T_{d(ON)}$	0.45	2.1	4.2	µs	

Note 1: Not subject to production test

7.2 Protection Functions

The device provides integrated protection functions. These are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not to be used for continuous or repetitive operation, with the exception of the current limitation. In a fault condition the FAN7093_F085 will apply the highest slew rate possible independent of the connected slew rate resistor. Over voltage, over temperature and over current are indicated by a fault current flag $I_{IS(LIM)}$ at the IS pin. The following describes the protection functions are listed in order of their priority. Over voltage lock out overrides all other error modes.

7.2.1 Over voltage Lock Out

To assure a high immunity against over voltage conditions like load dump, the device turns off the low-side MOSFET and turns on the high-side MOSFET when the supply voltage exceeds the over voltage protection level $V_{OV(OFF)}$. The control IC returns to normal operation 120us after the supply voltage decreases below the over voltage lock out level $V_{OV(ON)}$. In H-bridge configuration, this behavior of the FAN7093_F085 will lead to freewheeling in high-side during over voltage. If the load current exceeds 90A in over voltage lock out, the IC turns off the high side driver and latches this state.

7.2.2 Under voltage Shut Down

To avoid uncontrolled motion of for example a driven motor at low voltages, the control IC will turn off all MOSFETS, when the supply voltage drops below the turn-off voltage $V_{UV(OFF)}$. The control IC returns to normal operation when the supply voltage rises above the turn-on voltage $V_{UV(ON)}$.

7.2.3 Over temperature Protection

The FAN7093_F085 is protected against over temperature by an integrated temperature sensor in the control IC. Over temperature is turning off both output stages. This state is latched until the device is reset by a low signal with a minimum pulse length of t_{reset} at the $\overline{INH}$ pin, assuming the control IC temperature decreased by at least the thermal hysteresis Repetitive use of the over temperature protection impacts lifetime.

7.2.4 Current Limitation

The current is measured in both MOSFETS of the FAN7093_F085. As soon as the current is reaching the limit I_{CL}, the low- or high-side MOSFET is deactivated and the other MOSFET activated for t_{CLS}. During that time changes at the IN pin are ignored. However, the $\overline{INH}$ pin can still be used to turn off both MOSFETs. After time t_{CLS} the MOSFETS return to their initial setting. The error signal at the IS pin is reset after 2 * t_{CLS}. Unintentional triggering of the current limit circuitry through short current spikes (e.g. inflicted by EMI coming from the motor) is suppressed by an internal filter. Reaction delay time of the filter circuitry is affecting the current limit level I_{CL} depending on slew rate of the load

current *dI/dt*.

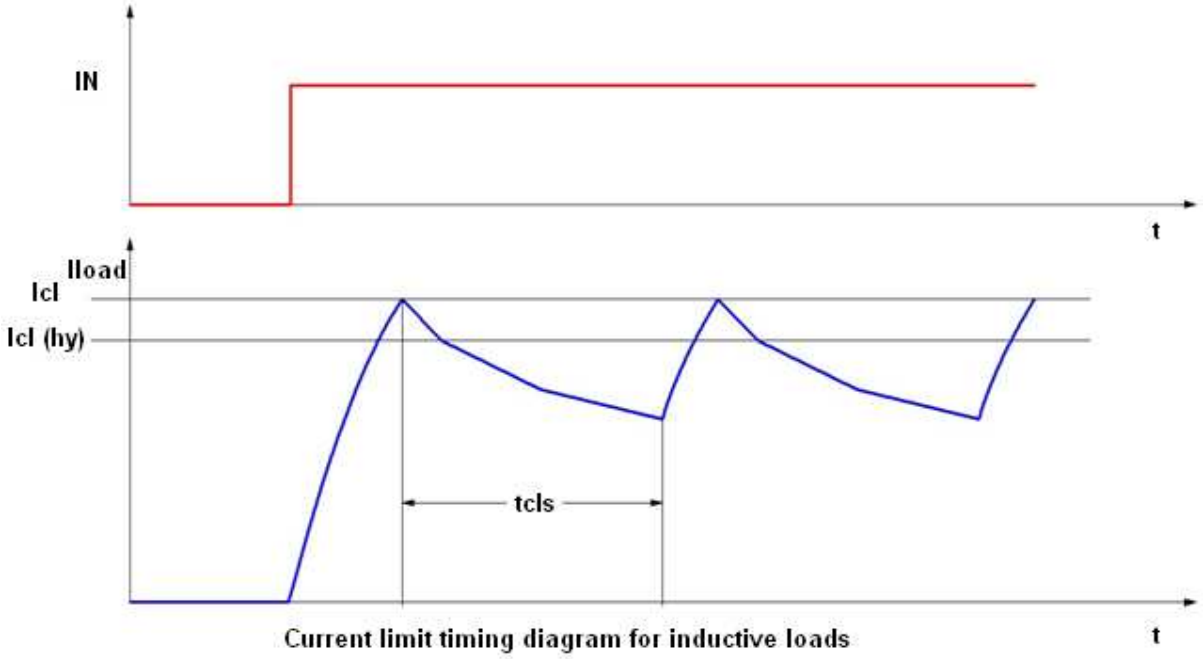


Figure 4 Timing Diagram Current Limitation (Inductive Load)

In combination with a typical inductive load, such as a motor, this results in a switched mode current limitation. This method of limiting the current has the advantage of greatly reduced power dissipation in the FAN7093_F085 compared to driving the MOSFET in linear mode. Therefore it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor start up). However, the regular use of the current limitation is allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature can reduce the lifetime of the device.

7.2.5 Short Circuit Protection

The device is short circuit protected against

- output shorted to ground
- output shorted to battery voltage
- short circuit of load

The short circuit protection is a combination of current limit and over-temperature shut down of the device

7.2.6 Electrical Characteristics - Protection Functions

VBATT = 7 V to 18 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Under Voltage Shut Down							
7.2.1	Turn - off Voltage	$V_{UV(ON)}$	–	–	5.6	V	V_S increasing
7.2.2	Turn - on Voltage	$V_{UV(OFF)}$	4.9	–	--	V	V_S decreasing
7.2.3	hysteresis	$V_{UV(HY)}$	–	0.15	–	V	–
Over Voltage Lock Out							
7.2.4	Turn - off Voltage	$V_{OV(ON)}$	28	–	–	V	V_S decreasing
7.2.5	Turn - on Voltage	$V_{OV(OFF)}$	27	–	35	V	V_S increasing
7.2.6	hysteresis	$V_{OV(HY)}$	–	1.0	–	V	–
7.2.7	Lock out time	t_{lock}		140		µs	
Current Limitation							
7.2.8	Current Limit Detection level High- and Low- side	I_{CL}	39	50	61	A	
7.2.9	Peak Current Limit Detection level High- and Low- side (Note 2)	I_{CP}	72	88	105	A	
Note 2. Not subject to production test, specified by design							
Current Limitation Timing							
7.2.10	Shut OFF Time for HS and LS	t_{CLS}	100	150	200	µs	
Thermal Shut Down [6]							
7.2.11	Turn off Tj	T_{jSD}	170	--	190	°C	–
7.2.12	Turn on Tj	T_{jSO}	150	–	170	°C	–
7.2.13	Thermal Hysteresis	$T_{sd(HY)}$	–	15	–	K	–
7.2.14	Reset Pulse at $\overline{INH}$ Pin ($\overline{INH}$ low)	t_{reset}	4	–	–	µs	–

7) Not subject to production test, specified by design

7.3 Control and Diagnostics

7.3.1 Input Circuit

The gate drivers for the MOSFETS are controlled through inputs IN and $\overline{INH}$ and are TTL/CMOS compatible Schmitt triggers with hysteresis. Setting the $\overline{INH}$ pin to high enables the device. In this condition one of the two power MOSFETS is turned on depending on the input level of the IN pin. To

deactivate both switches, the $\overline{INH}$ pin has to be set to low. No external driver is needed. The FAN7093_F085 can interface directly with a microcontroller, as long as the maximum ratings are not exceeded.

7.3.2 Dead Time Generation

The dead time is generated on the control IC to prevent shoot through between the power MOSFETS. The dead time is almost independent of the selected slew rate in order to reach a high PWM frequency of 60kHz

7.3.3 Adjustable Slew Rate

In order to optimize electromagnetic emission, the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin SR allows the user to optimize the balance between emission and power dissipation within the application by connecting an external resistor R_{SR} to GND. If the SR pin is open by design or if the intermittent disconnect happens, the slew rate is set to the value shown in table on page 8 rows 7.1.1, 7.1.9.

7.3.4 Status Flag Diagnostic with Current Sense Capability

The status pin IS is used as a combined current sense and error flag output. In normal operation (current sense mode), a current source, in the control IC is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high-side or low-side MOSFET. Current flow in the reverse direction cannot be detected except for a marginal leakage current $I_{IS(LK)}$. The external resistor R_{IS} determines the voltage per output current. The current sense ratio is 1/8500 (see table on page 15 for details). In case of a fault condition the status output is connected to a current source which is independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. In case of current limitation the $I_{IS(lim)}$ is activated for 2 * t_{CLS}.

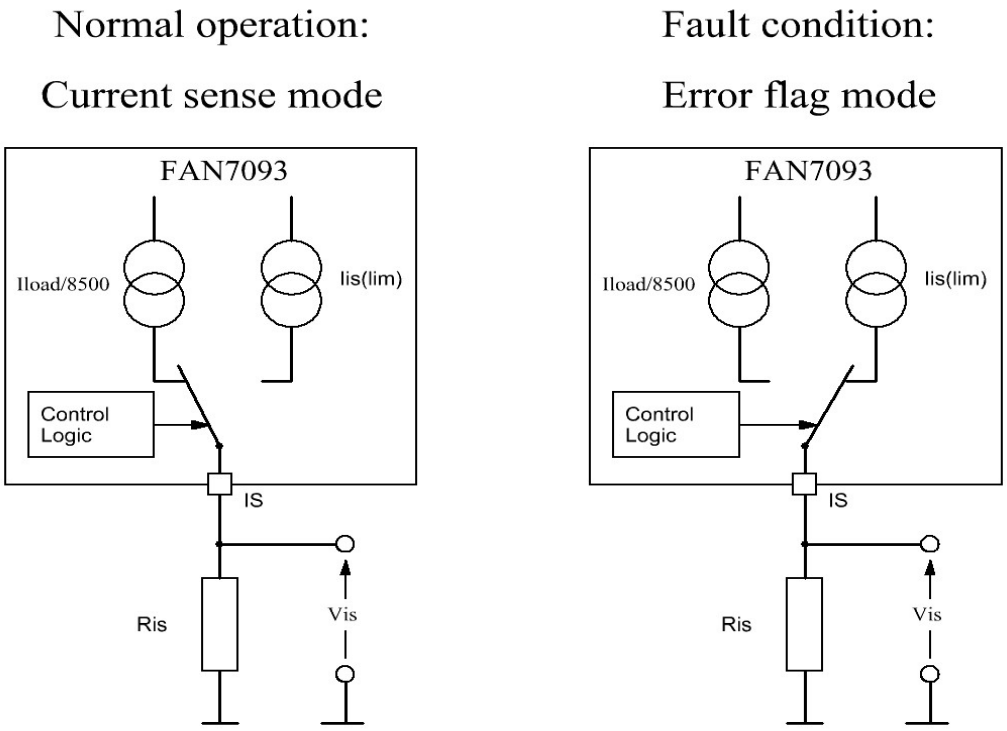


Figure 5 Current sense mode and error flag mode

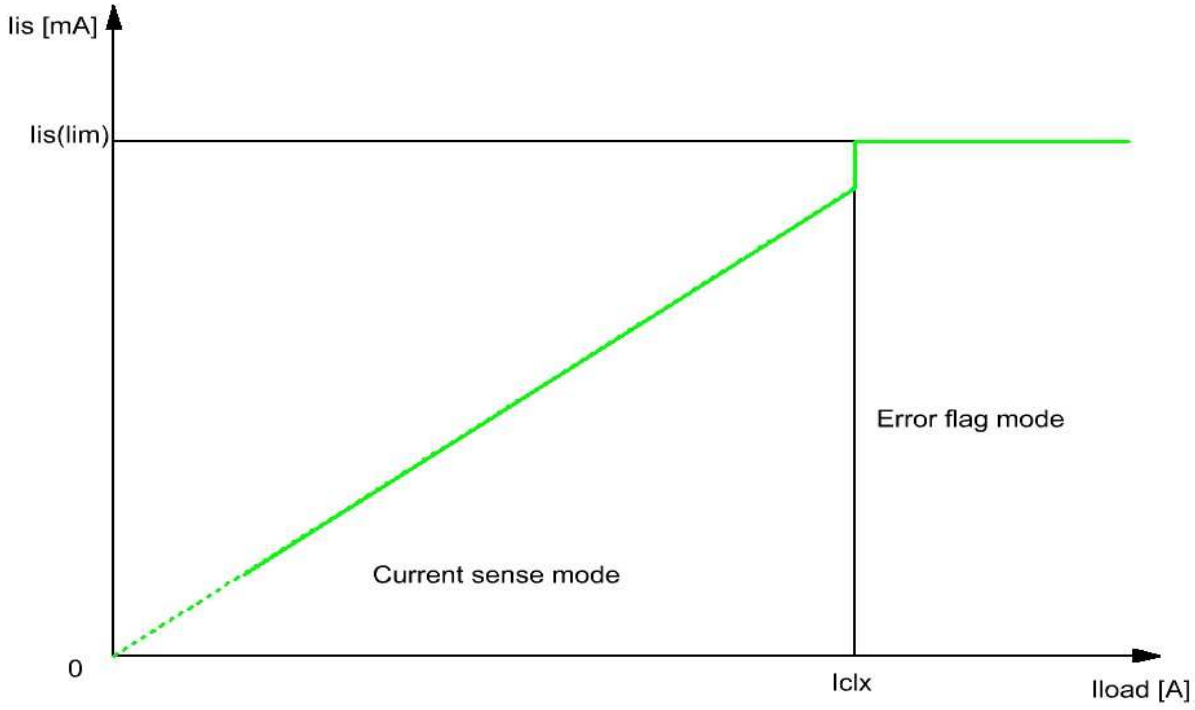


Figure 6 Sense current versus load current and flag current

7.3.5 Truth table

Device state	$\overline{INH}$	IN	HS	LS	IS	Mode
Normal operation	0	X	OFF	OFF	0	Stand-by mode
Normal operation	1	0	OFF	ON	CS	LS active
Normal operation	1	1	ON	OFF	CS	HS active
Over voltage	X	X	ON	OFF	1	Shut-down of LS, HS activated, error detected
Under voltage	X	X	OFF	OFF	0	UV lockout
Over temperature Or shorted LS or HS	0	X	OFF	OFF	0	Stand-by mode, reset of latch
Over temperature Or shorted LS or HS	1	X	OFF	OFF	1	Shut-down with latch, error detected
Current limit	1	1	OFF	ON	1	Switched mode, error detected [8)]
Current limit	1	0	ON	OFF	1	Switched mode, error detected[8)]

8) Device will return to normal operation after time tcls. The error signal will be reset after 2*tcls.

Inputs	Power FETs	Status flag IS
0 = logic low	OFF = turned off	CS = current sense mode
1 = logic high	ON = turned on	1 = logic high (error)
X = Don’t care		

7.3.6 Electrical Characteristics - Control and Diagnostics

VBATT = 7 V to 18 V, T_j = -40 C to +150 C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Control Inputs (IN and $\overline{INH}$)							
7.3.1	Low level Voltage $\overline{INH}$,IN	V_{INXH}	1.5			V	
7.3.2	High level Voltage $\overline{INH}$,IN	V_{INXH}			3.5	V	
7.3.3	Input voltage hysteresis	$V_{INXH(HY)}$	500			mV	
7.3.4	Input current high level	I_{INXH}	20		80	µA	V_{INH} = V_{IN} = 0.4V - 5.3V
Current Sense							
7.3.5	Current Sense ratio in static on-Condition KILIS = IL/IIS	KILIS	4.5 3.5	8.5	13.5	10^3	R_{IS} = 800 Ω I_L = 8A – 50A I_L = 1.1A – 8A
7.3.6	Maximum analog Sense Current	$I_{IS(lim)}$	4.5		5.5	mA	R_{IS} = 800 Ω
7.3.7	Sense Current in fault Condition (Note 3)	$I_{IS(fault)}$	5.5		7	mA	R_{IS} = 800 Ω note
7.3.8	Maximum IS output voltage	$V_{IS(fault)}$			7.5	V	$R_{IS} \geq 3$ kΩ
7.3.9	Isense Leakage current	I_{ISLeak}			300	µA	V_{INH} = 5 V, V_{IN} = X, I_L = 0 A
7.4.0	Settling time	t_{SET}			4	µs	*IN – 90%Vis*

Note 3. Not subject to production test, specified by design

8 Application

.

Application Examples

Typical motor drive application in full bridge configuration

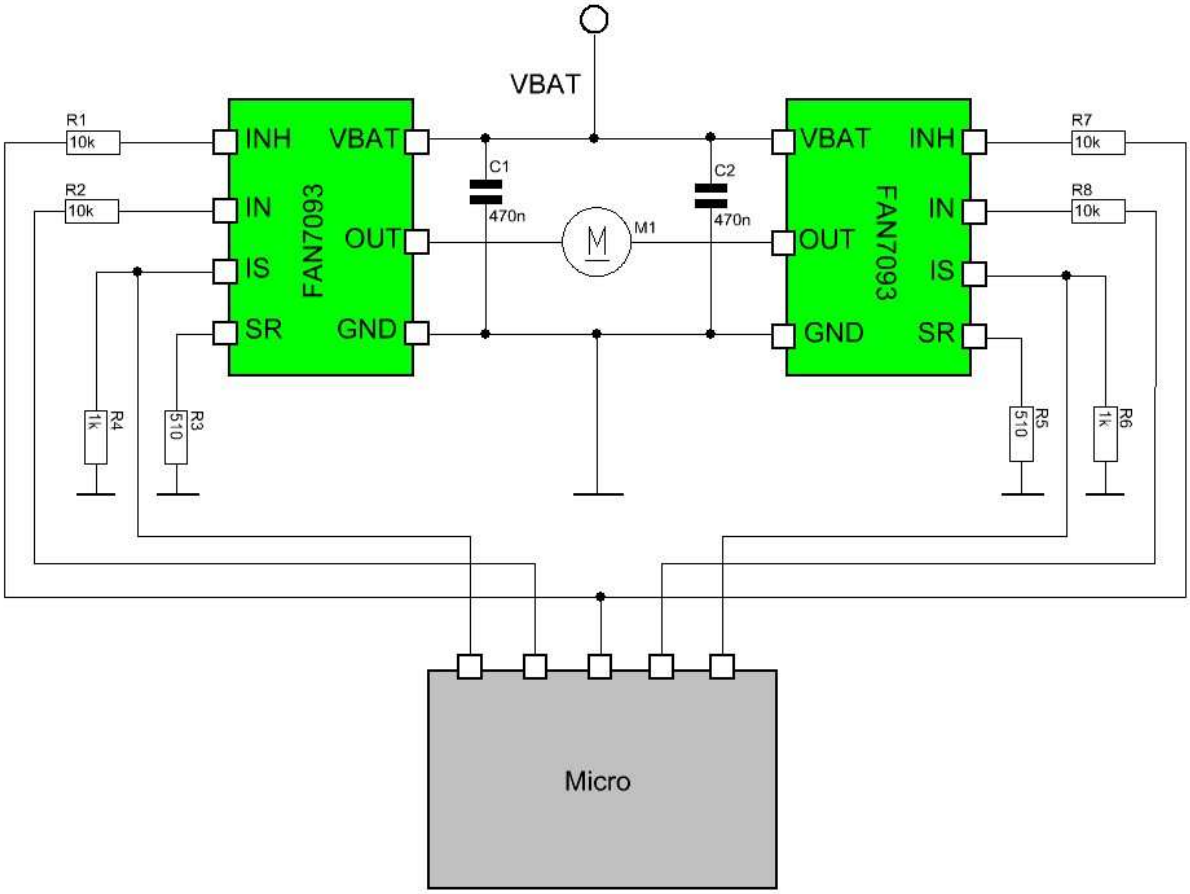


Figure 7 Full bridge application

Typical motor drive application in half bridge configuration

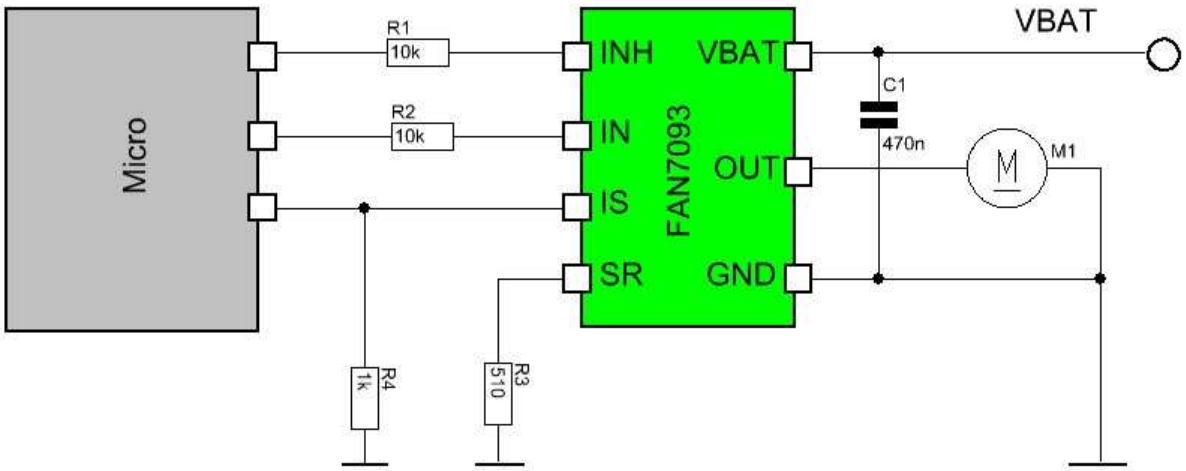
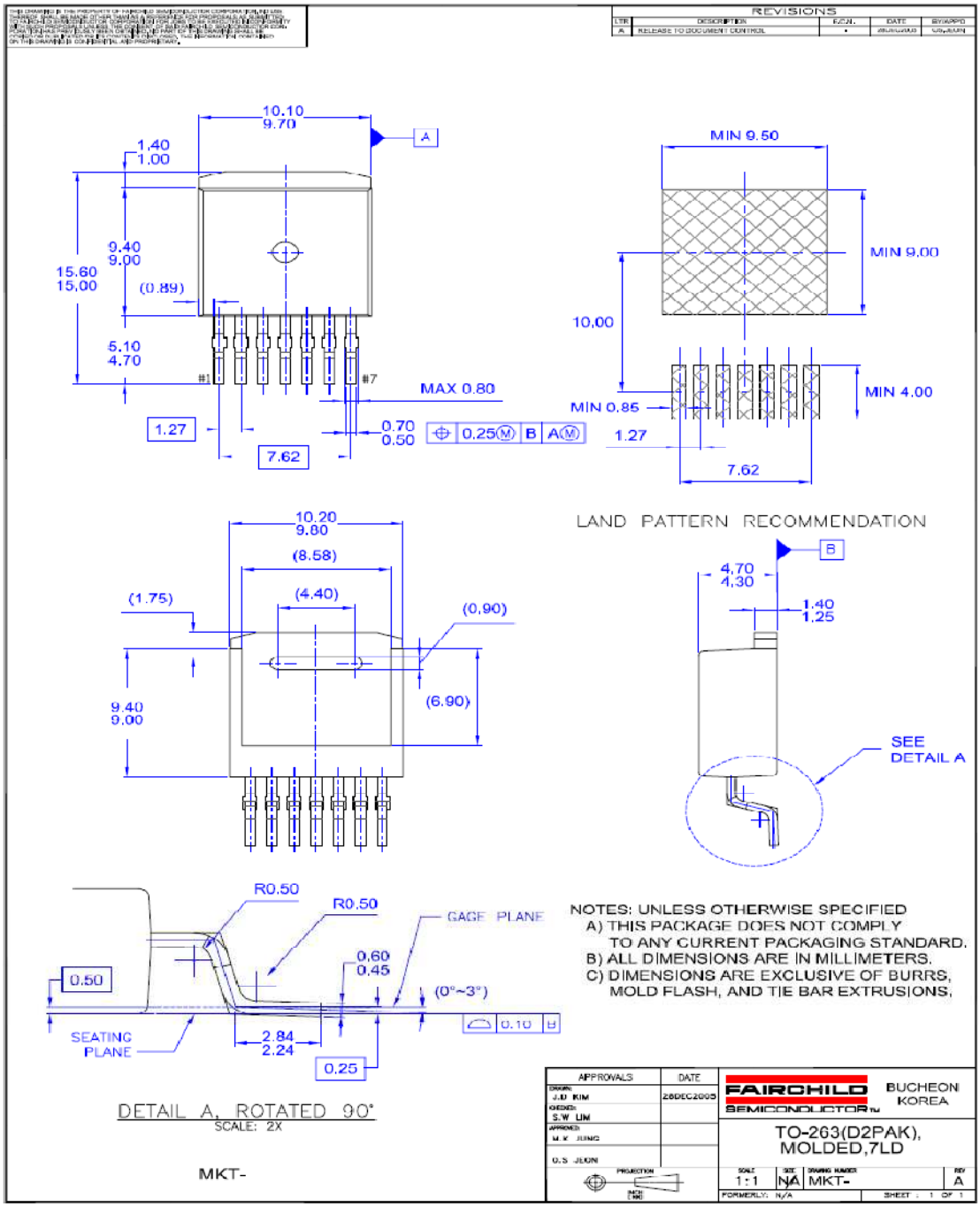


Figure 8 Half bridge application

9 Package drawings



FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
Auto-SPM™
AX-CAP™*
BitSiC®
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficentMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter® *
FPS™
F-PFS™
FRFET®
Global Power Resource^{SM}
Green FPS™
Green FPS™ e-Series™
G*max*™
GTO™
IntelliMAX™
ISOPLANAR™
Marking Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL ®*
The Power Franchise®
the power franchise®
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC®
TriFault Detect™
TRUECURRENT®*
µSerDes™
µSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I60