NX18P3001

Bidirectional high-side power switch for charger and USB-OTG combined applications

Rev. 1 — 24 September 2013 Product data sheet

1. General description

The NX18P3001 is an advanced bidirectional power switch and ESD- protection device for combined USB-OTG and charger port applications. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits designed to automatically isolate the power switch terminals when a fault condition occurs.

The device features two power switch input/output terminals (VBUSI and VBUSO), an open-drain acknowledge output (ACK), an enable input which includes logic level translation ($\overline{EN}$) and low capacitance Transient Voltage Suppression (TVS) type ESD clamps for USB data and ID pins.

When $\overline{EN}$ is set HIGH the device enters a low-power mode, disabling all protection circuits. When used in combined charger and USB-OTG applications the 30 V tolerant VBUSI switch terminal is used as the supply and switch input when charging, for USB-OTG the VBUSO switch terminal is used as the supply and switch input.

Designed for operation from 3.2 V to 17.5 V, it is used in battery charging and power domain isolation applications to reduce power dissipation and extend battery life.

2. Features and benefits

- 30 V tolerant VBUSI supply pin
- Wide supply voltage range from 3.2 V to 17.5 V
- Automatic switch operation for charging within the supply range
- I_{SW} maximum 3 A continuous current
- Low ON resistance: 62 mΩ (typical) at a supply voltage of 5.0 V
- 1.8 V control logic input to open the switch
- Soft start turn-on slew rate
- Protection circuitry
  - Overtemperature protection
  - Overvoltage lockout
  - Undervoltage lockout
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E)
  - IEC61000-4-2 contact discharge exceeds 8 kV for pins VBUSI, D–, D+ and ID
- Specified from –40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX18P3001UK	–40 °C to +85 °C	WLCSP12	wafer level chip-scale package, 12 bumps; body 1.36 × 1.66 × 0.51 mm (Backside Coating included)	NX18P3001

5. Marking

Table 2. Marking codes

Type number	Marking code
NX18P3001UK	X18P3

6. Functional diagram

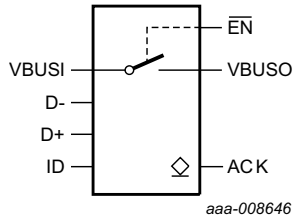


Fig 1. Logic symbol

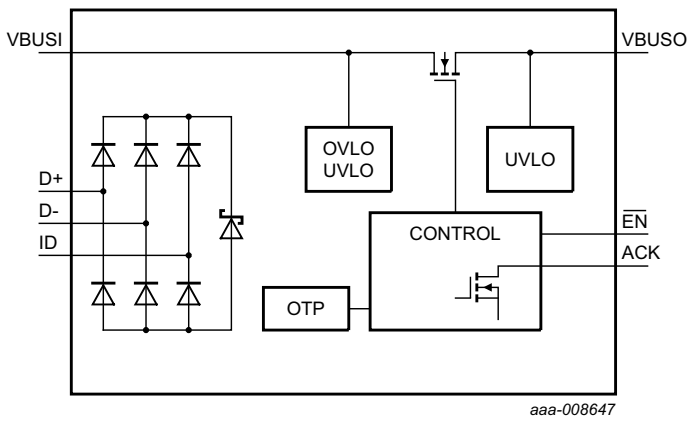


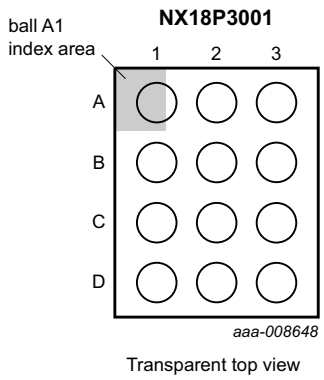
Fig 2. Logic diagram (simplified schematic)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

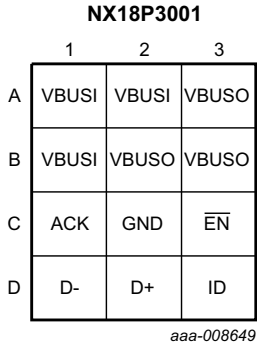
7. Pinning information

7.1 Pinning



Transparent top view

Fig 3. Pin configuration WLCSP12 package



Transparent top view

Fig 4. Ball mapping for WLCSP12

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBUSO	A3, B2, B3	VBUSO (output/input supply)
VBUSI	A1, A2, B1	VBUSI (input supply/output)
ACK	C1	acknowledge condition indicator (open-drain output)
GND	C2	ground (0 V)
EN	C3	enable input (active LOW)
D-	D1	ESD-protection I/O
D+	D2	ESD-protection I/O
ID	D3	ESD-protection I/O

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8. Functional description

Table 4. Function table[1]

$\overline{EN}$	VBUSI	VBUSO	ACK	Operation mode
L	< 3.2 V	< 3.2 V	Z	undervoltage lockout; switch open
L	3.2 V < VBUSI < 17.5 V	< 3.2 V	Z	enabled; switch closed; charging mode
L	< 3.2 V	> 3.2 V	Z	enabled; switch closed; OTG mode
L	X	X	0	overtemperature protection; switch open
L	> 17.5 V	X	0	overvoltage lockout; switch open
H	X	X	Z	disabled; switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.1 $\overline{EN}$-input

A HIGH on $\overline{EN}$ disables the N-channel MOSFET and all protection circuits putting the device into a low-power mode. A LOW on $\overline{EN}$ enables the protection circuits and then the N-channel MOSFET.

8.2 Undervoltage lockout

When $\overline{EN}$ is LOW and VBUSI and VBUSO < 3.2 V, the UnderVoltage LockOut (UVLO) circuits disable the N-channel MOSFET. Once VBUSI or VBUSO > 3.3 V and no other protection circuits are active, the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin.

8.3 Overvoltage lockout

When $\overline{EN}$ is LOW and VBUSI > 17.5 V, the OverVoltage LockOut (OVLO) circuit disables the N-channel MOSFET and set the ACK output LOW. Once VBUSI < 17.35 V and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin.

8.4 Overtemperature protection

When $\overline{EN}$ is LOW and the device temperature exceeds 125 °C the OverTemperature Protection (OTP) circuit disables the N-channel MOSFET and sets the ACK output LOW. Once the device temperature decreases to below 115 °C and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. If OVLO or OTP circuits are activated the ACK output is set LOW to indicate that a fault has occurred. The ACK output returns to high impedance state automatically once the fault condition is removed or $\overline{EN}$ is HIGH.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

9. Application diagram

The NX18P3001 typically connects a USB port in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level it is connected to.

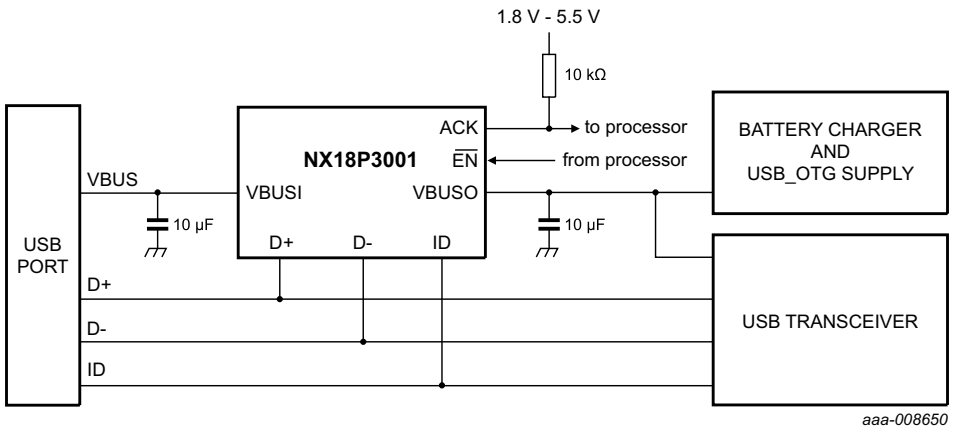


Fig 5. NX18P3001 application diagram

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUSI	[1]	−0.5	+32	V
		VBUSO	[1]	−0.5	+6.75	V
		$\overline{EN}$	[2]	−0.5	+6.0	V
		D-, D+, ID	[1]	−0.5	+6.0	V
V_O	output voltage	ACK		−0.5	+6.0	V
I_{IK}	input clamping current	$\overline{EN}$: V_I < −0.5 V		−50	-	mA
I_{SK}	switch clamping current	VBUSI; VBUSO; V_I < −0.5 V		−50	-	mA
I_{SW}	switch current	T_{amb} = 85 °C		-	3	A
$T_{j(max)}$	maximum junction temperature			−40	+125	°C
T_{stg}	storage temperature			−65	+150	°C

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C				
		WLCSP12 package	[3]		1.44	W

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For WLCSP12 package: P_{tot} derates linearly with 13.7 mW/K above 20 °C.

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUSI	3.0	30	V
		VBUSO	3.0	5.5	V
		$\overline{EN}$	0	5.5	V
$V_{I/O}$	input/output voltage	D-, D+, ID	0	5.5	V
T_{amb}	ambient temperature		−40	+85	°C

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	73	K/W

[1] The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Please rely on the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts

13. Static characteristics

Table 8. Static characteristics

$V_{I(VBUSI)}$ = 4.0 V to 16.0 V or $V_{I(VBUSO)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\overline{EN}$	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	ACK; I_O = 8 mA	-	-	0.5	-	0.5	V
R_{pu}	pull-up resistance	ACK	10	-	200	10	200	kΩ
V_{pu}	pull-up voltage	ACK	1.65	-	5.5	1.65	5.5	V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 8. Static characteristics *...continued*

$V_{I(VBUSI)}$ = 4.0 V to 16.0 V or $V_{I(VBUSO)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I_{GND}	ground current	$\overline{EN}$ = LOW; I_O = 0 A; see Figure 6 to Figure 13	-	280	-	-	450	µA
		$\overline{EN}$ = HIGH; $V_{I(VBUSx)}$ = 5.5 V; [2] I_O = 0 A; see Figure 6 to Figure 13	-	8	-	-	16	µA
		$\overline{EN}$ = HIGH; $V_{I(VBUSI)}$ = 16 V; I_O = 0 A; see Figure 6 to Figure 13	-	20	-	-	33	µA
$I_{S(OFF)}$	OFF-state leakage current	$V_{I(VBUSI)}$ = 30 V; [3] $V_{I(VBUSO)}$ = 0 V to 5 V; see Figure 14	-	0.1	-	-	6.5	µA
		$V_{I(VBUSO)}$ = 5.5 V; [4] $V_{I(VBUSI)}$ = 0 V to 5 V; see Figure 15	-	0.1	-	-	8.5	µA
V_{UVLO}	undervoltage lockout voltage	VBUSI; VBUSO; $\overline{EN}$ = LOW	3.0	3.2	3.4	3.0	3.4	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage	VBUSI; VBUSO; $\overline{EN}$ = LOW	-	100	-	-	-	mV
V_{OVLO}	overvoltage lockout voltage	VBUSI; $\overline{EN}$ = LOW	16.5	17.5	18.5	16.5	18.5	V
$V_{hys(OVLO)}$	overvoltage lockout hysteresis voltage	VBUSI; $\overline{EN}$ = LOW	-	105	-	-	-	mV
$C_{I/O}$	input/output capacitance	D-; D+; ID; $V_{I(VBUSx)}$ = 5.5 V [2]	-	3	-	-	-	pF
C_I	input capacitance	$\overline{EN}$	-	3	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	VBUSI; VBUSO	-	-	0.5	-	0.5	nF

[1] All typical values are measured at $V_{I(VBUSx)}$ = 5.0 V unless otherwise specified.

[2] VBUSx is the supply voltage associated with the input, either VBUSI or VBUSO.

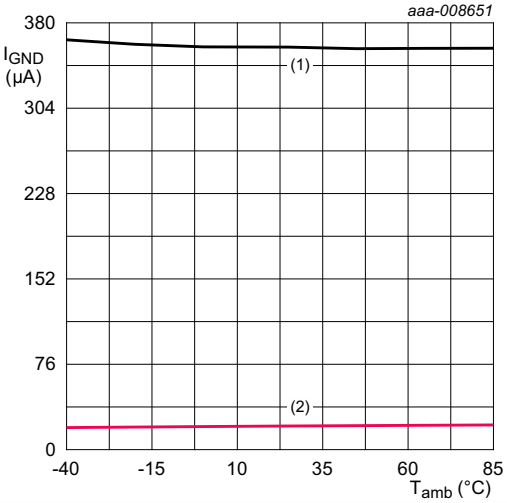
[3] Typical value is measured at $V_{I(VBUSO)}$ = 0 V.

[4] Typical value is measured at $V_{I(VBUSI)}$ = 0 V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

13.1 Graphs

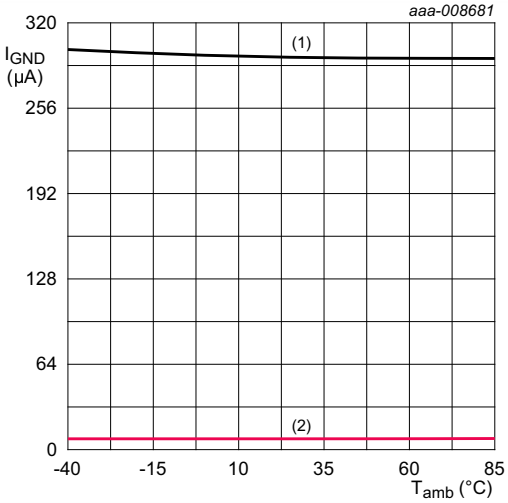


$V_{I(VBUSI)}$ = 16 V

(1) Enabled

(2) Disabled

Fig 6. Ground current versus temperature

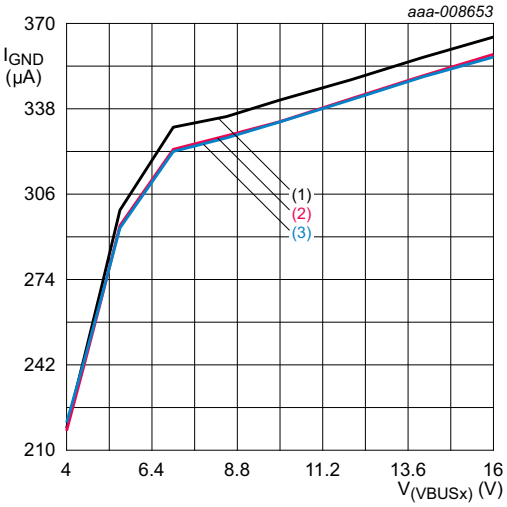


$V_{I(VBUSO)}$ = 5.5 V

(1) Enabled

(2) Disabled

Fig 7. Ground current versus temperature



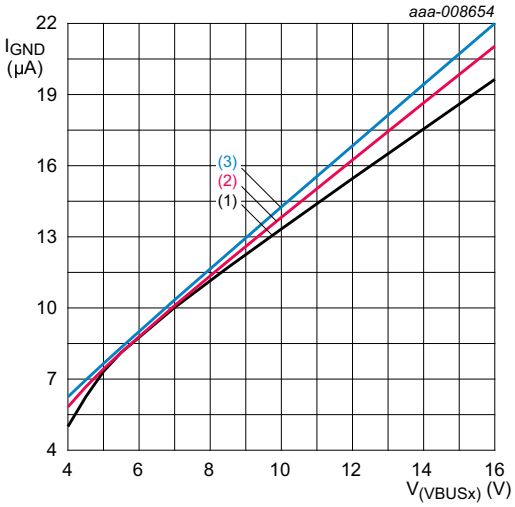
$\overline{EN}$ = L

(1) T_{amb} = −40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 8. Ground current versus input voltage on pin VBUSI



$\overline{EN}$ = H

(1) T_{amb} = −40 °C.

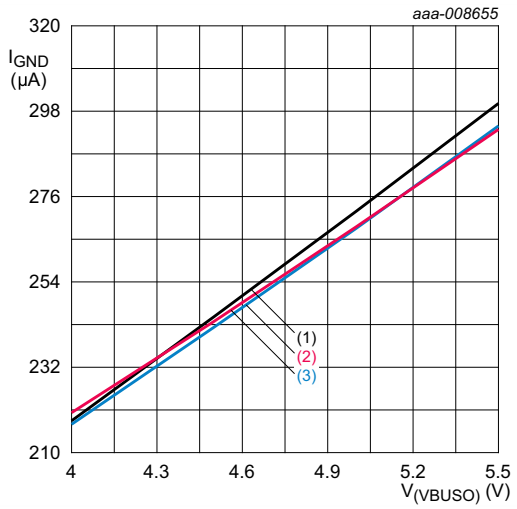
(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 9. Ground current versus input voltage on pin VBUSI

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



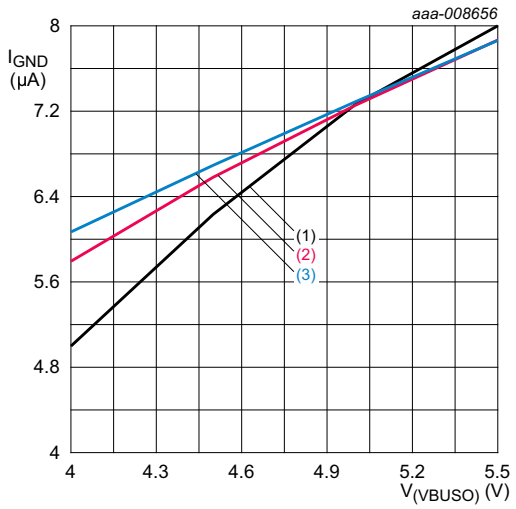
$\overline{EN}$ = L

(1) T_{amb} = −40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 10. Ground current versus input voltage on pin VBUSO



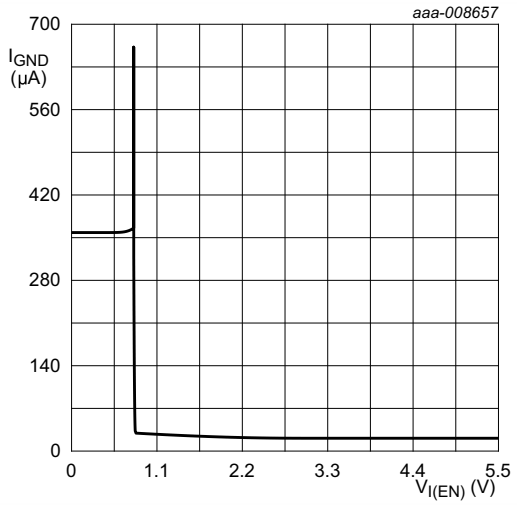
$\overline{EN}$ = H

(1) T_{amb} = −40 °C.

(2) T_{amb} = 25 °C.

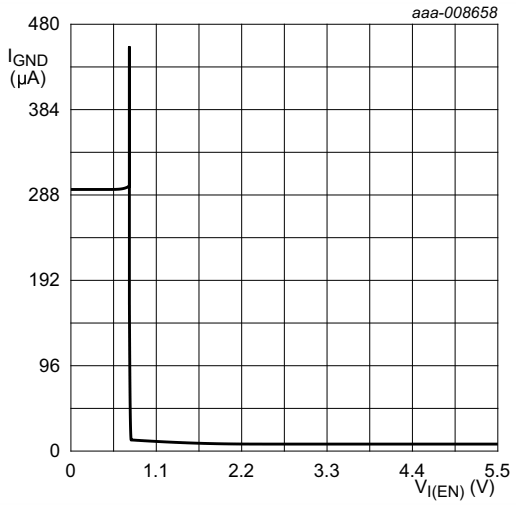
(3) T_{amb} = 85 °C.

Fig 11. Ground current versus input voltage on pin VBUSO



$V_{I(VBUSI)}$ = 16 V

Fig 12. Ground current versus input voltage on pin $\overline{EN}$

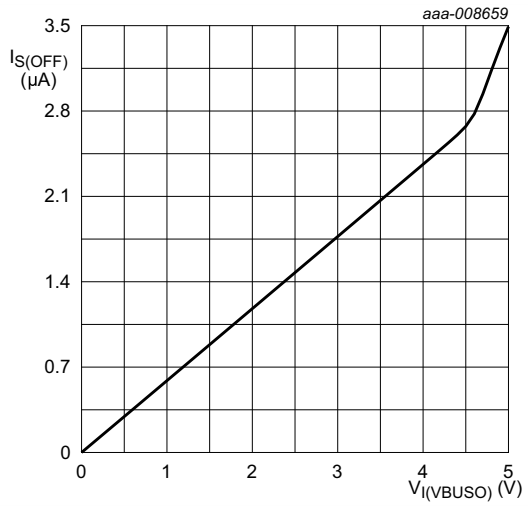


$V_{I(VBUSO)}$ = 5.5 V

Fig 13. Ground current versus input voltage on pin $\overline{EN}$

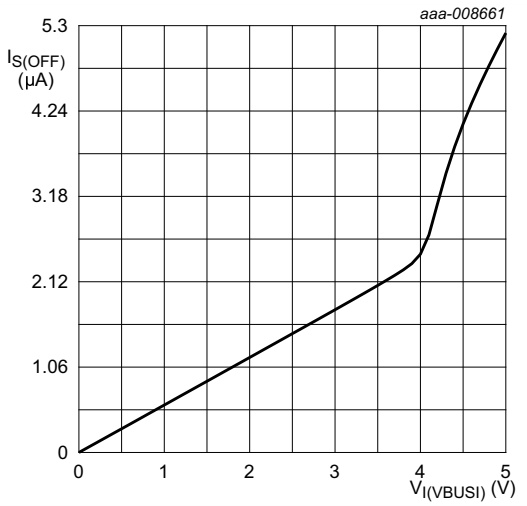
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



$V_{I(VBUSI)}$ = 16 V

Fig 14. OFF-state leakage current versus input voltage on pin VBUSO



$V_{I(VBUSO)}$ = 5.5 V

Fig 15. OFF-state leakage current versus input voltage on pin VBUSI

13.2 ON resistance

Table 9. ON resistance

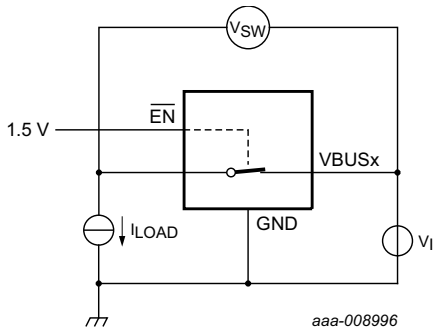
At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	$V_{I(VBUSI)}$ = 4.0 V to 16 V; see Figure 16 to Figure 20						
		I_{LOAD} = 200 mA	-	62	-	40	100	mΩ
		I_{LOAD} = 1.5 A	-	62	-	40	100	mΩ
		$V_{I(VBUSO)}$ = 4.0 V to 5.5 V; see Figure 16 to Figure 20						
		I_{LOAD} = 200 mA	-	62	-	40	100	mΩ
		I_{LOAD} = 1.5 A	-	62	-	40	100	mΩ

All information provided in this document is subject to legal disclaimers.

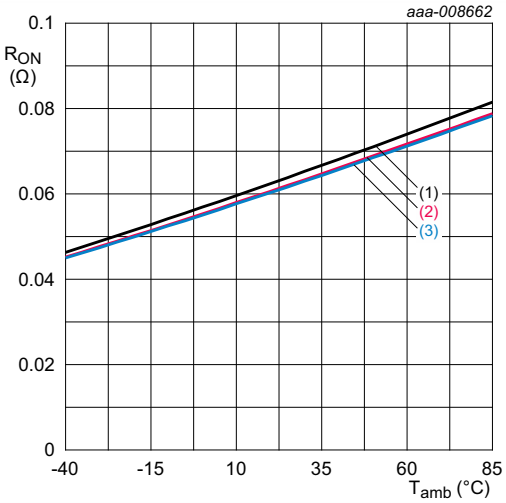
© NXP B.V. 2013. All rights reserved.

13.3 ON resistance test circuit and graphs



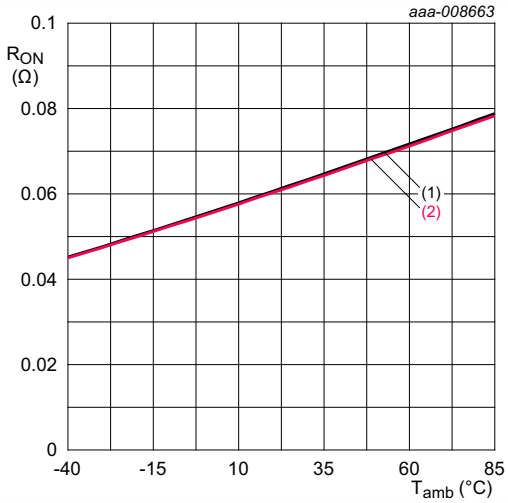
$R_{ON} = V_{SW} / I_{LOAD}$

Fig 16. Test circuit for measuring ON resistance



$V_{I(VBUSI)}$ = 4.0 V and 16 V

Fig 17. ON resistance versus temperature

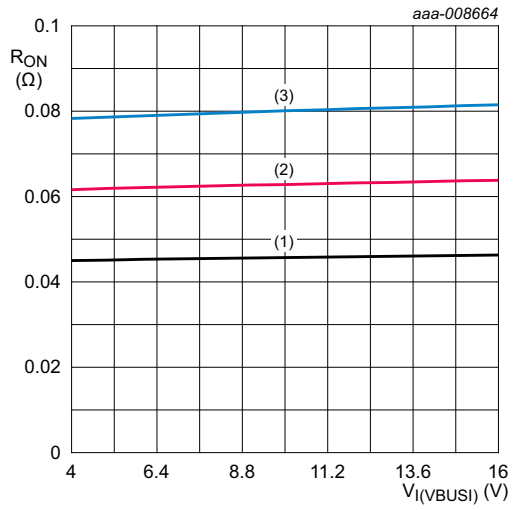


$V_{I(VBUSO)}$ = 4.0 V and 5.5 V

Fig 18. ON resistance versus temperature

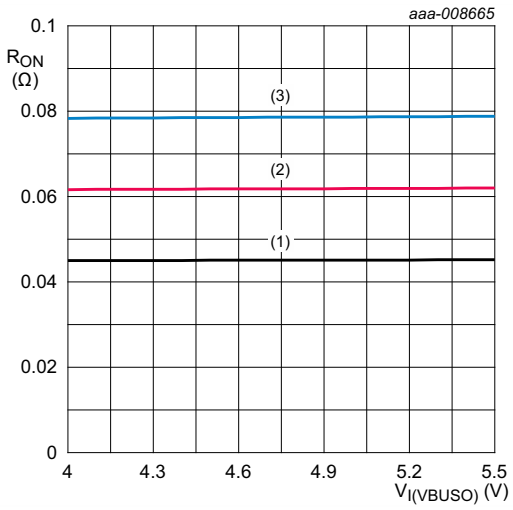
All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



(1) T_{amb} = −40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 85 °C.

Fig 19. ON resistance versus input voltage on pin VBUSI



(1) T_{amb} = −40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 85 °C.

Fig 20. ON resistance versus input voltage on pin VBUSO

14. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 22.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	$\overline{EN}$ to VBUSO; see Figure 21 and Figure 23 to Figure 26						
		$V_{I(VBUSI)}$ = 4.0 V	-	500	-	210	-	µs
		$V_{I(VBUSI)}$ = 16 V	-	500	-	250	-	µs
		$\overline{EN}$ to VBUSI; see Figure 21 and Figure 23 to Figure 26						
		$V_{I(VBUSO)}$ = 4.0 V	-	500	-	310	-	µs
		$V_{I(VBUSO)}$ = 5.5 V	-	500	-	290	-	µs
t_{dis}	disable time	$\overline{EN}$ to VBUSO; see Figure 21 and Figure 27 to Figure 30						
		$V_{I(VBUSI)}$ = 4.0 V	-	1.6	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	1.6	-	-	-	ms
		$\overline{EN}$ to VBUSI; see Figure 21 and Figure 27 to Figure 30						
		$V_{I(VBUSO)}$ = 4.0 V	-	1.6	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	1.6	-	-	-	ms

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 10. Dynamic characteristics *...continued*

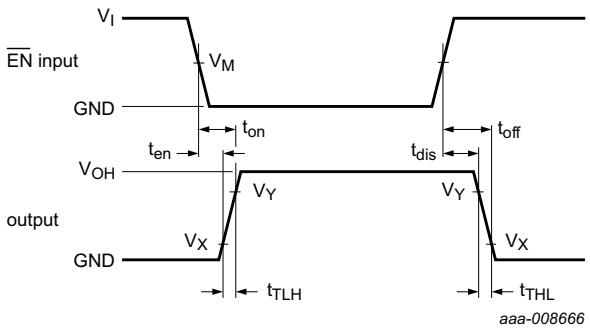
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 22.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{on}	turn-on time	$\overline{EN}$ to VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	1500	-	880	-	µs
		$V_{I(VBUSI)}$ = 16 V	-	2000	-	1130	-	µs
		$\overline{EN}$ to VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	1500	-	820	-	µs
		$V_{I(VBUSO)}$ = 5.5 V	-	1500	-	880	-	µs
t_{off}	turn-off time	$\overline{EN}$ to VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	34.6	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	34.6	-	-	-	ms
		$\overline{EN}$ to VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	34.6	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	34.6	-	-	-	ms
t_{TLH}	LOW to HIGH output transition time	VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	1000	-	670	-	µs
		$V_{I(VBUSI)}$ = 16 V	-	1500	-	880	-	µs
		VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	1000	-	510	-	µs
		$V_{I(VBUSO)}$ = 5.5 V	-	1000	-	590	-	µs
t_{THL}	HIGH to LOW output transition time	VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	33.0	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	33.0	-	-	-	ms
		VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	33.0	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	33.0	-	-	-	ms

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

14.1 Waveforms and test circuit



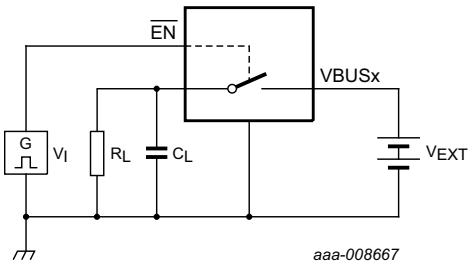
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 21. Switching times

Table 11. Measurement points

Supply voltage V_I		$\overline{EN}$ Input	Output	
VBUSI	**VBUSO**	**V_M**	**V_X**	**V_Y**
4.0 V to 16 V	4.0 V to 5.5 V	$0.5 \times V_{I(EN)}$	$0.1 \times V_{OH}$	$0.9 \times V_{OH}$



Test data is given in Table 12.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

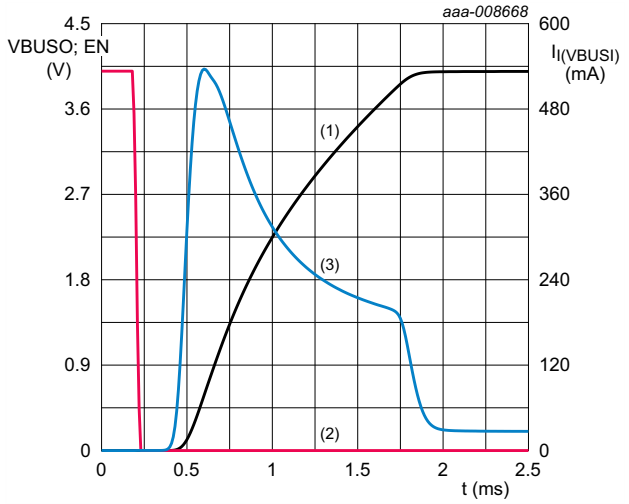
Fig 22. Test circuit for measuring switching times

Table 12. Test data

Supply voltage V_{EXT}		Input	Load	
VBUSI	**VBUSO**	**V_I**	**C_L**	**R_L**
4.0 V to 16 V	4.0 V to 5.5 V	1.5 V	100 µF	150 Ω

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



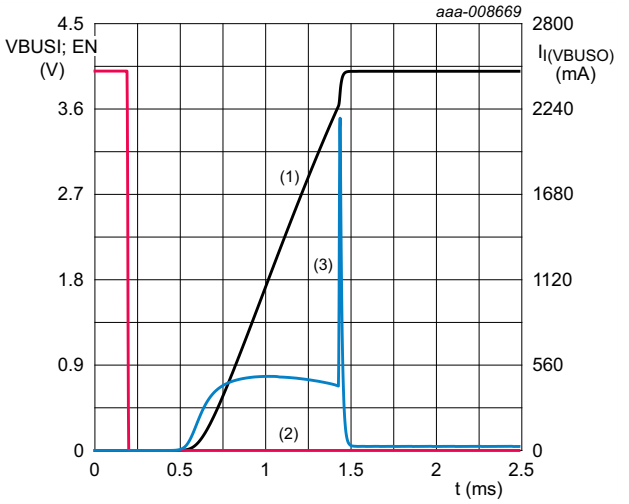
$V_{I(VBUSI)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 23. Enable time and in-rush current



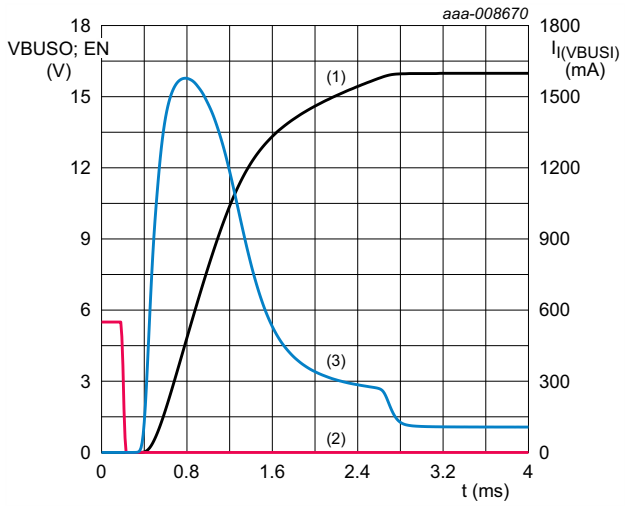
$V_{I(VBUSO)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

Fig 24. Enable time and in-rush current



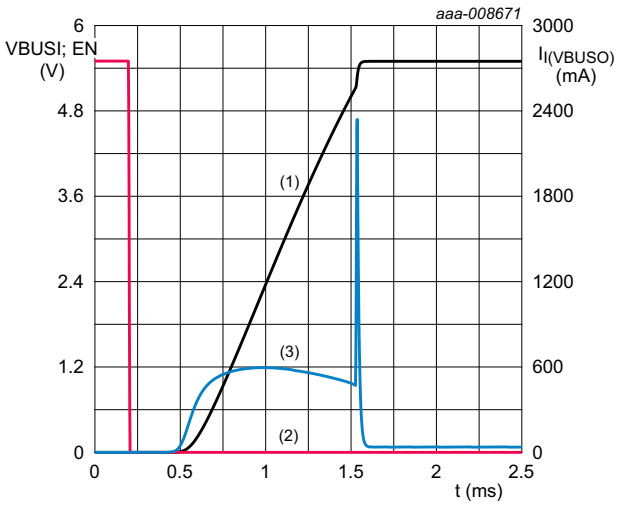
$V_{I(VBUSI)}$ = 16 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 25. Enable time and in-rush current



$V_{I(VBUSO)}$ = 5.5 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSI

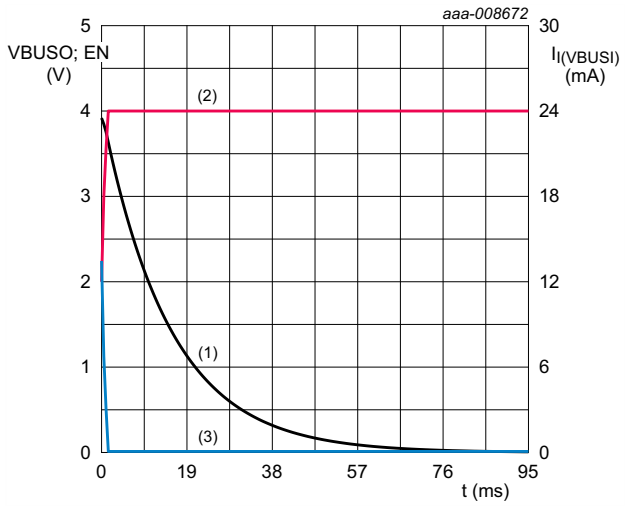
(2) EN

(3) $I_{I(VBUSO)}$

Fig 26. Enable time and in-rush current

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



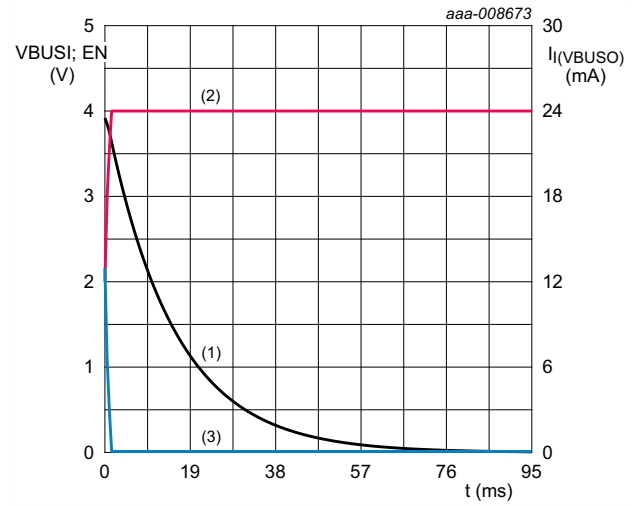
$V_{I(VBUSI)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 27. Disable time



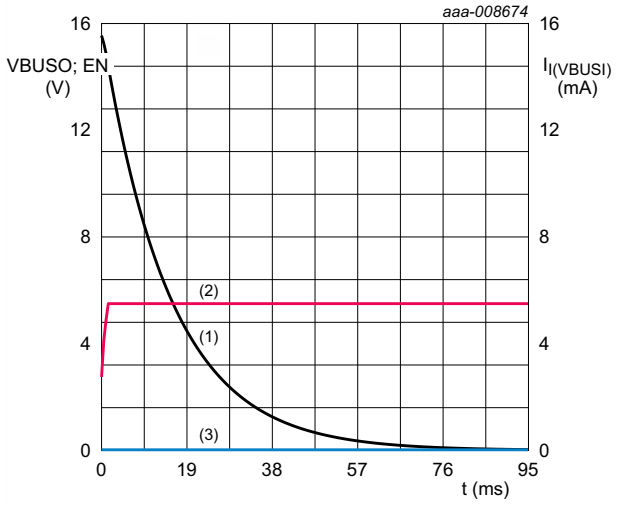
$V_{I(VBUSO)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

Fig 28. Disable time



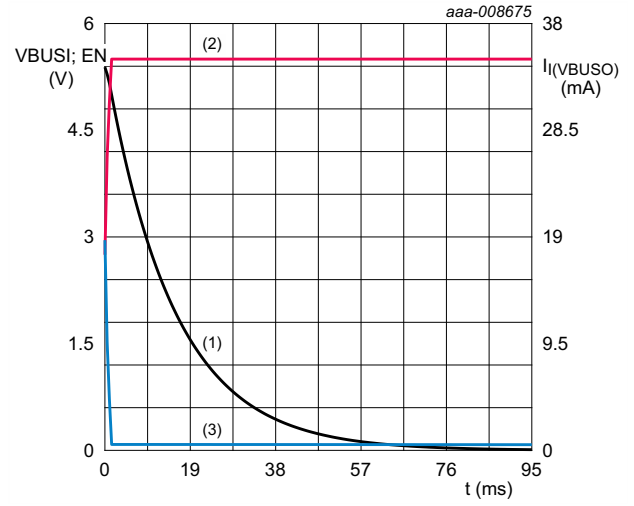
$V_{I(VBUSI)}$ = 16 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 29. Disable time



$V_{I(VBUSO)}$ = 5.5 V; R_L = 150 Ω; C_L = 100 µF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

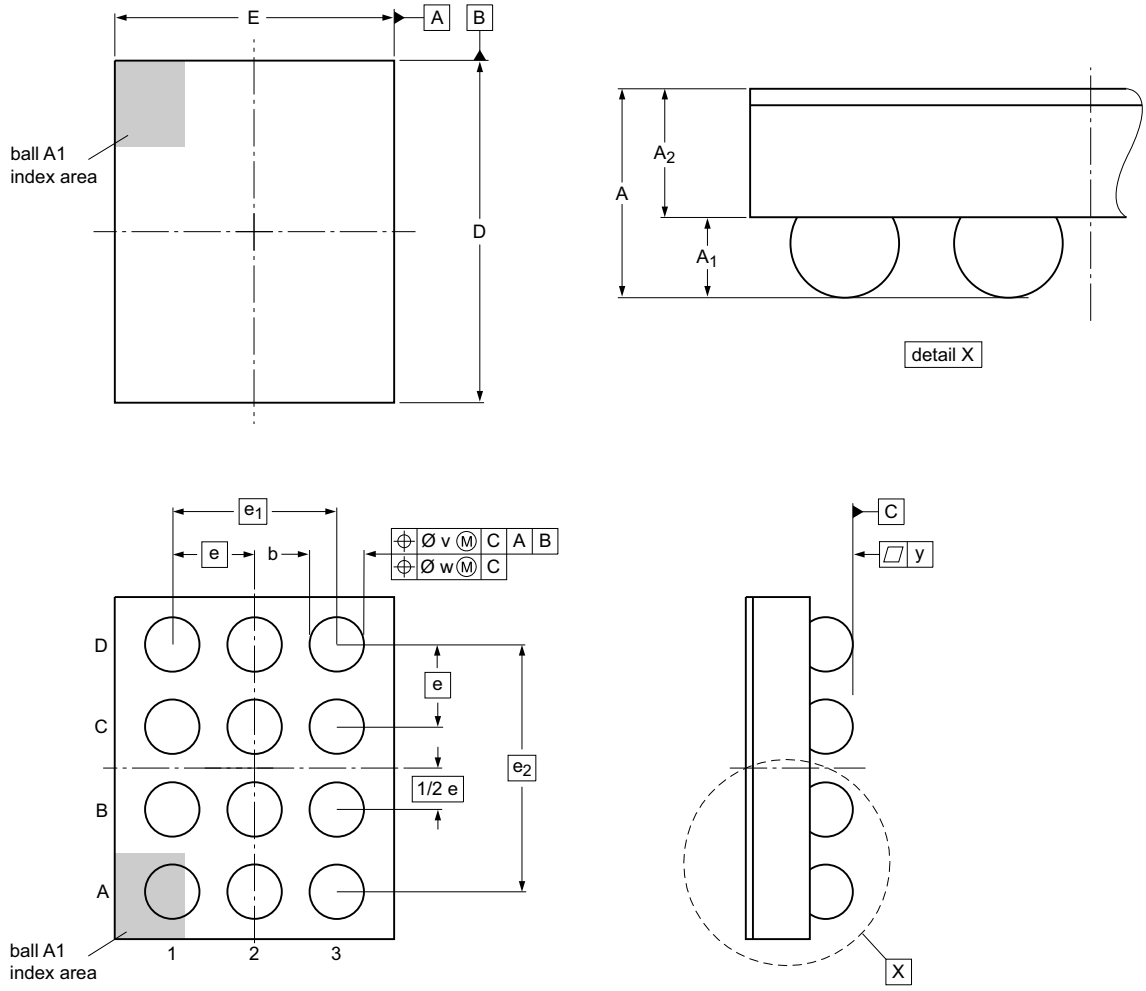
Fig 30. Disable time

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

15. Package outline

WLCSP12: wafer level chip-scale package;
12 bumps; 1.36 x 1.66 x 0.51 mm, 0.4 mm pitch (Backside coating included) **NX18P3001**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.55	0.23	0.34	0.29	1.69	1.39						
mm	nom	0.51	0.20	0.31	0.26	1.66	1.36	0.4	0.8	1.2	0.05	0.15	0.03
	min	0.47	0.17	0.29	0.23	1.63	1.33						

wlcsp12_nx18p3001_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX18P3001						~~13-03-29~~ 13-05-23

Fig 31. Package outline WLCSP12 package

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
OTP	OverTemperature Protection
USB-OTG	Universal Serial Bus On-The-Go
UVLO	UnderVoltage LockOut
OVLO	OverVoltage LockOut

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX18P3001 v.1	20130924	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

20. Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Marking 2
6 Functional diagram 2
7 Pinning information 3
7.1 Pinning 3
7.2 Pin description 3
8 Functional description 4
8.1 $\overline{EN}$-input 4
8.2 Undervoltage lockout 4
8.3 Overvoltage lockout 4
8.4 Overtemperature protection 4
8.5 ACK output 4
9 Application diagram 5
10 Limiting values 5
11 Recommended operating conditions 6
12 Thermal characteristics 6
13 Static characteristics 6
13.1 Graphs 8
13.2 ON resistance 10
13.3 ON resistance test circuit and graphs 11
14 Dynamic characteristics 12
14.1 Waveforms and test circuit 14
15 Package outline 17
16 Abbreviations 18
17 Revision history 18
18 Legal information 19
18.1 Data sheet status 19
18.2 Definitions 19
18.3 Disclaimers 19
18.4 Trademarks 20
19 Contact information 20
20 Contents 21

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 September 2013
Document identifier: NX18P3001