

# CD4066B Types

## COS/MOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

### High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V<sub>SS</sub> when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

### MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> ) (Voltages referenced to V <sub>SS</sub> Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V <sub>DD</sub> + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT (except for TRANSMISSION GATE which is 25 mA)	±10 mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> )	
For T <sub>A</sub> = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T <sub>A</sub> = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T <sub>A</sub> = -55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T <sub>A</sub> = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	
PACKAGE TYPES D, F, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

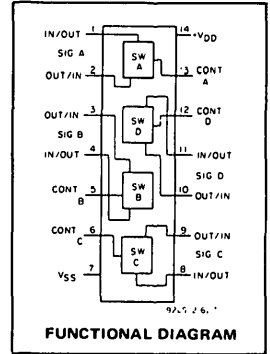
### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	3	18	V

### Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f<sub>is</sub> = 10 kHz, R<sub>L</sub> = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f<sub>is</sub> = 1 kHz, V<sub>is</sub> = 5 Vp-p, V<sub>DD</sub> - V<sub>SS</sub> ≥ 10 V, R<sub>L</sub> = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ V<sub>DD</sub> - V<sub>SS</sub> = 10 V, T<sub>A</sub> = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10<sup>12</sup> Ω typ.
- Low crosstalk between switches: -50 dB typ. @ f<sub>is</sub> = 8 MHz, R<sub>L</sub> = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"



### Applications:

- Analog signal switching/multiplexing
- Signal gating
- Modulator
- Squelch control
- Demodulator
- Chopper
- Commultiplexing switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

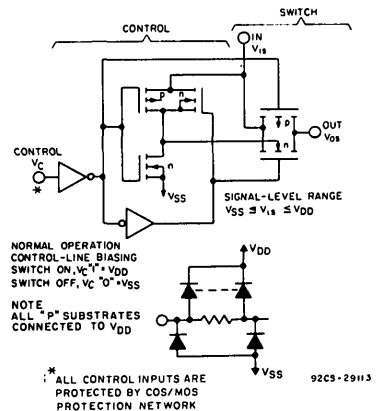


Fig. 1 - Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

# CD4066B Types

## ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	LIMITS AT INDICATED TEMPERATURES (°C)						UNITS		
				+25						
		V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125		Typ.	Max.
Quiescent Device Current, I <sub>DD</sub>		0,5	5	0,25	0,25	7,5	7,5	0,01	0,25	μA
		0,10	10	0,5	0,5	15	15	0,01	0,5	
		0,15	15	1	1	30	30	0,01	1	
		0,20	20	5	5	150	150	0,02	5	
Signal Inputs (V <sub>is</sub> ) and Output (V <sub>os</sub> )										
On-State Resistance, r <sub>on</sub> Max.	V <sub>C</sub> = V <sub>DD</sub> R <sub>L</sub> = 10 kΩ returned to V <sub>DD</sub> - V <sub>SS</sub> 2 V <sub>is</sub> = V <sub>SS</sub> to V <sub>DD</sub>	5	800	850	1200	1300	470	1050		Ω
		10	310	330	500	550	180	400		
		15	200	210	300	320	125	240		
Δ On-State Resistance Between Any 2 Switches, Δr <sub>on</sub>	R <sub>L</sub> = 10 kΩ, V <sub>C</sub> = V <sub>DD</sub>	5	-	-	-	-	15	-		Ω
		10	-	-	-	-	10	-		
		15	-	-	-	-	5	-		
Total Harmonic Distortion, THD	V <sub>C</sub> = V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V, V <sub>is</sub> (p-p) = 5 V (Sine wave centered on 0 V) R <sub>L</sub> = 10 kΩ, f <sub>is</sub> = 1 kHz sine wave	-	-	-	-	-	0,4	-		%
-3dB Cutoff Frequency (Switch on)	V <sub>C</sub> = V <sub>DD</sub> = 5 V, V <sub>SS</sub> = -5 V, V <sub>is</sub> (p-p) = 5 V (Sine wave centered on 0 V) R <sub>L</sub> = 1 kΩ	-	-	-	-	-	40	-		MHz
-50dB Feedthrough Frequency (Switch off)	V <sub>C</sub> = V <sub>SS</sub> = -5 V, V <sub>is</sub> (p-p) = 5 V Sine wave centered on 0 V R <sub>L</sub> = 1 kΩ	-	-	-	-	-	1	-		MHz
Input/Output Leakage Current (Switch off) I <sub>is</sub> Max.	V <sub>C</sub> = 0 V V <sub>is</sub> = 18 V; V <sub>os</sub> = 0 V, V <sub>is</sub> = 0 V; V <sub>os</sub> = 18 V	18	±0,1	±0,1	±1	±1	±10 <sup>-5</sup>	±0,1		μA
-50 dB Crosstalk Frequency	V <sub>C</sub> (A) = V <sub>DD</sub> = +5 V, V <sub>C</sub> (B) = V <sub>SS</sub> = -5 V, V <sub>is</sub> (A) = 5 V p-p, 50 Ω source R <sub>L</sub> = 1 kΩ	-	-	-	-	-	8	-		MHz
Propagation Delay (Signal Input to Signal Output) t <sub>pd</sub>	R <sub>L</sub> = 200 kΩ V <sub>C</sub> = V <sub>DD</sub> , V <sub>SS</sub> = GND, C <sub>L</sub> = 50 pF V <sub>is</sub> = 10 V (Square wave centered on 5 V t <sub>r</sub> , t <sub>f</sub> = 20 ns	5	-	-	-	-	20	40		ns
		10	-	-	-	-	10	20		
		15	-	-	-	-	7	15		
Capacitance: Input, C <sub>is</sub>	V <sub>DD</sub> = +5 V	-	-	-	-	-	8	-		pF
Output, C <sub>os</sub>	V <sub>C</sub> = V <sub>SS</sub> = -5 V	-	-	-	-	-	8	-		
Feedthrough, C <sub>ios</sub>		-	-	-	-	-	0,5	-		

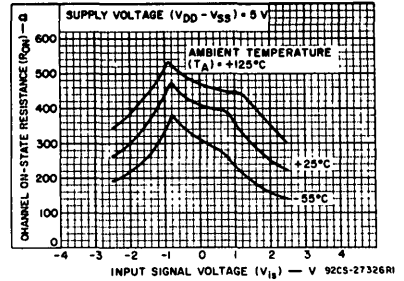


Fig. 2— Typical on-state resistance vs. input signal voltage (all types).

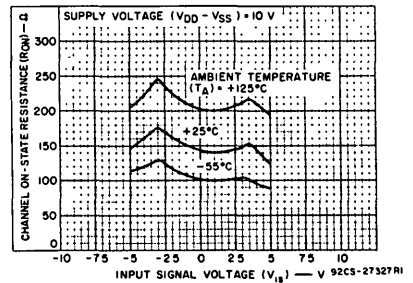


Fig. 3— Typical on-state vs. input signal voltage (all types).

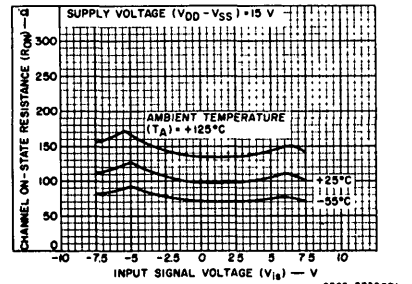


Fig. 4— Typical on-state resistance vs. input signal voltage (all types).

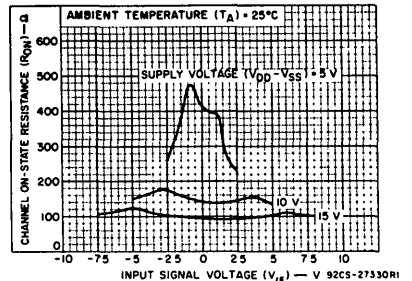


Fig. 5— on-state resistance vs. input signal voltage (all types).

# CD4066B Types

## ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	LIMITS AT INDICATED TEMPERATURES (°C)						UNITS
		Values at -55, +25, +125 Apply to D, F, H Packages					Values at -40, +25, +85 Apply to E Package	
		V <sub>DD</sub> (V)				+25		
		-55	-40	+85	+125	Typ.	Max.	
<b>Control (V<sub>C</sub>)</b>								
Control Input Low Voltage, V <sub>ILC</sub> Max.	I <sub>IS</sub>   < 10 μA V <sub>IS</sub> = V <sub>SS</sub> , V <sub>OS</sub> = V <sub>DD</sub> and V <sub>IS</sub> = V <sub>DD</sub> , V <sub>OS</sub> = V <sub>SS</sub>	5	1	1	1	1	-	1
		10	2	2	2	2	-	2
		15	2	2	2	2	-	2
Control Input High Voltage, V <sub>IHC</sub>	See Fig. 2	5	3.5 (Min.)					
		10	7 (Min.)					
		15	11 (Min.)					
Input Current, I <sub>IN</sub> Max.	V <sub>IS</sub> ≤ V <sub>DD</sub> V <sub>DD</sub> - V <sub>SS</sub> = 18 V V <sub>CC</sub> ≤ V <sub>DD</sub> - V <sub>SS</sub>	18	±0.1	±0.1	±1	±1	±10 <sup>-5</sup>	±0.1
Crosstalk (Control Input to Signal Output)	V <sub>C</sub> = 10 V (Sq. Wave) t <sub>r</sub> , t <sub>f</sub> = 20 ns R <sub>L</sub> = 10 kΩ	10	-	-	-	-	50	-
Turn-On Propagation Delay	V <sub>IN</sub> = V <sub>DD</sub> t <sub>r</sub> , t <sub>f</sub> = 20 ns C <sub>L</sub> = 50 pF R <sub>L</sub> = 1 kΩ	5	-	-	-	-	35	70
		10	-	-	-	-	20	40
		15	-	-	-	-	15	30
Maximum Control Input Repetition Rate	V <sub>IS</sub> = V <sub>DD</sub> , V <sub>SS</sub> = GND, R <sub>L</sub> = 1 kΩ to gnd, C <sub>L</sub> = 50 pF, V <sub>C</sub> = 10 V (Square wave centered on 5 V) t <sub>r</sub> , t <sub>f</sub> = 20 ns, V <sub>OS</sub> = ½ V <sub>OS</sub> @ 1 kHz	5	-	-	-	-	6	-
		10	-	-	-	-	9	-
		15	-	-	-	-	9.5	-
Input Capacitance, C <sub>IN</sub>						5	7.5	μF

V <sub>DD</sub> (V)	V <sub>IS</sub> (V)	Switch Input					Switch Output, V <sub>OS</sub> (V)	
		I <sub>IS</sub> (mA)					Min.	Max.
		-55°C	-40°C	+25°C	+85°C	+125°C		
5	0	0.64	0.61	0.51	0.42	0.36	-	0.4
5	5	-0.64	-0.61	-0.51	-0.42	-0.36	4.6	-
10	0	1.6	1.5	1.3	1.1	0.9	-	0.5
10	10	-1.6	-1.5	-1.3	-1.1	-0.9	9.5	-
15	0	4.2	4	3.4	2.8	2.4	-	1.5
15	15	-4.2	-4	-3.4	-2.8	-2.4	13.5	-

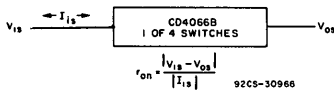


Fig. 6—Determination of  $r_{ON}$  as a test condition for control input high voltage (V<sub>IHC</sub>) specification.

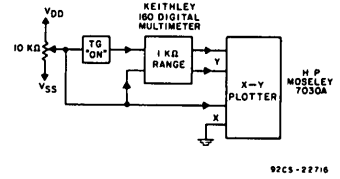


Fig. 7—Channel on-state resistance measurement circuit.

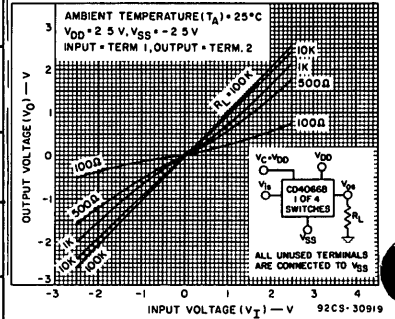


Fig. 8—Typical  $r_{ON}$  characteristics for 1 of 4 channels.

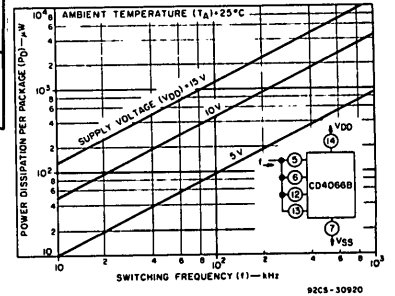


Fig. 9—Power dissipation per package vs. switching frequency.

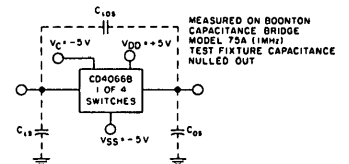


Fig. 10—Capacitance test circuit.



## CD4066B Types

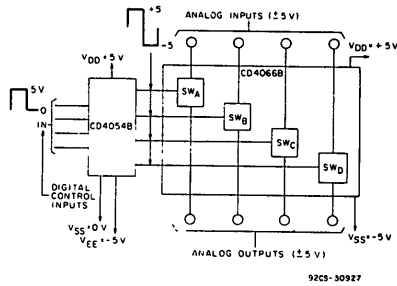
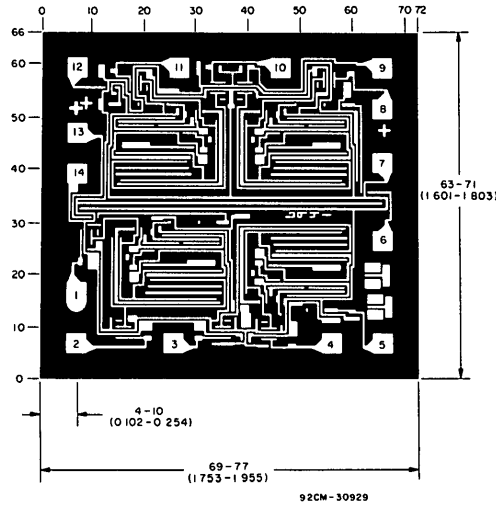


Fig. 18 — Bidirectional signal transmission via digital control logic.



CD4066BH  
CHIP PHOTOGRAPH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $5^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

### SPECIAL CONSIDERATIONS — CD4066B

1. In applications that employ separate power sources to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L$  = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the CD4066B.
2. In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from  $R_{ON}$  values shown). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminals 2,3,9, or 10.