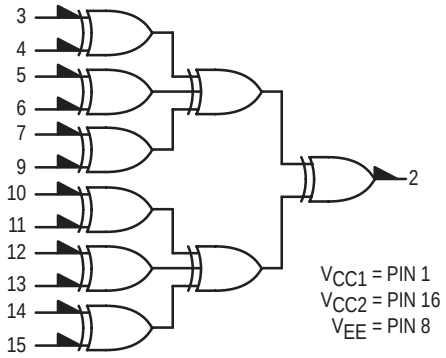
MC10160

12-Bit Parity Generator-Checker

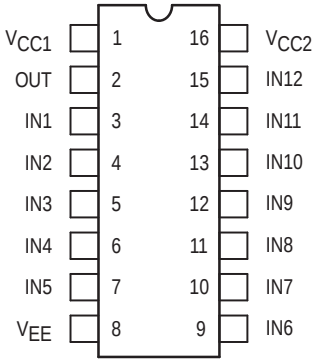
The MC10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

- P_D = 320 mW typ/pkg (No Load)
- t_{pd} = 5.0 ns typ
- t_r, t_f = 2.0 ns typ (20%–80%)

LOGIC DIAGRAM



DIP PIN ASSIGNMENT



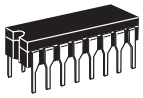
Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18.

INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

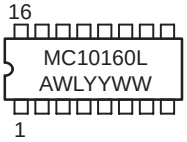
ON Semiconductor

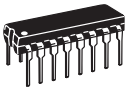
http://onsemi.com

MARKING DIAGRAMS

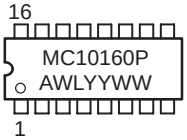


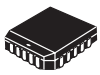
CDIP–16
L SUFFIX
CASE 620



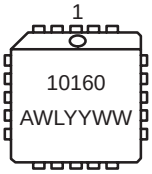


PDIP–16
P SUFFIX
CASE 648





PLCC–20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10160L	CDIP–16	25 Units / Rail
MC10160P	PDIP–16	25 Units / Rail
MC10160FN	PLCC–20	46 Units / Rail

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		86		62	78		86	mAdc
Input Current	I_{inH} (Note 1.)	3 4		425 350			265 220		265 220	μAdc
	I_{inL}	3	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	V_{OH}	2	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	2	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	2	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	2		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay	t_{3+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3+2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3–2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{3–2+}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	t_{4+2+}	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4+2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4–2–}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
	$t_{4–2+}$	2	1.8	8.1	2.0	5.0	7.5	2.0	8.0	
Rise Time (20 to 80%)	t_{2+}	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	
Fall Time (20 to 80%)	$t_{2–}$	2	1.1	3.5	1.1	2.0	3.3	1.0	3.5	

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

ELECTRICAL CHARACTERISTICS (continued)

@ Test Temperature			TEST VOLTAGE VALUES (Volts)					
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
–30°C			–0.890	–1.890	–1.205	–1.500	–5.2	
+25°C			–0.810	–1.850	–1.105	–1.475	–5.2	
+85°C			–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic	**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
			V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current	I_E	8	4,5,9, 10,13,14				8	1,16
Input Current	I_{inH}	3	3				8	1,16
	(Note 1.)	4	4				8	1,16
	I_{inL}	3		3			8	1,16
Output Voltage Logic 1	V_{OH}	2	3	4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Output Voltage Logic 0	V_{OL}	2		3,4,5,6,7,9,10, 11,12,13,14,15			8	1,16
Threshold Voltage Logic 1	V_{OHA}	2		4,5,6,7,9,10, 11,12,13,14,15	3		8	1,16
Threshold Voltage Logic 0	V_{OLA}	2		3,5,6,7,9,10, 11,12,13,14,15		4	8	1,16
Switching Times (50Ω Load)			**+1.11V**		**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	t_{3+2+}	2			3	2	8	1,16
	t_{3+2-}	2	4		3	2	8	1,16
	t_{3-2-}	2			3	2	8	1,16
	t_{3-2+}	2	4		3	2	8	1,16
	t_{4+2+}	2			4	2	8	1,16
	t_{4+2-}	2	3		4	2	8	1,16
	t_{4-2-}	2			4	2	8	1,16
	t_{4-2+}	2	3		4	2	8	1,16
Rise Time (20 to 80%)	t_{2+}	2			3	2	8	1,16
Fall Time (20 to 80%)	t_{2-}	2			3	2	8	1,16

1. Pins 3, 6, 7, 11, 12, 15 are similar. Pins 4, 5, 9, 10, 13, 14 are similar.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.