Data Sheet | August 6, 2007 | FN9101.6

Precision Single-Phase Buck PWM Controller for Intel Mobile Voltage Positioning IMVP-IV™ and IMVP-IV+™

The ISL6218 Single-Phase Buck PWM control IC, with integrated half bridge gate driver, provides a precision voltage regulation system for advanced Pentium-M microprocessors in notebook computers. This control IC also features both input voltage feed-forward and average current mode control for excellent dynamic response, "Loss-less" current sensing using MOSFET $r_{DS(ON)}$, and user selectable switching frequencies from 250kHz to 500kHz per phase.

The ISL6218 includes a 6-bit digital-to-analog converter (DAC) that dynamically adjusts the CORE PWM output voltage from 0.700V to 1.708V in 16mV steps, and conforms to the Intel IMVP-IV™ mobile VID specification. The ISL6218 also has logic inputs to select Active, Deep Sleep and Deeper Sleep modes of operation. A precision reference, remote sensing and proprietary architecture with integrated processor-mode compensated "Droop" provides excellent static and dynamic CORE voltage regulation.

Another feature of the ISL6218 IC controller is the internal PGOOD delay circuit that holds the PGOOD pin low for 3ms to 12ms after the VCCP and VCC_MCH regulators are within regulation. This PGOOD signal is masked during VID changes. Output overvoltage and undervoltage are monitored and result in the converter latching off and PGOOD signal being held low.

The overvoltage and undervoltage thresholds are 112% and 84% of the VID, Deep or Deeper Sleep setpoint. Overcurrent protection features a 32 cycle overcurrent shutdown. PGOOD, Overvoltage, Undervoltage and Overcurrent provide monitoring and protection for the microprocessor and power system. The ISL6218 IC is available in a 38 Ld TSSOP and 40 Ld QFN package.

Features

- IMVP-IV™ Compliant CORE Regulator
- Single-Phase Power Conversion
- "Loss-less" Current Sensing for Improved Efficiency and Reduced Board Area
  - Optional Discrete Precision Current Sense Resistor
- Internal Gate Drive and Boot-Strap Diode
- Precision CORE Voltage Regulation
  - 0.8% System Accuracy Over-temperature
- 6-Bit Microprocessor Voltage Identification Input
- Programmable "Droop" and CORE Voltage Slew Rate to Comply with IMVP-IV™ Specification
- Discontinuous Mode Of Operation for Increased Light Load Efficiency in Deep and Deeper Sleep Mode
- Direct Interface with System Logic ($\overline{STP}\_\overline{CPU}$ and DPRSLPVR) for Deep and Deeper Sleep Modes of Operation
- Easily Programmable Voltage Setpoints for Initial "Boot", Deep Sleep and Deeper Sleep Modes
- Excellent Dynamic Response
  - Combined Voltage Feed-Forward and Average Current Mode Control
- Overvoltage, Undervoltage and Overcurrent Protection
- Power-good Output with Internal Blanking During VID and Mode Changes
- User Programmable Switching Frequency of 250kHz to 500kHz
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

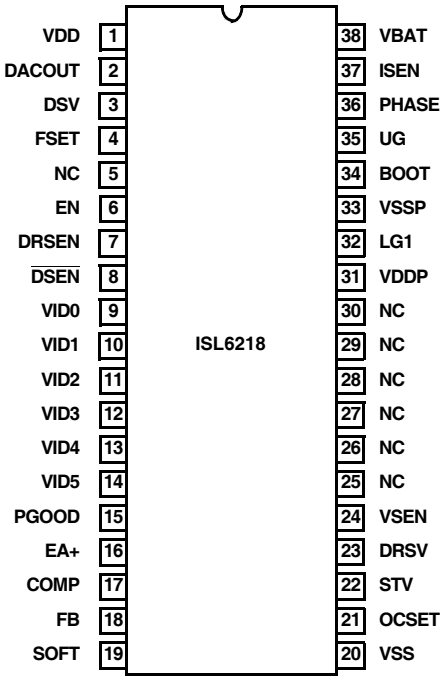
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG #
ISL6218CV*	ISL 6218CV	-10 to +85	38 Ld TSSOP	M38.173
ISL6218CVZ* (Note)	ISL 6218CVZ	-10 to +85	38 Ld TSSOP (Pb-free)	M38.173
ISL6218CVZA* (Note)	ISL 6218CVZ	-10 to +85	38 Ld TSSOP (Pb-free)	M38.173
ISL6218CRZ* (Note)	ISL62 18CRZ	-10 to +85	40 Ld 6x6 QFN (Pb-free)	L40.6x6

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

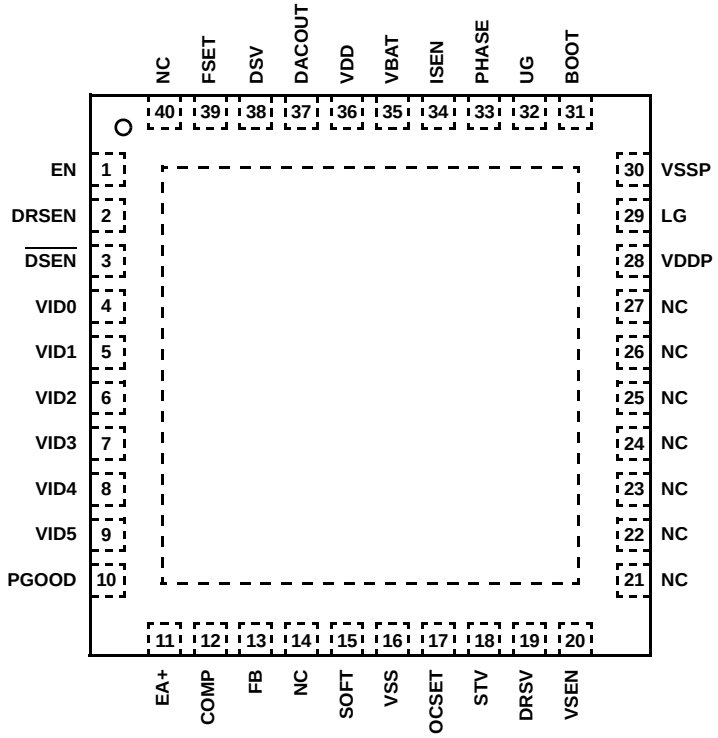
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL6218
(38 LD TSSOP)
TOP VIEW



ISL6218
(40 LD QFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage VDD, VDDP . . . . . -0.3 to +7V
Battery Voltage, VBAT . . . . . +25V
Boot1 and UGATE1 . . . . . +33V
Phase1 and ISEN1 . . . . . +28V
Boot1 with respect to Phase1 . . . . . +6.5V
UGATE1. . . . . (Phase1 - 0.3V) to (Boot1 + 0.3V)
All other pins . . . . . -0.3V to (VDD + 0.3V)

Recommended Operating Conditions

Supply Voltage, VDD, VDDP . . . . . +5V ±5%
Battery Voltage, VBAT . . . . . +5.6V to 21V
Ambient Temperature. . . . . -10°C to +85°C
Junction Temperature . . . . . -10°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TSSOP Package (Note 1)	72	N/A
QFN Package (Notes 2, 3)	32	4.5

Maximum Operating Junction Temperature. . . . . +125°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Limits established by characterization and are not production tested.

Electrical Specifications

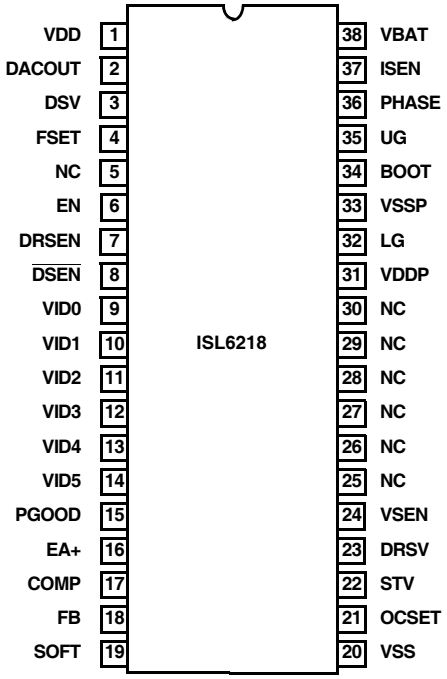
Operating Conditions: V_{DD} = 5V, T_A = -10°C to +85°C, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Input Supply Current, I(VDD)	EN = 3.3V, $\overline{DSEN}$ = 0, DRSEN = 0	-	1.4	-	mA
	EN = 0V	-	1	-	µA
POR (Power-On Reset) Threshold	VDD Rising	4.39	4.45	4.5	V
	VDD Falling	4.10	4.20	4.37	V
REFERENCE AND DAC					
System Accuracy	Percent system deviation from programmed VID Codes @ 1.356	-0.8	-	0.8	%
DAC (VID0 to VID5) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.3	V
DAC (VID0 to VID5) Input High Voltage	DAC Programming Input High Threshold Voltage	0.7	-	-	V
Maximum Output Voltage		-	1.708	-	V
Minimum Output Voltage		-	0.70	-	V
CHANNEL GENERATOR					
Frequency, f_{SW}	R_{Fset} = 243k, ±1%	225	250	275	kHz
Adjustment Range		250	-	500	kHz
ERROR AMPLIFIER					
DC Gain		-	100	-	dB
Gain-Bandwidth Product	C_L = 20pF	-	18	-	MHz
Slew Rate	C_L = 20pF	-	4.0	-	V/µs

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +85°C, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ISEN					
Full Scale Input Current		-	32	-	µA
Overcurrent Threshold	ROCSET = 110k (see Figure 10)	-	54	-	µA
Soft-Start Current	SOFT = 0V	-	31	-	µA
Droop Current	ISEN = 32µA	12.0	14	16.0	µA
GATE DRIVER					
UGATE Source Resistance	500mA Source Current	-	1	1.5	Ω
UGATE Source Current (Note 4)	$V_{UGATE-PHASE}$ = 2.5V	-	2	-	A
UGATE Sink Resistance	500mA Sink Current	-	1	1.5	Ω
UGATE Sink Current (Note 4)	$V_{UGATE-PHASE}$ = 2.5V	-	2	-	A
LGATE Source Resistance	500mA Source Current	-	1	1.5	Ω
LGATE Source Current (Note 4)	V_{LGATE} = 2.5V	-	2	-	A
LGATE Sink Resistance	500mA Sink Current	-	0.5	0.8	Ω
LGATE Sink Current (Note 4)	V_{LGATE} = 2.5V	-	4	-	A
BOOTSTRAP DIODE					
Forward Voltage	VDDP = 5V, Forward Bias Current = 10mA	0.57	0.68	0.74	V
POWER GOOD MONITOR					
PGOOD Sense Current		2.43	-	-	mA
PGOOD Pull-Down MOSFET $r_{DS(ON)}$		56	63	82	Ω
Undervoltage Threshold (VSEN/VREF)	VSEN Rising	-	85.0	-	%
Undervoltage Threshold (VSEN/VREF)	VSEN Falling	-	84.0	-	%
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	0.26	0.4	V
LOGIC THRESHOLD					
EN, $\overline{DSEN}$, DRSEN Low		-	-	1	V
EN, $\overline{DSEN}$, DRSEN High		2	-	-	V
PROTECTION					
Overvoltage Threshold (V_{SEN}/V_{REF})	V_{SEN} Rising	-	112.0	-	%
DELAY TIME					
Delay Time from LGATE Falling to UGATE Rising	VDDP = 5V, BOOT to PHASE = 5V, UGATE - PHASE = 1V, LGATE = 1V	10	18	30	ns
Delay Time from UGATE Falling to LGATE Rising	VDDP = 5V, BOOT to PHASE = 5V, UGATE - PHASE = 1V, LGATE = 1V	10	18	30	ns

Functional Pin Description 38 Ld TSSOP



VDD

This pin is used to connect +5V to the IC to supply all power necessary to operate the chip. The IC starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold.

VDDP

This pin provides a low ESR bypass connection to the internal gate drivers for the +5V source.

PGOOD

This pin is used as an input and an output and is tied to the Vccp and Vcc_mch PGOOD signals. During start-up, this pin is recognized as an input, and prevents further slewing of the output voltage from the “Boot” level until PGOOD from Vccp and Vcc_mch is enabled High. After start-up, this pin has an open drain output used to indicate the status of the CORE output voltage. This pin is pulled low when the system output is outside of the regulation limits. PGOOD includes a timer for power-on delay.

EN

This pin is connected to the system signal VR_ON and provides the enable/disable function for the PWM controller.

OCSET

A resistor from this pin to ground sets the overcurrent protection threshold. The current from this pin should be between 10µA and 25µA (70kΩ to 175kΩ equivalent pull-down resistance).

VSEN

This pin is used for remote sensing of the microprocessor CORE voltage.

COMP

This pin provides connection to the error amplifier output.

FB

This pin is connected to the inverting input of the error amplifier.

EA+

This pin is connected to the non-inverting input of the error amplifier and is used for setting the “Droop” voltage.

STV

The voltage on this pin sets the initial start-up or “Boot” voltage.

SOFT

This pin programs the slew rate of VID changes, Deep Sleep and Deeper Sleep transitions, and soft-start after initializing. This pin is connected to ground via a capacitor, and to EA+ through an external “Droop” resistor.

$\overline{\text{DSEN}}$

This pin connects to system logic “$\overline{\text{STP}}\_\overline{\text{CPU}}$” and enables Deep Sleep mode of operation. Deep Sleep is enabled when a logic LOW signal is detected on this pin.

DRSEN

This pin connects to system logic “DPRSLPVR” and enables Deeper Sleep mode of operation when a logic HIGH is detected on this pin.

VBAT

Voltage on this pin provides feed-forward battery information that adjusts the oscillator ramp amplitude.

FSET

A resistor from this pin to ground programs the switching frequency.

ISEN

This pin is used as current sense input from the converter channel phase node.

DACOUT

This pin provides access to the output of the Digital-to-Analog Converter.

DSV

The voltage on this pin provides the setpoint for output voltage during Deep Sleep Mode of operation.

DRSV

The voltage on this pin provides the setpoint for output voltage during Deeper Sleep Mode of operation.

VID0, VID1, VID2, VID3, VID4, VID5

These pins are used as inputs to the 6-bit Digital-to-Analog converter (DAC). VID0 is the least significant bit and VID5 is the most significant bit.

UG

This pin is the gate drive output to the high side MOSFETs.

LG

This pin is the gate drive output to the low side MOSFETs.

BOOT

This pin is connected to the Bootstrap capacitor for upper gate drive.

PHASE

This pin is connected to the phase node of the power channel.

VSSP

This pin is the return for the lower gate drive and is connected to power ground.

VSS

This pin provides connection for signal ground.

Typical Application

Figure 1 shows a Single-Phase Synchronous Buck Converter circuit used to provide “CORE” voltage regulation for the Intel Pentium-M mobile processor using IMVP-IV™ voltage positioning.

The circuit shows pin connections for the ISL6218 PWM controller in the 38 Ld TSSOP package.

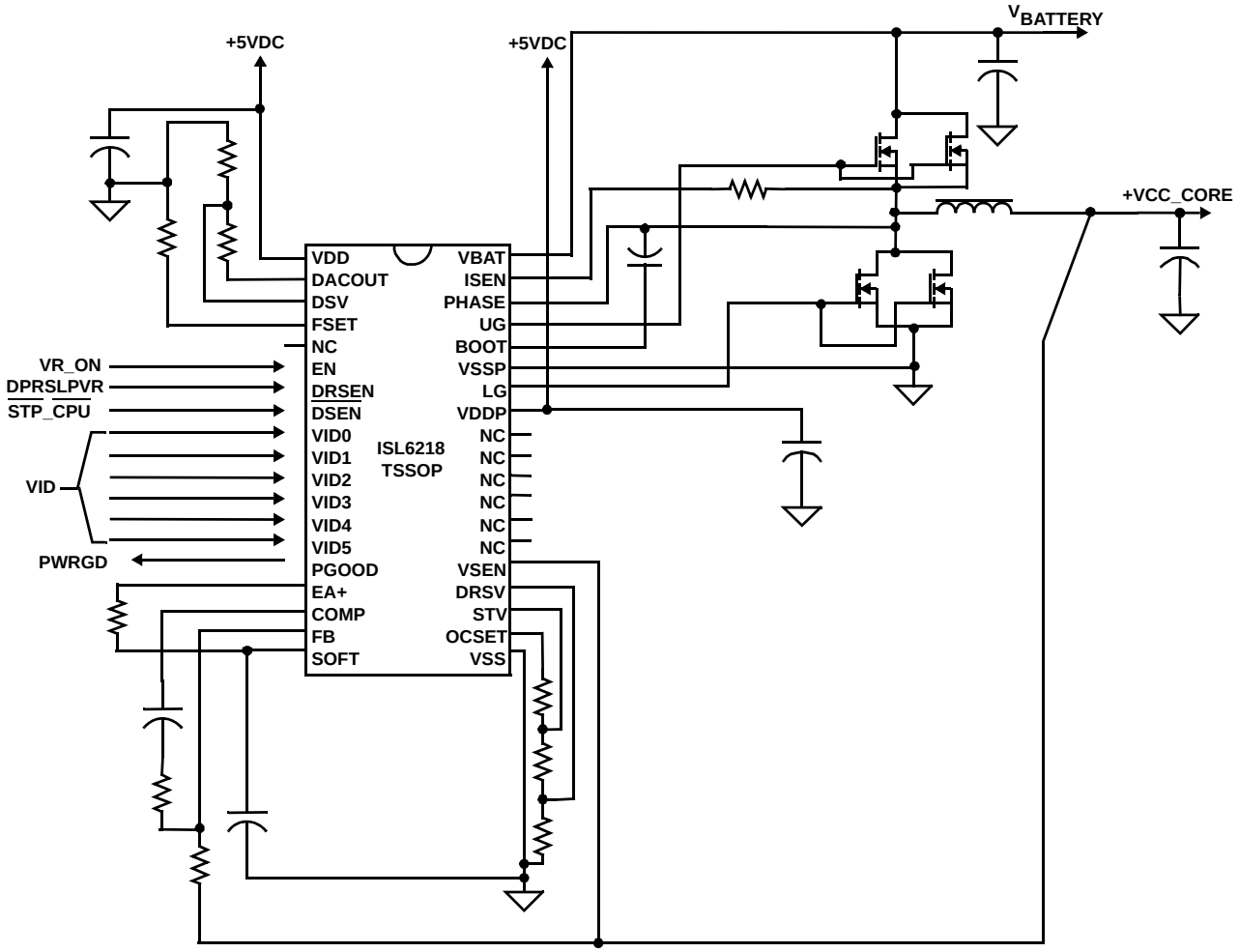
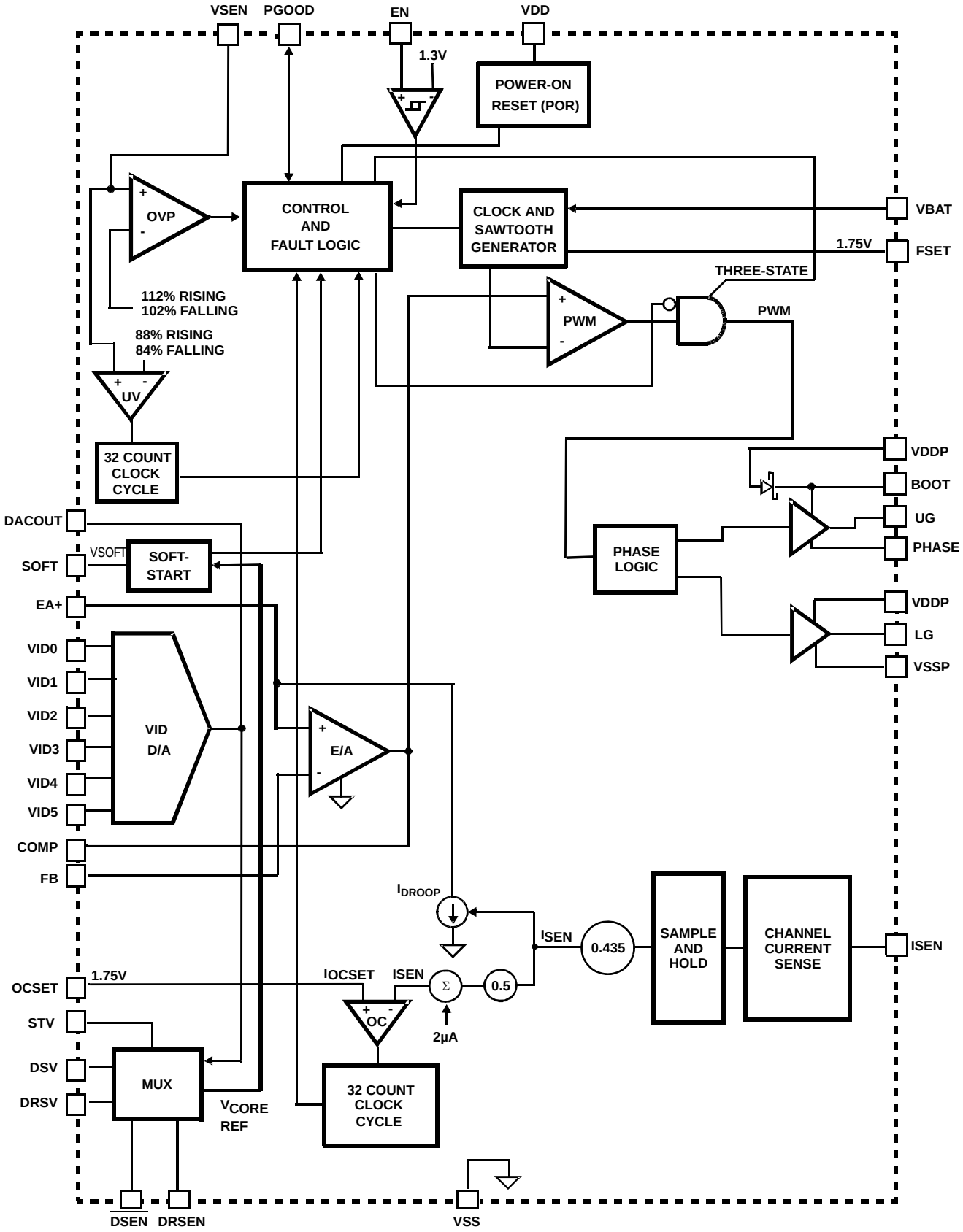


FIGURE 1. TYPICAL APPLICATION CIRCUIT FOR ISL6218 SINGLE-PHASE PWM CONTROLLER

Block Diagram



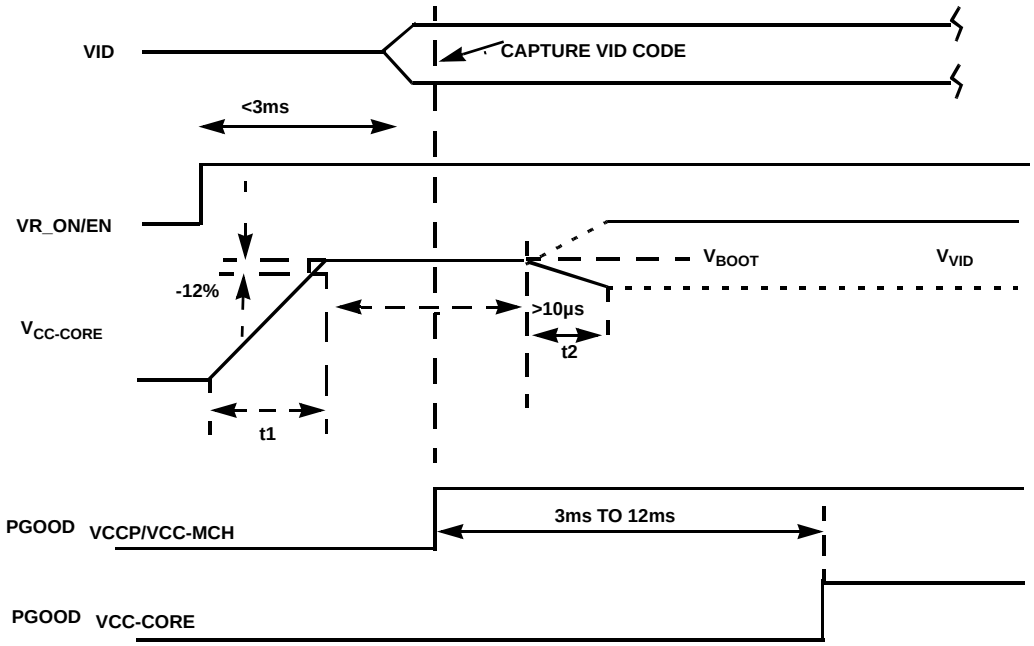


FIGURE 2. TIMING DIAGRAM SHOWING VR_ON, VCC_CORE AND PGOOD FOR VCC_CORE, VCCP AND VCC_MCH

Theory of Operation

Initialization

Once the +5VDC supply voltage (as connected to the ISL6218 VDD pin) reaches the Power-On Reset (POR) rising threshold, the PWM drive signals are held in "Three-State" or high impedance mode. This results in both the high side and low side MOSFETs being held off. Once the supply voltage exceeds the POR rising threshold, the controller will respond to a logic level high on the EN pin and initiate the soft-start interval. If the supply voltage drops below the POR falling threshold, POR shutdown is triggered and the PWM outputs are again driven to "Three-State".

The system signal, VR_ON is directly connected to the EN pin of the ISL6218. Once the voltage on the EN pin rises above 2.0V, the chip is enabled and soft-start begins. The EN pin of the ISL6218 is also used to reset the ISL6218 for cases when an undervoltage or overcurrent fault condition has latched the IC off. Toggling the state of this pin to a level below 1.0V will re-enable the IC. For the case of an overvoltage fault, the VDD pin must be reset.

During start-up, the ISL6218 regulates to the voltage on the STV pin. This is referred to as the "Boot" voltage and is labeled VBOOT in Figure 2. Once power good signals are received from the Vccp and Vcc_mch regulators, the ISL6218 will capture the VID code and regulate, within 3ms to 12ms, to this command voltage. The PGOOD pin of the ISL6218 is both an input and an output and is further described in "Fault Protection" on page 13.

Soft-Start Interval

Refer to Figure 2 and Figure 4. Once VDD rises above the POR rising threshold and the EN pin voltage is above the threshold of 2.0V, a soft-start interval is initiated. The voltage on the EA+ pin is the reference voltage for the regulator. The voltage on the EA+ pin is equal to the voltage on the SOFT pin minus the "Droop" resistor voltage, V_{DROOP}. During start-up, when the voltage on SOFT is less than the "Boot" voltage V_{BOOT}, a 130µA current source I1, is used to slowly ramp up the voltage on the soft-start capacitor C_{SOFT}. This slowly ramps up the reference voltage for the controller, and controls the slew rate of the output voltage. The STV pin is externally programmable and sets the start-up or "Boot" voltage V_{BOOT}. The programming of this voltage level is explained in "STV, DSV and DRSV" on page 12.

The ISL6218 PGOOD pin is both an input and an output. The system signal IMVP4_PWRGD is connected to power good signals from the Vccp and Vcc_mch supplies. The Intersil ISL6225 Dual Voltage Regulator is an ideal choice for the Vccp and Vcc_mch supplies.

Refer to Figure 2 and Figure 4. Once the output voltage is within the "Boot" level regulation limits and a logic high PGOOD signal from the Vccp and Vccp_mch regulators is received, the ISL6218 is enabled to capture the VID code and regulate to that command voltage.

The "Droop" current source I_{DROOP}, is proportional to load current. This current source is used to reduce the reference voltage on EA+ by the voltage drop across the "Droop" resistor. A more in-depth explanation of "Droop" and the sizing of this resistor can be found in "Droop Compensation" on page 14.

The choice of value for soft-start capacitor is determined by the maximum slew rate required for the application. An example calculation is shown in Equation 1. Using the I1 current source on the SOFT pin as 130µA, and the slew rate of (10mV/µs), the SOFT capacitor is calculated in Equation 1:

$$C_{SOFT} = \frac{I_{SOURCE}}{SlewRate} = 130\mu A \cdot \frac{1\mu s}{10mV} \approx 0.012\mu F \quad \text{(EQ. 1)}$$

Gate Drive Signals

The ISL6218 provides internal gate drive for a single channel, Synchronous Buck, Core Regulator.

The ISL6218 was designed with a 4A, low side gate current sink ability, and a 2A, low-side gate current source ability to efficiently drive the latest, high performance MOSFETs. This feature will provide the system designer with flexibility in MOSFET selection as well as optimum efficiency during all modes of operation.

Frequency Setting

The power channel switching frequency is set up by a resistor from the FSET pin to ground. The choice of FSET resistance for a desired switching frequency can be approximated using Figure 3. The switching frequency is designed to operate between 250kHz and 500kHz per phase.

CORE Voltage Programming

The voltage identification pins (VID0, VID1, VID2, VID3, VID4 and VID5) set the DAC output voltage. These pins do not have internal pull-up or pull-down capability. These pins will recognize 1.0V, 3.3V or 5.0V CMOS logic. Table 1 shows the command voltage, V_{DAC} for the 6 bit VID codes.

The IC responds to VID code changes as shown in Figure 5. PGOOD is masked between these transitions.

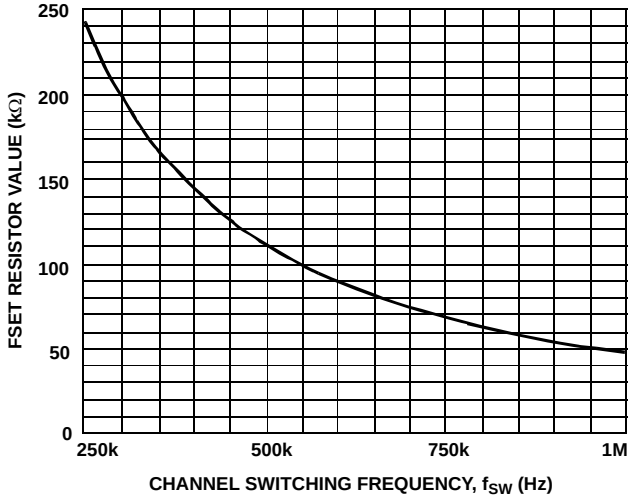


FIGURE 3. CHANNEL SWITCHING FREQUENCY vs R_{FSET}

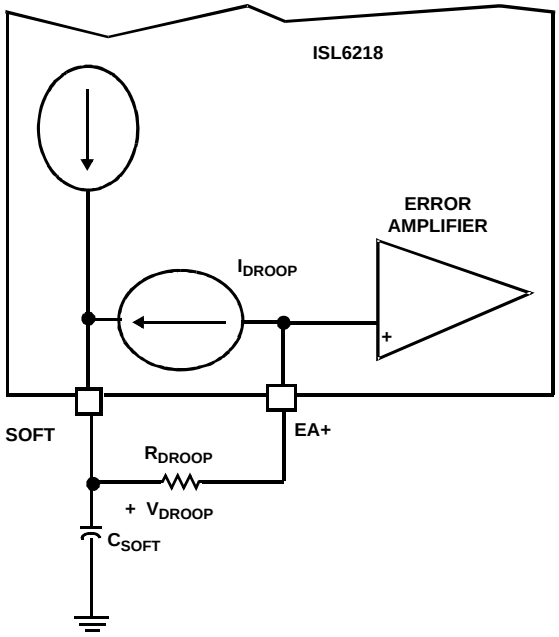


FIGURE 4. SOFT-START TRACKING CIRCUITRY SHOWING INTERNAL CURRENT SOURCES AND "DROOP" FOR ACTIVE, DEEP AND DEEPER SLEEP MODES OF OPERATION

TABLE 1. INTEL IMPV-IV VID CODES

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	1.708
0	0	0	0	0	1	1.692
0	0	0	0	1	0	1.676
0	0	0	0	1	1	1.660
0	0	0	1	0	0	1.644
0	0	0	1	0	1	1.628
0	0	0	1	1	0	1.612
0	0	0	1	1	1	1.596
0	0	1	0	0	0	1.580
0	0	1	0	0	1	1.564
0	0	1	0	1	0	1.548
0	0	1	0	1	1	1.532
0	0	1	1	0	0	1.516
0	0	1	1	0	1	1.500
0	0	1	1	1	0	1.484
0	0	1	1	1	1	1.468
0	1	0	0	0	0	1.452
0	1	0	0	0	1	1.436
0	1	0	0	1	0	1.420
0	1	0	0	1	1	1.404

TABLE 1. INTEL IMPV-IV VID CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	1	0	0	1.388
0	1	0	1	0	1	1.372
0	1	0	1	1	0	1.356
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	0	1	1.308
0	1	1	0	1	0	1.292
0	1	1	0	1	1	1.276
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	0	1.228
0	1	1	1	1	1	1.212
1	0	0	0	0	0	1.196
1	0	0	0	0	1	1.180
1	0	0	0	1	0	1.164
1	0	0	0	1	1	1.148
1	0	0	1	0	0	1.132
1	0	0	1	0	1	1.116
1	0	0	1	1	0	1.100
1	0	0	1	1	1	1.084
1	0	1	0	0	0	1.068
1	0	1	0	0	1	1.052
1	0	1	0	1	0	1.036
1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.004
1	0	1	1	0	1	0.988
1	0	1	1	1	0	0.972
1	0	1	1	1	1	0.956
1	1	0	0	0	0	0.940
1	1	0	0	0	1	0.924
1	1	0	0	1	0	0.908
1	1	0	0	1	1	0.892
1	1	0	1	0	0	0.876
1	1	0	1	0	1	0.860
1	1	0	1	1	0	0.844
1	1	0	1	1	1	0.828
1	1	1	0	0	0	0.812
1	1	1	0	0	1	0.796
1	1	1	0	1	0	0.780
1	1	1	0	1	1	0.764

TABLE 1. INTEL IMPV-IV VID CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	0	0	0.748
1	1	1	1	0	1	0.732
1	1	1	1	1	0	0.716
1	1	1	1	1	1	0.700

Active, Deep Sleep and Deeper Sleep Modes

The ISL6218 Single-Phase Controller is designed to control the CORE output voltage as per the IMVP-IV™ specifications for Active, Deep Sleep, and Deeper Sleep Modes of Operation.

After initial start-up, a logic high signal on $\overline{\text{DSEN}}$ and a logic low signal on DRSEN signals the ISL6218 to operate in Active mode (refer to Table 2). This mode will recognize VID code changes and regulate the output voltage to these command voltages.

A logic low signal present on $\overline{\text{STPCPU}}$ (pin $\overline{\text{DSEN}}$), with a logic low signal on DPRSLPVR (pin DRSEN) signals the ISL6218 to reduce the CORE output voltage to the Deep Sleep level, the voltage on the DSV pin.

A logic high on DPRSLPVR (pin DRSEN), with a logic low signal on $\overline{\text{STPCPU}}$ (pin $\overline{\text{DSEN}}$), signals the ISL6218 controller to further reduce the CORE output voltage to the Deeper Sleep level, which is the voltage on the DRSV pin.

Deep Sleep and Deeper Sleep voltage levels are programmable and are explained in “STV, DSV and DRSV” on page 12.

TABLE 2. OUTPUT VOLTAGE AS A FUNCTION OF $\overline{\text{DSEN}}$ AND DRSEN LOGIC STATES

$\overline{\text{DSEN}}$ - $\overline{\text{STP\_CPU}}$	DRSEN - DPRSLPVR	MODE OF OPERATION	OUTPUT VOLTAGE
1	0	Active	VID
0	0	Deep Sleep	DSV
0	1	Deeper Sleep	DRSV
1	1	Deeper Sleep	DRSV

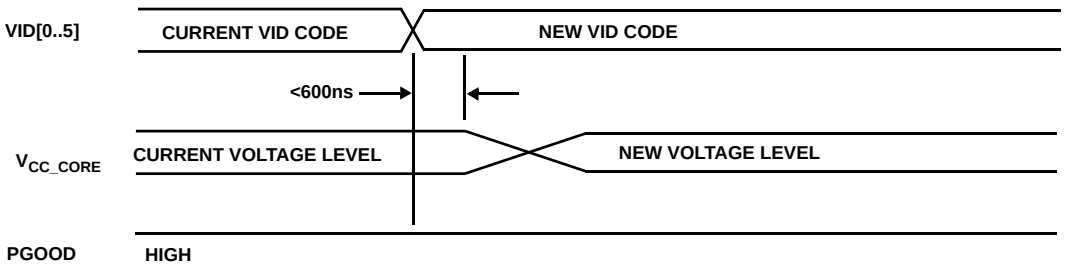


FIGURE 5. PLOT SHOWING TIMING OF VID CODE CHANGES AND CORE VOLTAGE SLEWING AS WELL AS PGOOD MASKING

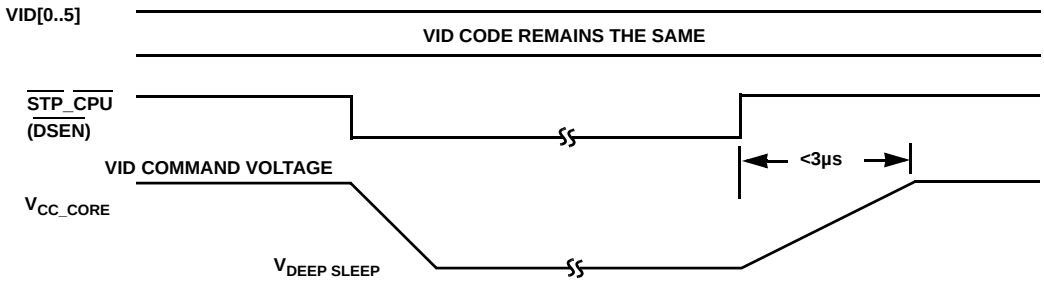


FIGURE 6. CORE VOLTAGE SLEWING TO 98.8% OF PROGRAMMED VID VOLTAGE FOR A LOGIC LEVEL LOW ON $\overline{DSEN}$

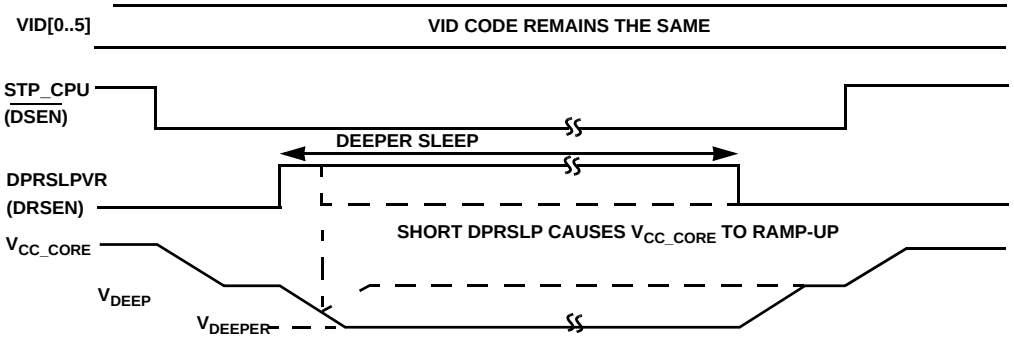


FIGURE 7. VCORE RESPONSE FOR DEEPER SLEEP COMMAND

Deep Sleep $\overline{Enable}$ ($\overline{DSEN}$) and Deeper Sleep Enable (DRSEN)

Table 2 shows logic states controlling modes of operation Figure 6 and Figure 5 show the timing for transitions entering and exiting Deep Sleep Mode and Deeper Sleep Mode, controlled by the system signals $\overline{STPCPU}$ and DPRSLPVR. Pins $\overline{DSEN}$ (Deep Sleep $\overline{Enable}$) and DRSEN (Deeper Sleep Enable) of the ISL6218 are connected to these 2 signals, respectively.

For the case when $\overline{DSEN}$ is logic high, and DRSEN is logic low, the controller will operate in Active Mode and regulate the output voltage to the VID commanded DAC voltage minus the voltage “Droop” as determined by the load current. Voltage “Droop” is the reduction of output voltage proportional to output current.

When a logic low is seen on the $\overline{DSEN}$ and DRSEN is logic low the controller will then regulate the output voltage to the voltage seen on the DSV pin minus “Droop”.

When $\overline{DSEN}$ is logic low and DRSEN is logic high the controller will operate in Deeper Sleep mode. The ISL6218 will then regulate to the voltage seen on the DRSV pin minus “Droop”.

Deep and Deeper Sleep voltage levels are programmable and explained in “STV, DSV and DRSV” on page 12.

DISCONTINUOUS OPERATION - $\overline{PSI}$

The ISL6218 Single-Phase PWM controller is a Synchronous Buck Regulator. However, in Deep and Deeper Sleep modes where the load current is low, the controller operates as a standard buck regulator. This mode of operation acts to eliminate negative inductor current by truncating the low side MOSFET gate drive pulse, and

shutting off the low side MOSFET. This “Three-State” mode will hold both upper and low side MOSFETs off during the time that the Low Side MOSFET would normally be on.

This “Diode Emulation” is initiated when the current, as sensed through the low side MOSFET, is negative. This event triggers the “Three-State” mode until the next PWM cycle.

This Discontinuous operation improves efficiency by preventing the reverse conduction of current through the low side MOSFET. This eliminates conduction loss and output discharge. Discontinuous operation is enabled in Deep and Deeper Sleep modes and is based solely on current feedback.

Due to this ISL6218’s ability to sense zero current and prevent discharging through the low side MOSFETs during light loads, the ISL6218 meets the requirements for $\overline{PSI}$ without requiring any external signals.

STV, DSV and DRSV

START-UP “BOOT” VOLTAGE - STV

The Start-up, or “Boot,” voltage is programmed by an external resistor divider network from the OCSET pin (refer to Figure 8). Internally, a 1.75V reference voltage is output on the OCSET pin. The start-up voltage is set through a voltage divider from the 1.75V reference at the OCSET pin. The voltage on the STV pin will be the controller regulating voltage during the start-up sequence.

Once the PGOOD pin of the ISL6218 controller is externally enabled high by the Vccp and Vcc_mch controllers, the ISL6218 will then ramp, after a 10µs delay, to the voltage commanded by the VID setting minus “Droop”.

DEEP SLEEP VOLTAGE- DSV

The Deep Sleep voltage is programmed by an external voltage divider network from the DACOUT pin (Refer to Figure 8). The DACOUT pin is the output of the VID digital-to-analog converter. By having the Deep Sleep voltage setup from a resistor divider from DAC, the Deep Sleep voltage will be a constant percentage of the VID. Through the voltage divider network, Deep Sleep voltage is set to 98.8% of the programmed VID voltage, as per the IMVP-IV™ specification.

The IC enters the Deep Sleep mode when the $\overline{DSEN}$ is low and the DRSEN pin is low as shown in Figure 6 and Figure 5. Once in Deep Sleep Mode, the controller will regulate to the voltage seen on the DSV pin minus “Droop”.

DEEPER SLEEP VOLTAGE - DRSV

The Deeper Sleep voltage, DRSV, is programmed by an external voltage divider network from the 1.75V reference on the OCSET pin (Refer to Figure 8). In Deeper Sleep mode the ISL6218 controller will regulate the output voltage to the voltage present on the DRSV pin minus “Droop”.

The IC enters Deeper Sleep mode when DRSEN is high and $\overline{DSEN}$ is low, as shown in Figure 5.

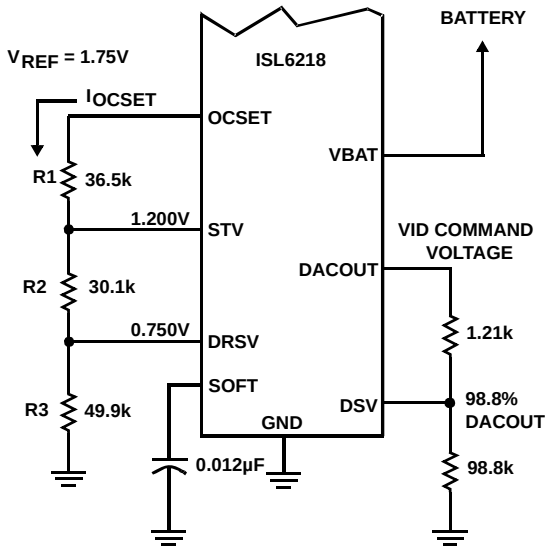


FIGURE 8. CONFIGURATIONS FOR BATTERY INPUT, OVERCURRENT SETTING AND START, DEEP SLEEP AND DEEPER SLEEP VOLTAGE

OVERCURRENT SETTING - OCSET

The ISL6218 overcurrent protection essentially compares a user-selectable overcurrent threshold to the scaled and sampled output current. An overcurrent condition is defined when the sampled current is equal to or greater than the threshold current. A step by step process to the user-desired overcurrent set point is detailed next.

Step 1: Setting the Overcurrent Threshold

The overcurrent threshold is represented by the DC current flowing out of the OCSET pin (See Figure 8). Since the OCSET pin is held at a constant 1.75V, the user need only populate a resistor from this pin to ground to set the desired overcurrent threshold, I_{OCSET}. The user should pick a value of I_{OCSET} between 10µA and 15µA. Once this is done, use Ohm’s Law to determine the necessary resistor to place from OCSET to ground:

$$R_{OCSET} = \frac{1.75V}{I_{OCSET}} = R_1 + R_2 + R_3 \quad \text{(EQ. 2)}$$

For example, if the desired overcurrent threshold is 15µA, the total resistance from OCSET must equal 117kΩ.

Step 2: Selecting ISEN Resistance for Desired Overcurrent Level

After choosing the I_{OCSET} level, the user must then decide what level of total output current is desired for overcurrent. Typically, this number is between 150% and 200% of the maximum operating current of the application. For example, if the max operating current is 27A, and the user chooses 150% overcurrent, the ISL6218 will shut down if the output current exceeds 27A*1.5 or 40A. According to the “Block Diagram” on page 7, Equation 3 should be used to determine R_{ISEN} once the overcurrent level, I_{OC}, is chosen.

$$R_{ISEN} = \frac{I_{OC} \cdot \frac{r_{(DSON)}}{M} \cdot 0.2175}{I_{OCSET} - 2\mu A} - 130 \quad \text{(EQ. 3)}$$

In Equation 3, M represents the number of Low-Side MOSFETs. Using the examples above (I_{OC} = 40A, I_{OCSET} = 15µA) and substituting the values M = 2, $r_{DS(ON)}$ = 4.5mΩ, R_{ISEN} is calculated to be 1370Ω.

Step 3: Thermal Compensation for $r_{DS(ON)}$ (if desired)

If PTCs are used for thermal compensation, then R_{ISEN} is found using the room temperature value of $r_{DS(ON)}$. If standard resistors are used for RISEN, then the "HOT" value of $r_{DS(ON)}$ should be used for this calculation.

MOSFET $r_{DS(ON)}$ sensing provides advantages in cost, efficiency, and board area. However, if more precise current feedback is desired, a discrete Precision Current Sense Resistor R_{POWER} may be inserted between the SOURCE of each channel's lower MOSFET and ground. The small R_{ISEN} resistor, as previously described, is then replaced with a standard 1% resistor and connected from the ISEN pin of the ISL6218 controller to the SOURCE of the lower MOSFET.

BATTERY FEED-FORWARD COMPENSATION - VBAT

As shown in Figure 8, the ISL6218 incorporates Battery Voltage Feed-Forward Compensation. This compensation provides a constant Pulse Width Modulator Gain independent of battery voltage. An understanding of this gain is required for proper loop compensation. The Battery Voltage is connected directly to the ISL6218 by the VBAT pin, and the gain of the system ramp modulator is a constant 6.0.

FAULT PROTECTION

The ISL6218 protects the CPU from damaging stress levels. The overcurrent trip point is integral in preventing output shorts of varying degrees from causing current spikes that would damage a CPU. The output overvoltage and undervoltage detection features insure a safe window of operation for the CPU.

OUTPUT VOLTAGE MONITORING

VSEN is connected to the local CORE Output Voltage and is used for PGOOD, undervoltage and overvoltage sensing only. (Refer to the "Block Diagram" on page 7).

The VSEN voltage is compared with two voltage levels that indicate an overvoltage or undervoltage condition of the output. Violating either of these conditions results in the PGOOD pin toggling low to indicate a problem with the output voltage.

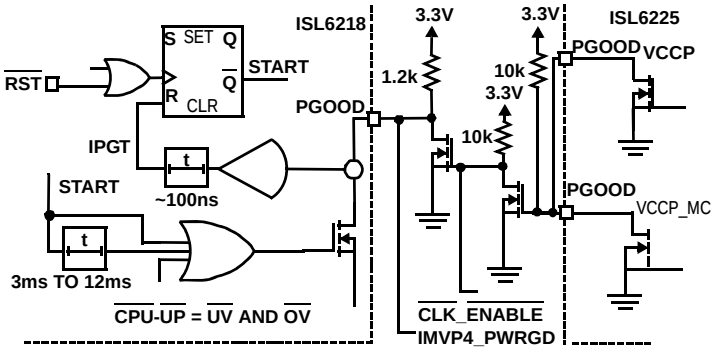


FIGURE 9. INTERNAL PGOOD CIRCUITRY FOR THE ISL6218 CORE VOLTAGE REGULATOR

PGOOD

As previously described, the ISL6218 PGOOD pin operates as both an input and an output. During start-up, the PGOOD pin operates as an input. Refer to Figure 9.

As per the IMVP-IV™ specification, once the ISL6218 CORE regulator regulates to the "Boot" voltage, it waits for the PGOOD logic HIGH signals from the Vccp and Vcc_mch regulators. The Intersil ISL6225 is a perfect choice for these two supplies as it is a dual regulator and has independent PGOOD functions for each supply. Once these two supplies are within regulation, $PGOOD_{Vccp}$ and $PGOOD_{Vcc\_mch}$ will be high impedance, and will allow the PGOOD of the ISL6218 to sink approximately 2.6mA to ground through the internal MOSFET, shown in Figure 9. The ISL6218 detects this current and starts an internal PGOOD timer.

The current sourced into the PGOOD pin is critical for proper start-up operation. The pullup resistor, $R_{pull\text{-}up}$ is sized to give a minimum of 2.6mA of current sourced into the PGOOD pin from 3.3V supply.

As given in the "Electrical Specifications" table on page 4, the PGOOD MOSFET $r_{DS(ON)}$ is given as 82Ω maximum. If a 3.3V source is used as the Pull-up, then the Pull-up resistor is given Equation 4:

$$Pullup = \frac{V_{SOURCE}}{2.6mA} - r_{DSON}(max) = \frac{3.3 - 0.05(3.3)}{2.6mA} - 82 = 1.2k\Omega \quad \text{(EQ. 4)}$$

where V_{SOURCE} is the supply minus 5% for tolerance. This will insure that the required PGOOD current will be sourced into the PGOOD pin for worst case conditions of low supply and largest MOSFET $r_{DS(ON)}$.

Once the proper level of PGOOD current is detected, the ISL6218 then captures the VID and regulates to this value. The PGOOD timer is a function of the internal clock and switching frequency. The internal PGOOD delay can be calculated in Equation 5:

$$\text{PGOOD Timer Delay} = 3072 / f_{SW} \quad \text{(EQ. 5)}$$

The ISL6218 controller regulates the CORE output voltage to the VID command and once the timer has expired, the PGOOD output is allowed to go high.

Note, the PGOOD functions of the V_{CC_CORE}, Vccp and Vcc_mch regulators are wire OR'd together to create the system signal "IMVP4_PWRGD". If any of the supplies fall outside the regulation window, their respective PGOOD pins are pulled low, which forces IMVP4_PWRGD low. PGOOD of the ISL6218 is internally disabled during all VID and Mode transitions.

OVERVOLTAGE

The VSEN voltage is compared with an internal overvoltage protection (OVP) reference set to 112% of the VID voltage. If the VSEN voltage exceeds the OVP reference, a comparator simultaneously sets the OV latch and triggers the PWM output low. The drivers turn on the lower MOSFETs, shunting the converter output to ground. Once the output voltage falls below 102% of the set point, the high side and low side PWM outputs are held in "Three-State".

This prevents dumping of the output capacitors back through the output inductors and lower MOSFETs, which would cause a negative voltage on the CORE output.

This architecture eliminates the need of a high current, Schottky diode on the output. If the overvoltage conditions persist, the PWM outputs are cycled between output low and output "off", similar to a hysteretic regulator. The OV latch is reset by cycling the VDD supply voltage to initiate a POR. Depending on the mode of operation, the overvoltage setpoint is 112% of the VID, Deep or Deeper Sleep setpoint.

UNDERVOLTAGE

The VSEN pin is also compared to an Undervoltage (UV) reference, which is set to 84% of the VID, Deep or Deeper Sleep setpoint, depending on the mode of operation. If the VSEN voltage is below the UV reference for more than 32 consecutive phase clock cycles, the power good monitor triggers the PGOOD pin to go low and latches the chip off until power is reset to the chip or the EN pin is toggled.

OVERCURRENT

The R_{ISEN} resistor scales the voltage sampled across the lower MOSFET and provides current feedback I_{SEN}, which is proportional to the output current (refer to Figure 10). After current sensing function, I_{SEN} is obtained (refer to the "Block Diagram" on page 7 and Figure 10). I_{SEN} is compared with an internally generated overcurrent trip threshold that is propotional to the current sourced from the OCSET pin, I_{OCSET}. The overcurrent trip current source is programmable and described in "Overcurrent Setting - OCSET" on page 12.

If I_{SEN} exceeds the I_{OCSET} level, an up/down counter is enabled. If I_{SEN}' does not fall below I_{OCSET} within 32 phase cycle counts, the PGOOD pin transitions low and latches the chip off. If normal operation resumes within the 32 phase cycle count window, the controller will continue to operate normally.

NOTE: Due to "DROOP", there is inherent Current limit since load current cannot exceed the amount that would command an output voltage lower than 84% of the VID voltage. This would result in an undervoltage shutdown and would also cause the PGOOD pin to transition low and latch the chip off.

CONTROL LOOPS

Figure 10 shows a simplified diagram of the voltage regulation and current control loops for a Single-Phase converter. Both voltage and current feedback are used to precisely regulate voltage and tightly control output current I_{L1}. The voltage loop is comprised of the Error Amplifier, Comparators, Internal Gate Drivers and MOSFETs. The Error Amplifier drives the modulator to force the FB pin to the IMVP-IV™ reference minus "Droop".

VOLTAGE LOOP

The output CORE voltage feedback is applied to the Error Amplifier through the compensation network. The signal seen on the FB pin will drive the Error Amplifier output either high or low, depending upon the CORE voltage. A CORE voltage level that is lower than the IMVP-IV™ reference, as output from the 6-bit DAC, causes the amplifier output to move towards a higher output voltage level. The amplifier output voltage is applied to the positive input of the comparator. Increasing Error Amplifier voltage results in increased Comparator output duty cycle. This increased duty cycle signal is passed through the PWM circuit to the internal gate drive circuitry. The output of the internal gate drive is directly connected to the gate of the MOSFETs. Increased duty cycle, or ON-time, for the high side MOSFET transistors, results in increased output voltage (VCORE) to compensate for the low output voltage sensed.

DROOP COMPENSATION

Microprocessors and other peripherals tend to change their load current demands from near no-load to full load, often during operation. These same devices require minimal output voltage deviation during a load step.

A high di/dt load step will cause an output voltage spike. The amplitude of the spike is dictated by the output capacitor ESR multiplied by the load step magnitude plus the output capacitor ESL times the load step di/dt. A positive load step produces a negative output voltage spike and vice versa. A large number of low-series-impedance capacitors are often used to prevent the output voltage deviation from exceeding the tolerance of some devices. One widely accepted solution to this problem is output voltage "Droop", or active voltage positioning.

As shown in the block diagram, the sensed current (I_{SEN}) is used to control the "Droop" current source, I_{DROOP}. The "Droop" current source is a controlled current source and is proportional to output current. This current source is

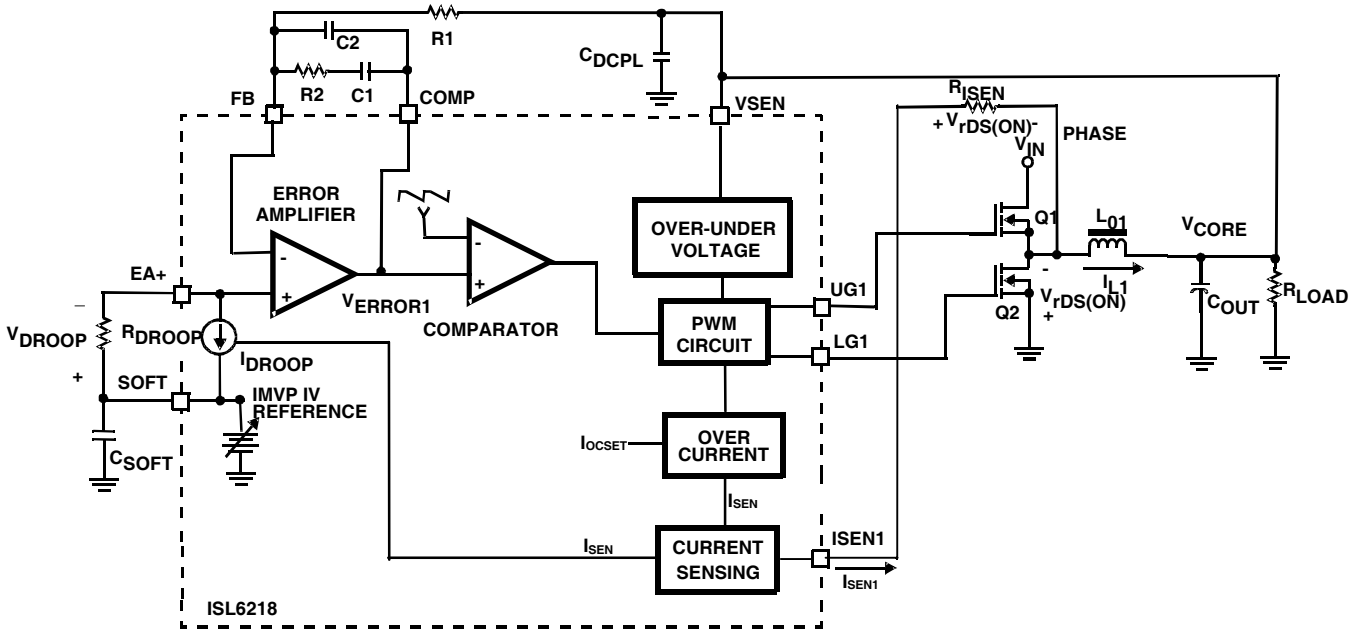


FIGURE 10. SIMPLIFIED BLOCK DIAGRAM OF THE ISL6218 VOLTAGE AND CURRENT CONTROL LOOPS FOR THE SINGLE CHANNEL REGULATOR.

approximately ½ of the I_{SEN}, as shown in the "Block Diagram" on page 7. The Droop current is sourced out of the SOFT pin through the Droop resistor and returns through the EA+ pin. This creates a "Droop" voltage V_{DROOP}, that subtracts from the IMVP-IV™ reference voltage on SOFT to generate the voltage setpoint for the CORE regulator.

Full load current for the Intel IMVP-IV™ Thin and Light specification is 25A. Knowing that the Droop Current, sourced out of the SOFT pin will be ½ of the I_{SEN}, a "Droop" resistor, R_{DROOP}, can be selected to provide the amount of voltage "Droop" required at full load. The selection of this resistor is explained "Selection of RDROOP" on page 15.

SELECTION OF R_{DROOP}

Figure 11 shows a static "Droop" load line for the 1.484V Active Mode. The ISL6218, as previously mentioned, allows the programming of the load line slope by the selection of the R_{DROOP} resistor.

As per the Intel IMVP-IV™ and IMVP-IV+™ specification, Droop = 0.003 (Ω). Therefore, 25A of full load current equates to a 0.075V Droop output voltage from the VID setpoint. R_{DROOP} can be selected based on R_{ISEN} which is calculated through Equation 3, $r_{(DS(ON))}$ and Droop, as per the "Block Diagram" on page 7 or Equation 6:

$$R_{DROOP} = 2.3 \cdot (Droop) \cdot \frac{R_{ISEN}}{\frac{r_{(DSON)}}{M}} (\Omega) \quad \text{(EQ. 6)}$$

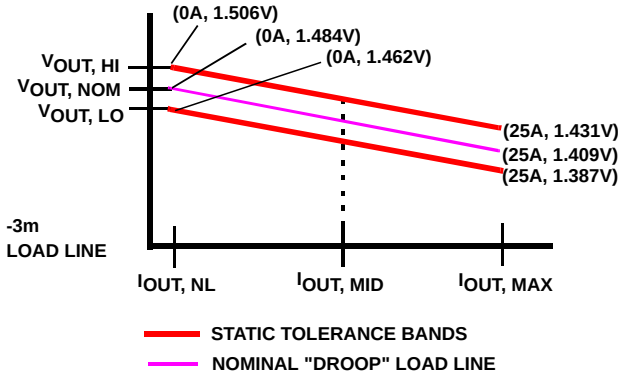


FIGURE 11. IMVP-IV™ ACTIVE MODE STATIC LOAD LINE

Component Selection Guidelines

Output Capacitor Selection

Output capacitors are required to filter the output inductor current ripple, and supply the transient load current. The filtering requirements are a function of the channel switching frequency and the output ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current.

The microprocessor used for IMVP-IV™ will produce transient load rates as high as 30A/ns. High frequency ceramic capacitors are used to supply the initial transient current, and slow the rate-of-change seen by the bulk capacitors. Bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements, rather than actual capacitance requirements. To meet the stringent requirements of IMVP-IV™, (15) 2.2µF, 0612 "Flip Chip" high frequency, ceramic capacitors are placed very close

to the Processor power pins; they are placed carefully so they do not to add inductance in the circuit board traces, which could cancel the usefulness of these low inductance components.

Specialized low-ESR capacitors intended for switching regulator applications are recommended for the bulk capacitors. The bulk capacitors ESR and ESL determine the output ripple voltage and the initial voltage drop following a high slew-rate transient edge. Recommended are at least (4) 4V, 220µF Sanyo Sp-Cap capacitors in parallel, or (5) 330µF SP-Cap style capacitors. These capacitors provide an equivalent ESR of less than 3mΩ. These components should be laid out very close to the load.

As the sense trace for VSEN may be long and routed close to switching nodes, a 1.0µF ceramic decoupling capacitor is located between VSEN and ground at the ISL6218 package.

Output Inductor Selection

The output inductor is selected to meet the voltage ripple requirements and minimize the converter response time to a load transient.

The inductor selected for the power channel determines the channel ripple current. Increasing the value of inductance reduces the total output ripple current and total output voltage ripple, but will slow the converter response time to a load transient.

One of the parameters limiting the converter's response time to a load transient is the time required to slew the inductor current from its initial current level to the transient current level. During this interval, the difference between the two levels must be supplied by the output capacitance. Minimizing the response time can minimize the output capacitance required.

The channel ripple current is approximated by Equation 7:

$$\Delta I_{CH} = \frac{V_{IN} - V_{OUT}}{F_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 7)}$$

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors must be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

Two important parameters to consider when selecting the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select a bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline.

MOSFET Selection and Considerations

For the Intel IMVP-IV™ application that requires up to 20A of current, it is suggested that Single-Phase channel operation, with a minimum of (4) MOSFETs per channel, be implemented. This configuration would be: (2) High Switching Frequency, Low Gate Charge MOSFET for the Upper; and (2) Low $r_{DS(ON)}$ MOSFETs for the Lowers.

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle of the converter. Refer to Equations 8 and 9. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFETs have significant switching losses, since the lower devices turn on and off into near zero voltage. The following equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated in the ISL6218 drivers and do not heat the MOSFETs; however, large gate-charge increases the switching time t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_{SW}}{2} \quad \text{(EQ. 8)}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 9)}$$

Typical Application - Single Phase Converter Using ISL6218 PWM Controller

Figure 12 shows the ISL6218, Synchronous Buck Converter circuit, which is used to provide the CORE voltage regulation for the Intel IMVP-IV™ application. The circuit uses a single power channel to deliver up to 20A steady state current, and has a 330kHz channel switching frequency. For thermal compensation, a PTC resistor is used as sense resistors. The Output capacitance is less than 3mΩ of ESR and is (4) 220µF, 4V Sp-Cap parts in parallel with (35) high frequency, 10µF ceramic capacitors.

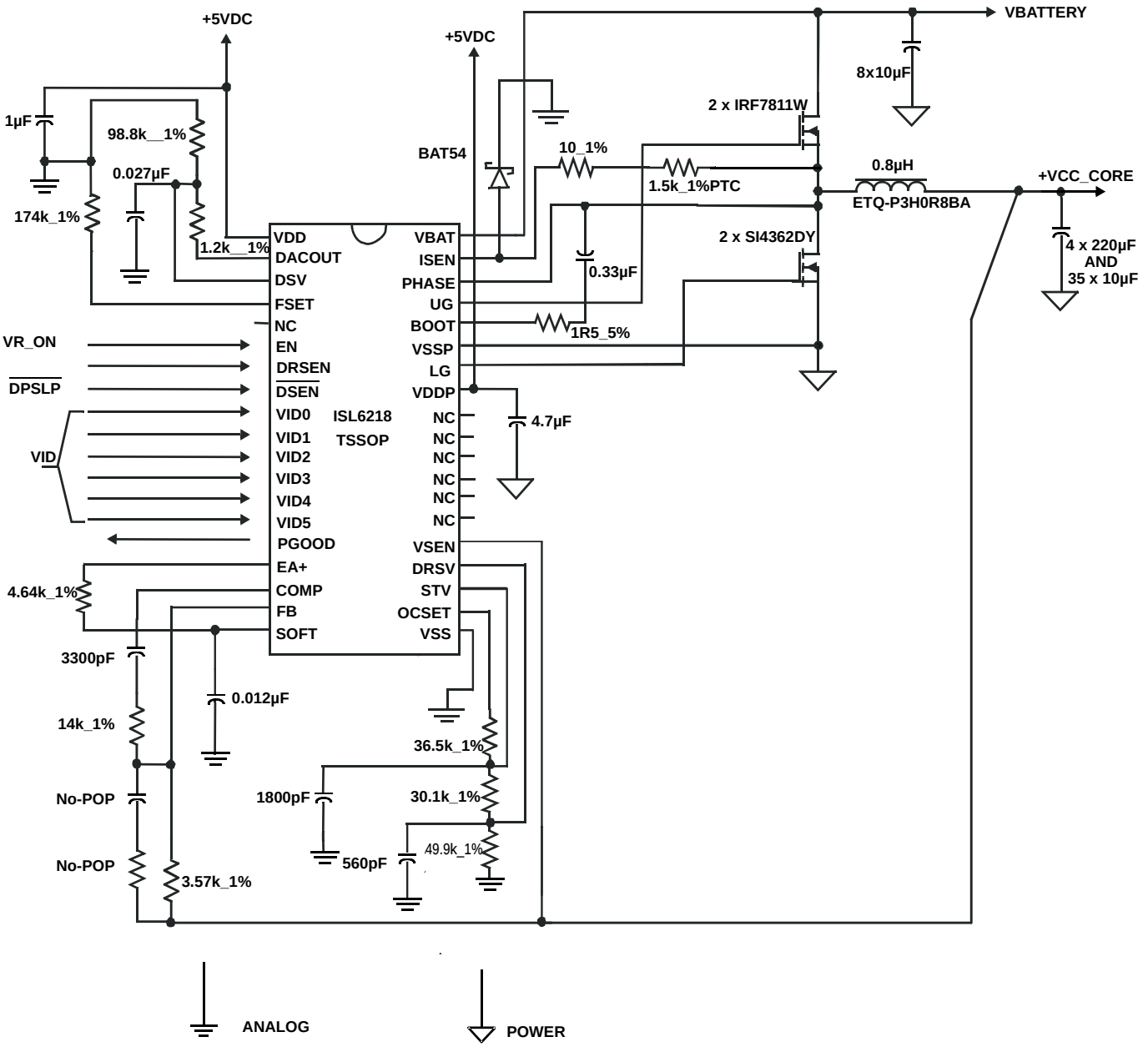
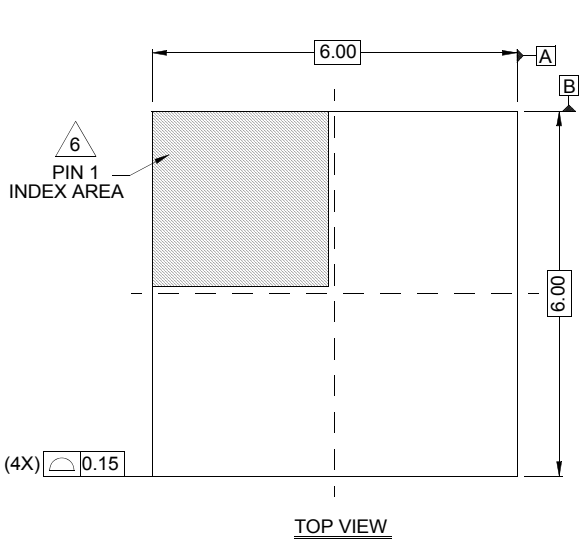


FIGURE 12. TYPICAL APPLICATION CIRCUIT FOR THE ISL6218, IMVP-IV™ CORE VOLTAGE REGULATOR

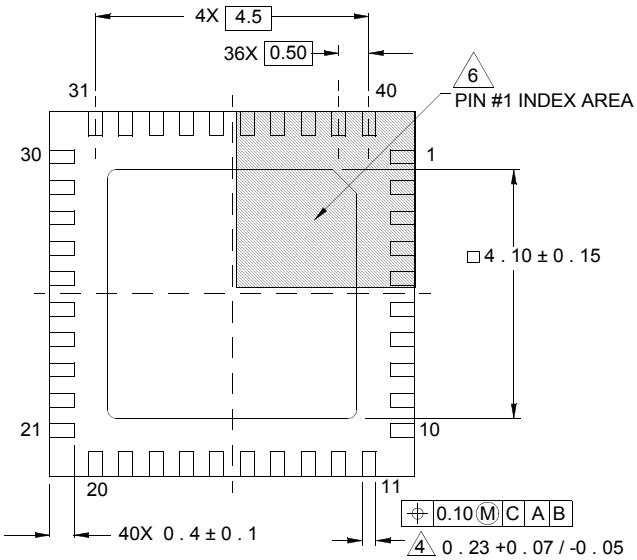
Package Outline Drawing

L40.6x6

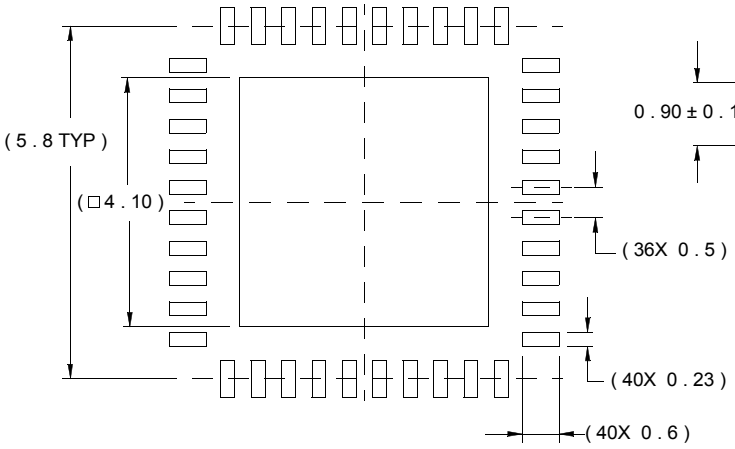
40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 10/06



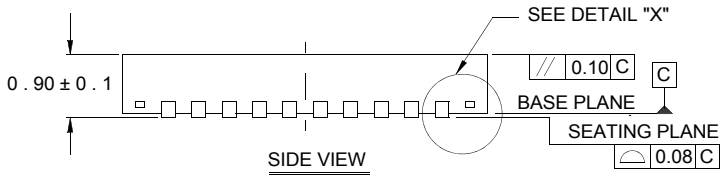
TOP VIEW



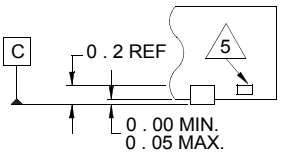
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

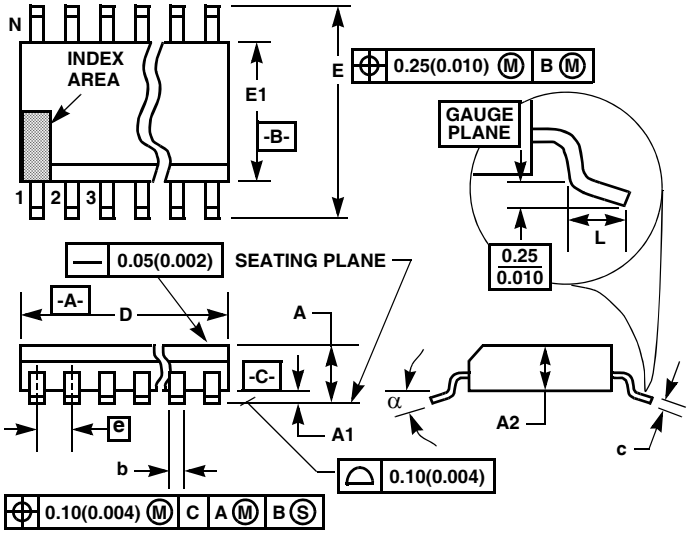


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-BD-1, Issue F.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M38.173

38 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-153-BD-1 ISSUE F)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0106	0.17	0.27	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.0197 BSC		0.500 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	38		38		7
α	0º	8º	0º	8º	-

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