DDR Termination Regulator

General Description

RT9026 is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count systems. The RT9026 possesses a high speed operating amplifier that provides fast load transient response and only requires 20μF of ceramic output capacitance. The RT9026 supports remote sensing functions and all features required to power the DDRI/II/III and low-power DDRIII/DDRIV VTT bus termination according to the JEDEC specification. In addition, the RT9026 includes integrated sleep-state controls placing VTT in High-Z in S3 (suspend to RAM) and soft-off for VTT and VTTREF in S5 (shutdown). The RT9026 is available in the thermal efficient package SOP-8 (Exposed Pad), MSOP-10 (Exposed Pad) and WDFN-10L 3x3.

Applications

- DDRI/II/III and Low-Power DDRIII/DDRIV Memory Termination
- SSTL-2, SSTL-18
- HSTL Termination

Ordering Information

RT9026 □□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)
FP : MSOP-10 (Exposed Pad)
QW : WDFN-10L 3x3 (W-Type)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

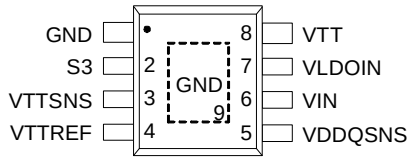
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

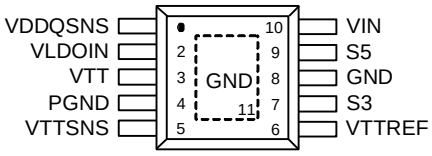
- **Support DDRI, DDRII, DDRIII, Low-Power DDRIII and DDRIV Requirement**
  - **Source/Sink 3A for DDRI and DDRII**
  - **Source/Sink 2A for DDRIII**
  - **Source/Sink 1.5A for Low-Power DDRIII**
  - **Source/Sink 1.2A for Low-Power DDRIV**
- **Input Voltage Range : 3.15V to 5.5V**
- **VLDOIN Voltage Range : 1.2V to 3.3V**
- **Requires Only 20mF Ceramic Output Capacitance**
- **Supports High-Z in S3 and Soft-Off in S5**
- **Integrated Divider Tracks 1/2 VDDQSNS for Both VTT and VTTREF**
- **Remote Sensing (VTTSNS)**
- **±20mV Accuracy for VTT and VTTREF**
- **10mA Buffered Reference (Sourcing/Sinking) (VTTREF)**
- **Built-In Soft-Start**
- **Over Current Protection**
- **Thermal Shutdown Protection**
- **SOP-8 (Exposed Pad), MSOP-10 (Exposed Pad) and 10-Lead WDFN Package**
- **RoHS Compliant and Halogen Free**

Pin Configurations

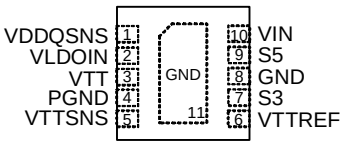
(TOP VIEW)



SOP-8 (Exposed Pad)



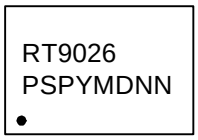
MSOP-10 (Exposed Pad)



WDFN-10L 3x3

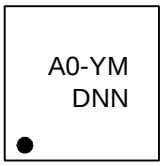
Marking Information

RT9026PSP



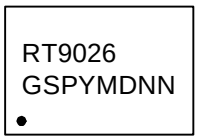
RT9026PSP : Product Code
YMDNN : Date Code

RT9026PFP



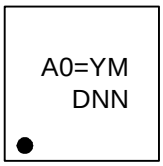
A0- : Product Code
YMDNN : Date Code

RT9026GSP



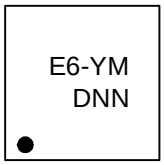
RT9026GSP : Product Code
YMDNN : Date Code

RT9026GFP



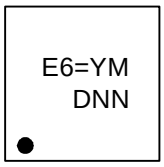
A0= : Product Code
YMDNN : Date Code

RT9026PQW



E6- : Product Code
YMDNN : Date Code

RT9026GQW



E6= : Product Code
YMDNN : Date Code

Typical Application Circuit

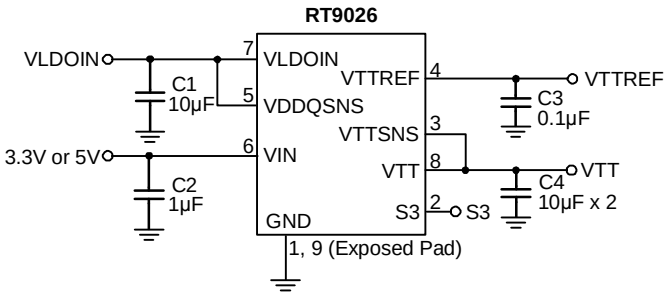


Figure 1. For SOP-8 (Exposed Pad) Package

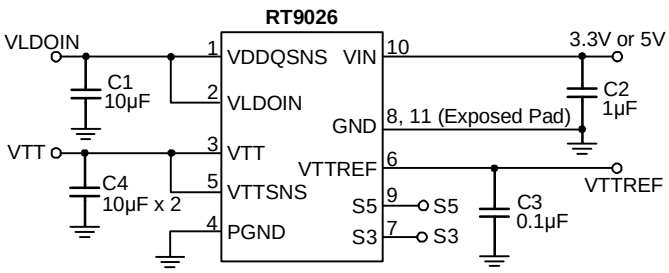


Figure 2. For MSOP-10 (Exposed Pad) / WDFN-10L 3x3 Package

Functional Pin Description

Pin No.		Pin Name	Pin Function
RT9026□SP	RT9026□FP RT9026□QW		
1, 9 (Exposed Pad)	8, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
2	7	S3	Active Low Suspend to RAM Mode Control Pin, VTT is turned off and left High-Z, VTTREF is active.
3	5	VTTSNS	VTT Voltage Sense Input Pin. Connect to plus terminal of the output capacitor.

To be Continued

Pin No.		Pin Name	Pin Function
RT9026□SP	RT9026□FP RT9026□QW		
4	6	VTTREF	Buffered output that is a reference output, equal to VDDQSNS/2.
5	1	VDDQSNS	VLDOIN Sense Input Pin.
6	10	VIN	Analog Input Pin (to control loop).
7	2	VLDOIN	Power supply of the VTT and VTTREF output stage (to power MOS).
8	3	VTT	Output voltage for connection to termination resistors, equal to VDDQSNS/2.
--	4	PGND	Power Ground of the VTT Output.
--	9	S5	Active low shutdown control pin, both VTT and VTTREF are turned off and discharged to ground.

Function Block Diagram

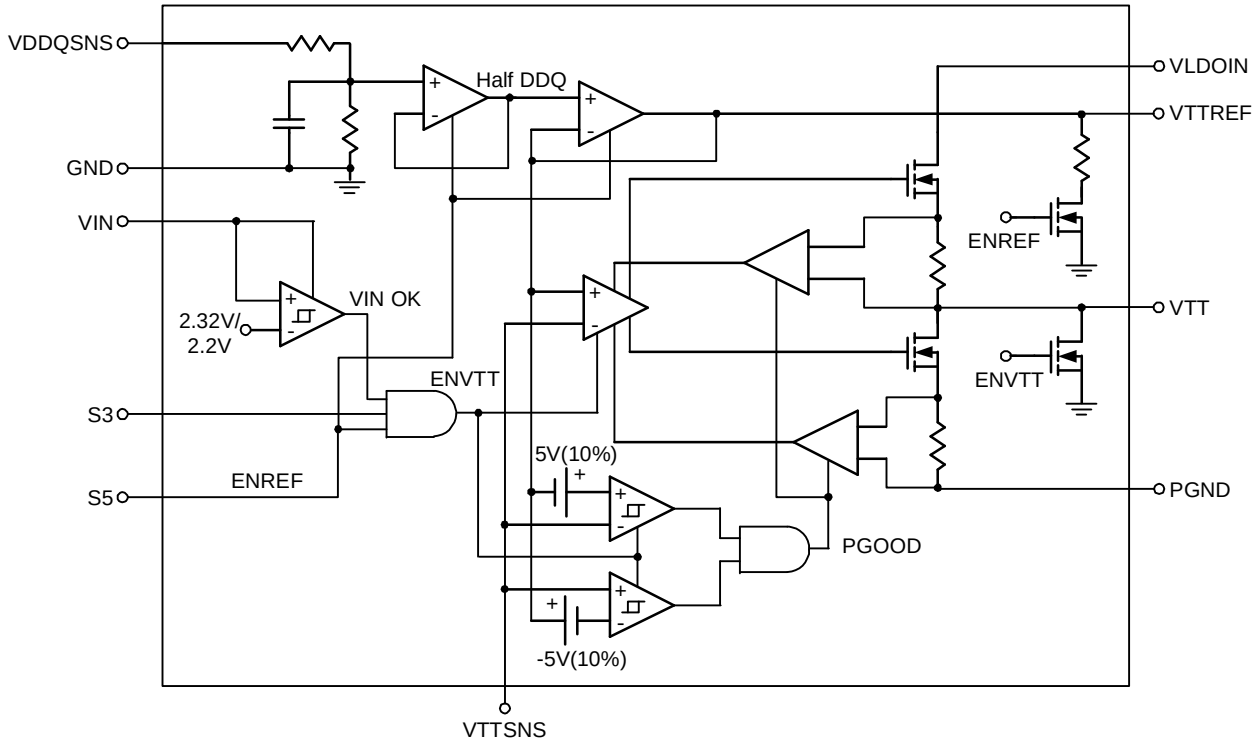


Table 1. S3 and S5 Control Table

State	S3	S5	VTT	VREF
Normal	High	High	1.25V/0.9V/0.75V /0.675V/0.6V	1.25V/0.9V/0.75V /0.675V/0.6V
Standby	Low	High	12mV/6mV (High-Z)	1.25V/0.9V/0.75V /0.675V/0.6V
Shutdown	Low	Low	0V (Discharge)	0V (Discharge)
Shutdown	High	Low	0V (Discharge)	0V (Discharge)

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- 6V
- Supply Input Voltage, VLDOIN, VDDQSNS ---------- 3.6V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-8 (Exposed Pad) ---------- 1.333W
  - MSOP-10 (Exposed Pad) ---------- 1.163W
  - WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 28°C/W
  - MSOP-10 (Exposed Pad), θ_{JA} ---------- 86°C/W
  - MSOP-10 (Exposed Pad), θ_{JC} ---------- 30°C/W
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 3.15V to 5.5V
- Supply Input Voltage, VLDOIN, VDDQSNS ---------- 1.2V to 3.3V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, VLDOIN = VDDQSNS = 2.5V, C1=10µF, C2=1µF, C3=0.1µF, C4=10µFx2, T_A = 25°C, S5 function only for RT9026PFP and RT9026PQW, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN (to control loop) Supply Current	I_{VIN}	V_{IN} = 5V, No Load, S5 = S3 = 5V	--	--	2	mA
VIN Standby Current	I_{VINSTB}	V_{IN} = 5V, No Load, S5 = 5V, S3 = 0V	--	--	300	µA
VIN Shutdown Current	$I_{VINSHDN}$	V_{IN} = 5V, No Load, S5 = S3 = 0V (Only for RT9026PFP and RT9026PQW)	--	--	1	µA
VLDOIN (to power MOS) Supply Current	I_{VLDOIN}	V_{IN} = 5V, No Load, S5 = S3 = 5V	--	--	2	mA
VLDOIN Standby Current	$I_{VLDOINSTB}$	V_{IN} = 5V, No Load, S5 = 5V, S3 = 0V	--	--	10	µA
VLDOIN Shutdown Current	$I_{VLDOINSHDN}$	V_{IN} = 5V, No Load, S5 = S3 = 0V	--	--	1	µA
VDDQSNS Input Current	$I_{VDDQSNS}$	V_{IN} = 5V, S5 = S3 = 5V	--	--	50	µA
VTTSNS Input Current	I_{VTTSNS}	V_{IN} = 5V, S5 = S3 = 5V	--	--	1	µA
VTT Output Voltage	VTT	VDDQSNS = VLDOIN = 2.5V	--	1.25	--	V
		VDDQSNS = VLDOIN = 1.8V	--	0.9	--	
		VDDQSNS = VLDOIN = 1.5V	--	0.75	--	

To be Continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
VTT Output Voltage		VTT	VDDQSNS = VLDOIN = 1.35V	--	0.675	--	V
			VDDQSNS = VLDOIN = 1.2V	--	0.6	--	
VTTREF, VTT Output Tolerance		V_{VTTTOL}	VDDQSNS = VLDOIN = 2.5V/1.8V/1.5V/1.35V/1.2V, $\lvert I_{VTT} \rvert$ = 0A	–20	--	20	mV
			VDDQSNS = VLDOIN = 1.2V, $\lvert I_{VTT} \rvert$ = 1.2A	–40	--	40	
			VDDQSNS = VLDOIN = 2.5V/1.8V/1.5V/1.35V, $\lvert I_{VTT} \rvert$ = 1.5A	–40	--	40	
			VDDQSNS = VLDOIN = 2.5V/1.8V, $\lvert I_{VTT} \rvert$ = 3A	–40	--	40	
VTT Source Current Limit		$I_{VTTOCLsr}$	VTT = 0V	3	4	--	A
VTT Sink Current Limit		$I_{VTTOCLsk}$	VTT = VDDQSNS	3	4	--	A
VTT Discharge Current		I_{DSCHRG}	VDDQSNS = 0V, VTT = 1.25V, S5 = S3 = 0V	10	17	--	mA
VTTREF Output Voltage		V_{VTTREF}	$V_{VTTREF} = \left(\frac{V_{VDDQSNS}}{2}\right)$	--	1.25/0.9/ 0.75/ 0.675/0.6	--	V
VDDQSNS/2, VTTREF Output Voltage Tolerance		$V_{VTTREFTOL}$	VLDOIN = VDDQSNS = 2.5V/1.8V/1.5V/1.35V/1.2V, I_{VTTREF} < 10mA	–20	--	20	mV
VTTREF Source Current Limit		$I_{VTTREFOCL}$	V_{VTTREF} = 0V	20	40	60	mA
UVLO Threshold Voltage		V_{UVLO}	Rising	--	--	2.7	V
			Hysteresis	--	0.2	--	
Input Voltage	Logic-High	V_{IH}	S5, S3 pin	1.6	--	--	V
	Logic-Low	V_{IL}	S5, S3 pin	--	--	0.4	
Logic Input Leakage Current		I_{ILK}	S5, S3 pin	--	--	1	μA
Thermal Shutdown Protection		T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four-layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the exposed pad for SOP-8 (Exposed Pad) , MSOP-10 (Exposed Pad) and WDFN-10L 3x3 package.

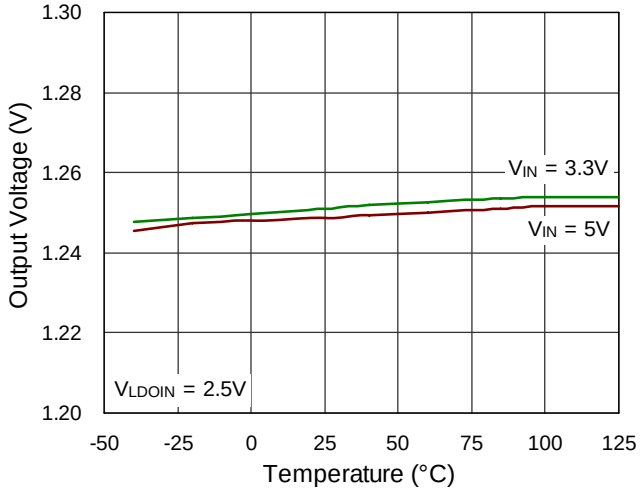
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

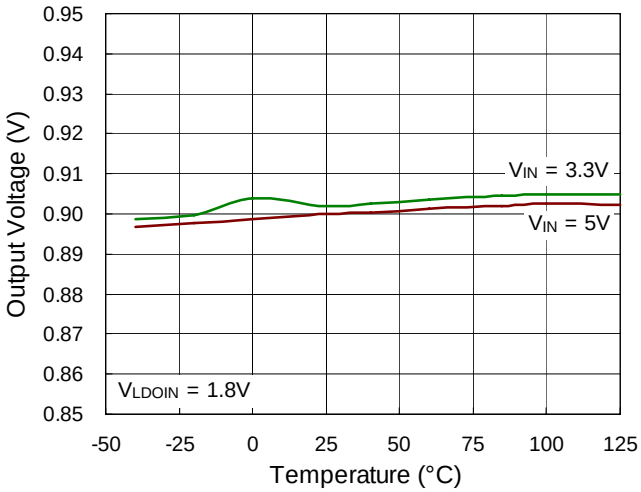
Typical Operating Characteristics

V_{DDQSNS} = V_{LDOIN}, C1 = 10µF, C2 = 1µF, C3 = 0.1µF, C4 = 10µF x 2 unless otherwise specified.

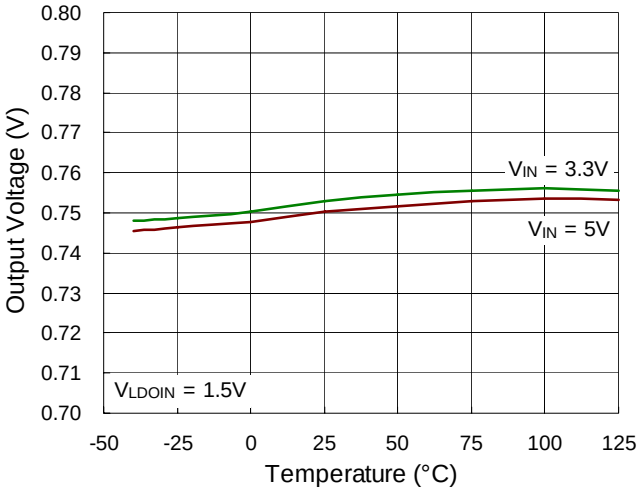
1.25V_{TT} Output Voltage vs. Temperature



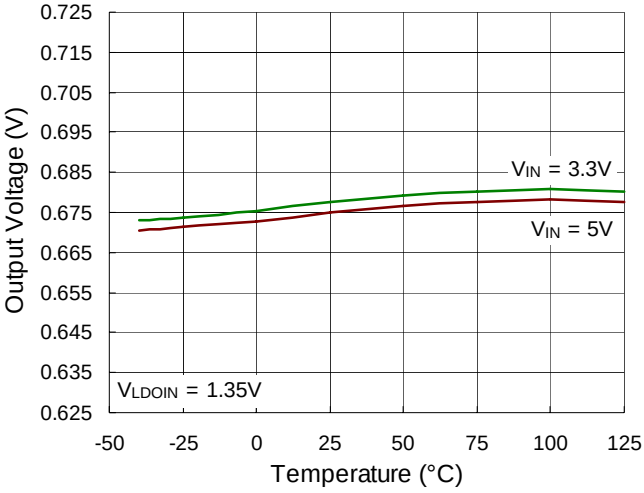
0.9V_{TT} Output Voltage vs. Temperature



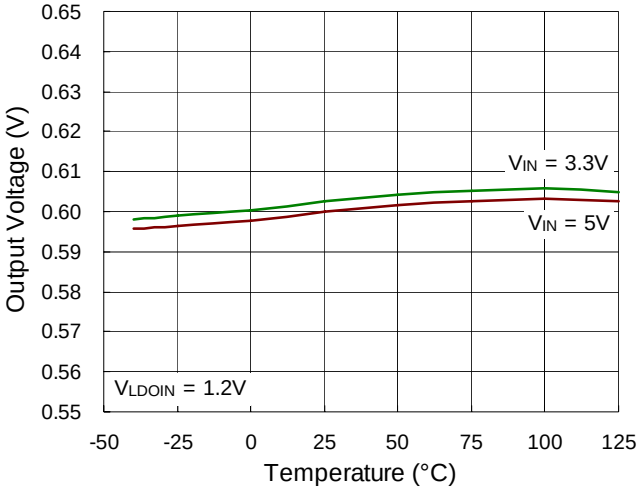
0.75V_{TT} Output Voltage vs. Temperature



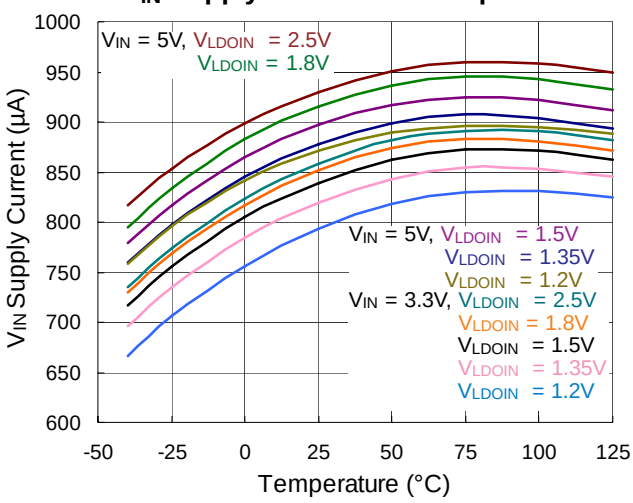
0.675V_{TT} Output Voltage vs. Temperature



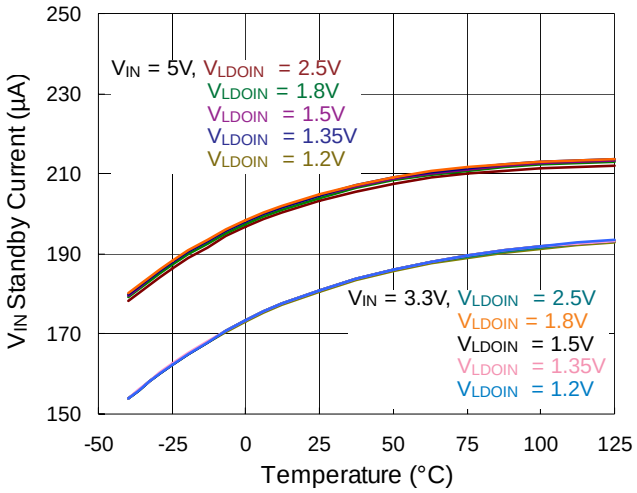
0.6V_{TT} Output Voltage vs. Temperature



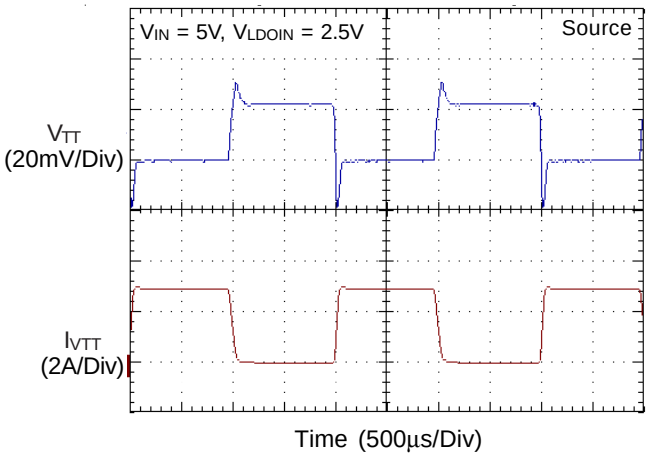
V_{IN} Supply Current vs. Temperature



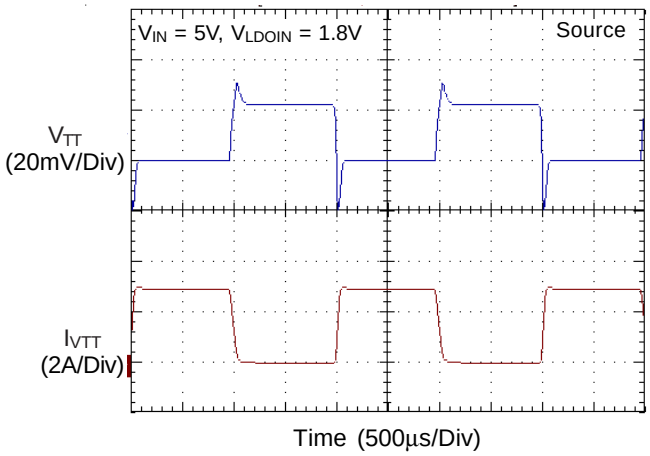
V_{IN} Standby Current vs. Temperature



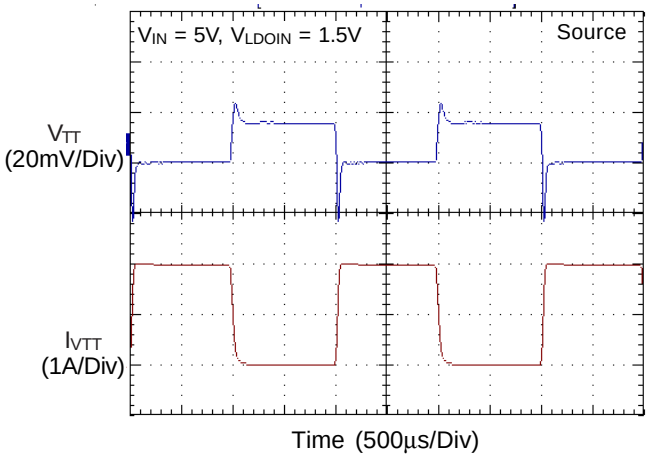
1.25V_{TT} @ 3A Transient Response



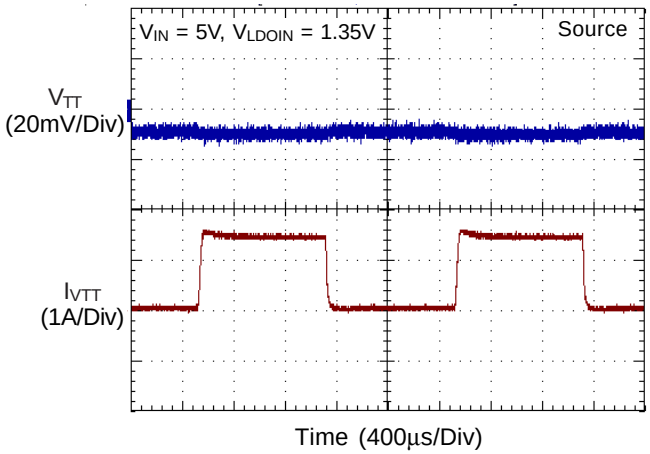
0.9V_{TT} @ 3A Transient Response



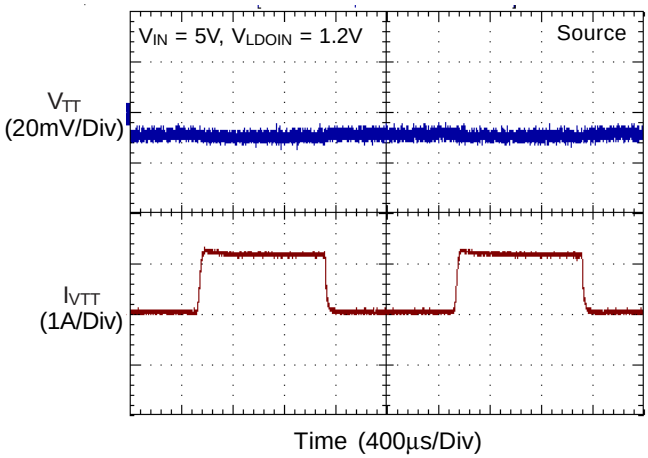
0.75V_{TT} @ 2A Transient Response



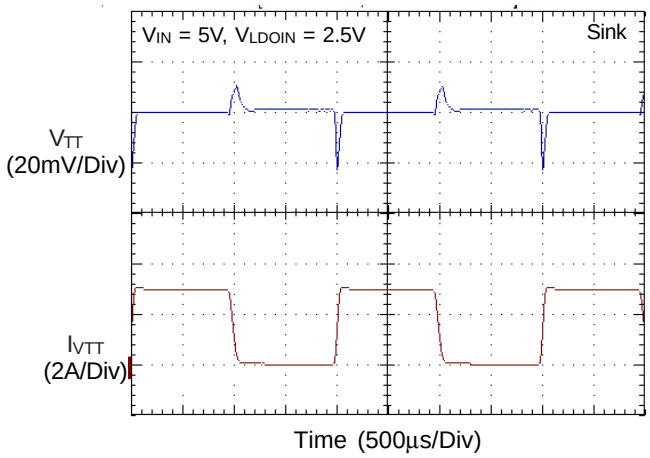
0.675V_{TT} @ 1.5A Transient Response



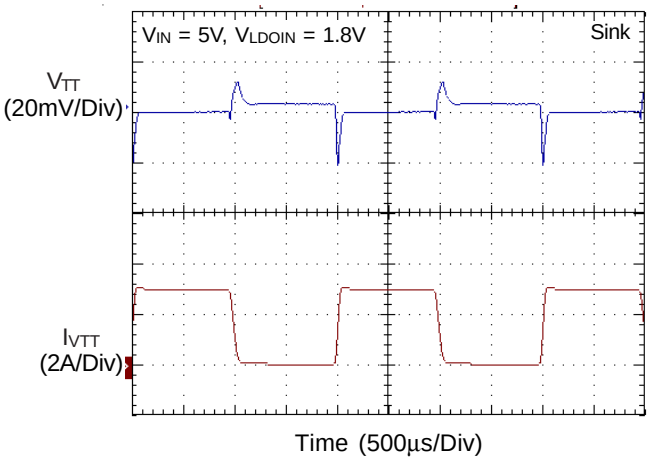
0.6V_{TT} @ 1.2A Transient Response



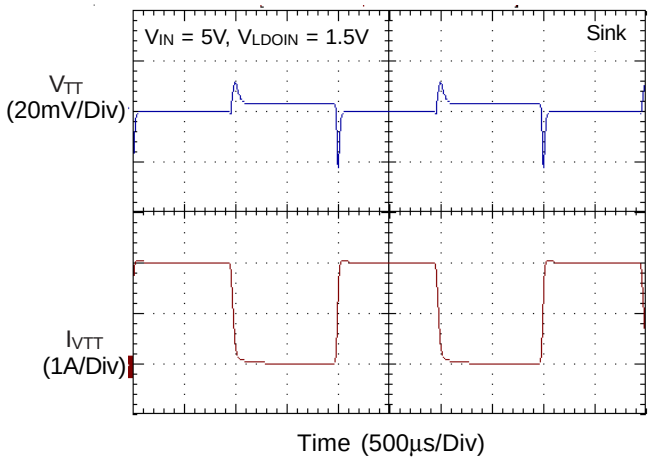
1.25V_{TT} @ 3A Transient Response



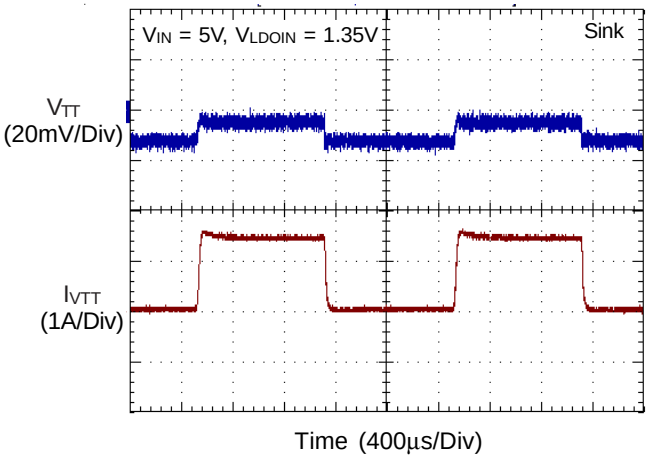
0.9V_{TT} @ 3A Transient Response



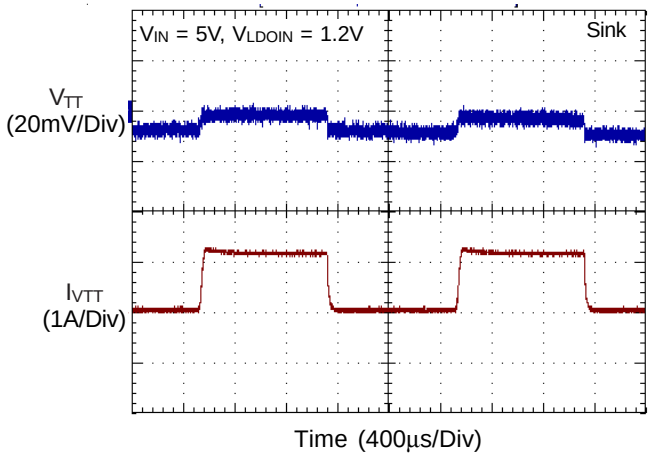
0.75V_{TT} @ 2A Transient Response



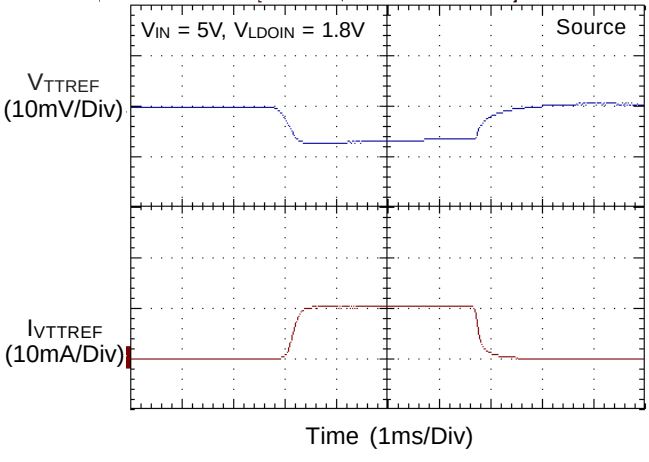
0.675V_{TT} @ 1.5A Transient Response



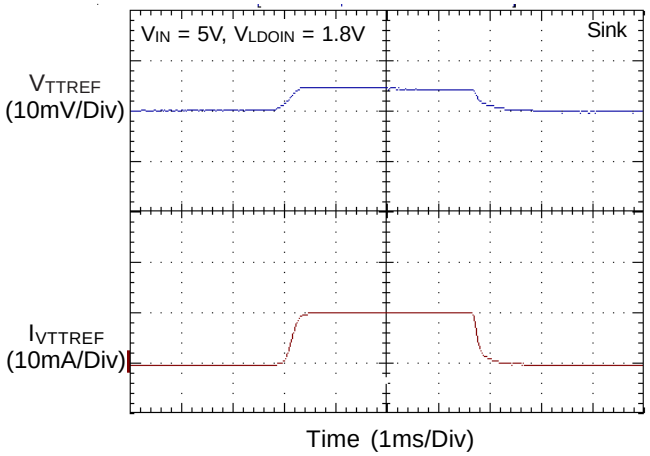
0.6V_{TTREF} @ 1.2A Transient Response



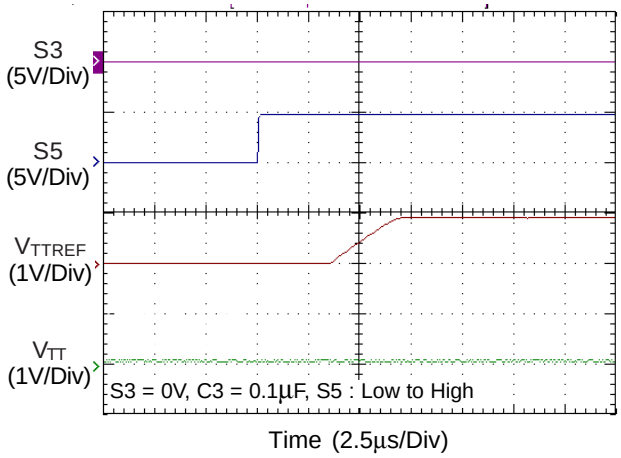
0.9V_{TTREF} @ 10mA Transient Response



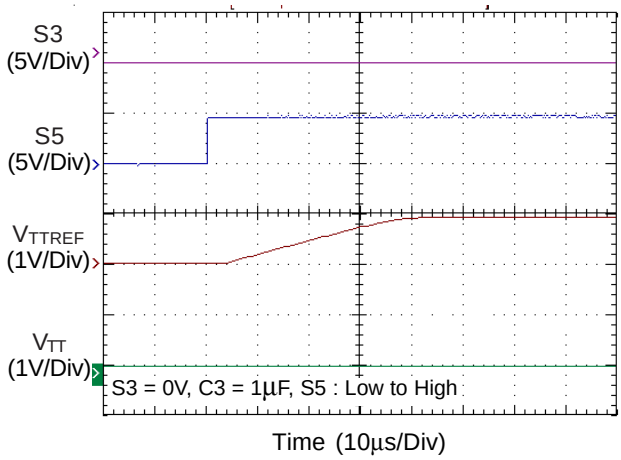
0.9V$_{TTREF}$ @ 10mA Transient Response



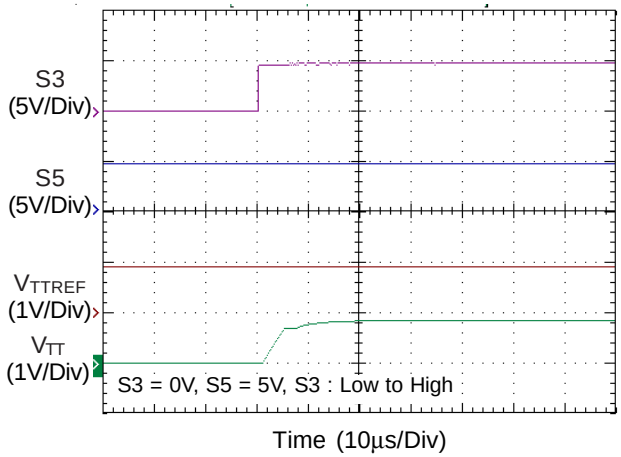
Start Up



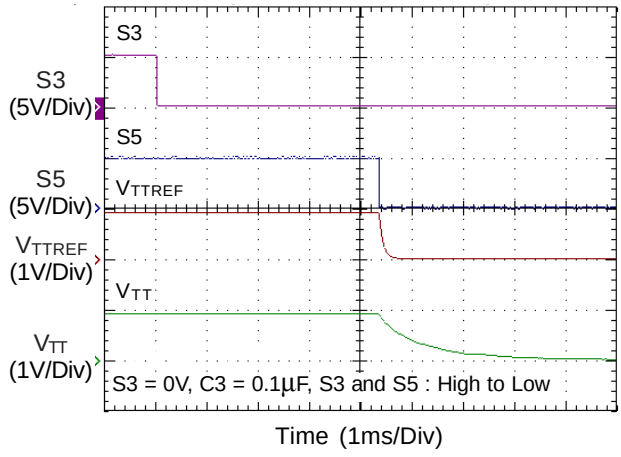
Start Up



Start Up



Power Off



Application Information

RT9026 is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost and low-external component count system such as notebook PC applications. The RT9026 possesses a high speed operating amplifier that provides fast load transient response and only requires a 10µF ceramic input capacitor and two 10µF ceramic output capacitor.

VTTREF Regulator

VTTREF is a reference output voltage with source/sink current capability up to 10mA. To ensure stable operation 0.1µF ceramic capacitor between VTTREF and GND is recommended.

S3, S5 Logic Control

The S3 and S5 terminals should be connected to SLP_S3 and SLP_S5 signals respectively. Both VTTREF and VTT are turned on at normal state (S3 = High, S5 = High). In standby state (S3 = Low, S5 = High) VTTREF is kept alive while VTT is turned off and left high impedance. Both VTT and VTTREF outputs are turned off and discharged to ground through internal MOSFETs during shutdown state (S5 = low).

Table 2. S3 and S5 Control

STATE	S3	S5	VTTREF	VTT
Normal	H	H	ON	ON
Standby	L	H	ON	OFF(high-Z)
Shutdown	L	L	OFF (discharge)	OFF (discharge)

Capacitor Selection

Good bypassing is recommended from VLDOIN to GND to help improve AC performance. A 10µF or greater input capacitor located as close as possible to the IC is recommended. The input capacitor must be located at a distance of less than 0.5 inches from the VLDOIN pin of the IC.

Adding a ceramic capacitor 1µF close to the VIN pin and it should be kept away from any parasitic impedance from the supply power.

For stable operation, the total capacitance of the cerarnic capcitor at the VTT output terminal must not be larger than 30µF. The RT9026 is designed specifically to work with low ESR ceramic output capacitor in space saving and performance consideration. Larger output capacitance can reduce the noise and improve load transient response, stability and PSRR. The output capacitor should be located near the VTT output terminal pin as close as possible.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT9026, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. The thermal resistance θ_{JA} for WDFN-10L 3x3 is 70°C/W, for SOP-8 (Exposed Pad) is 75°C/W and for MSOP-10 (Exposed Pad) is 86°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 packages

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) packages

$P_{D(MAX)}$ = (125°C – 25°C) / (86°C/W) = 1.163W for MSOP-10 (Exposed Pad) packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9026 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

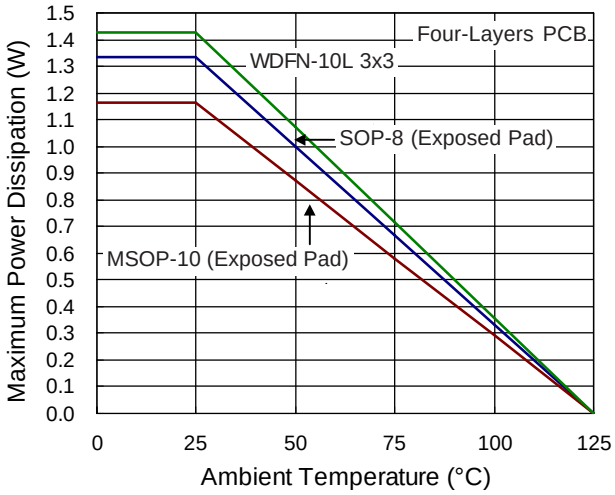
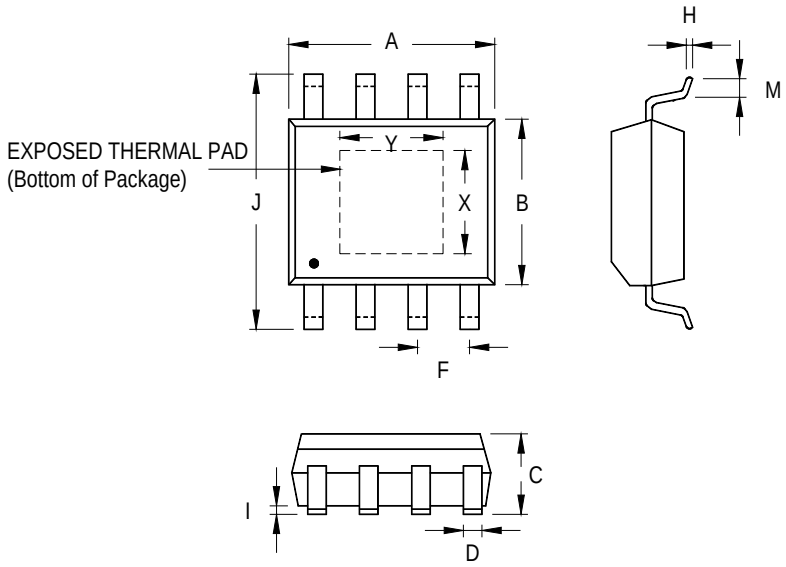


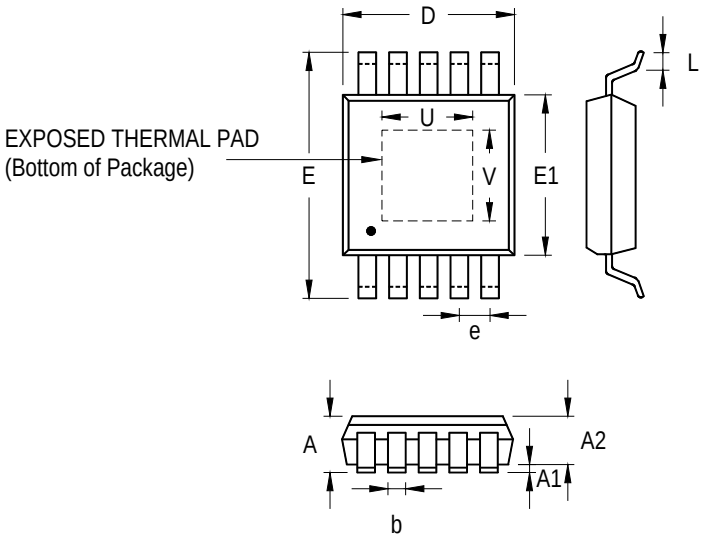
Figure 3. Derating Curves for the RT9026 Packages

Outline Dimension



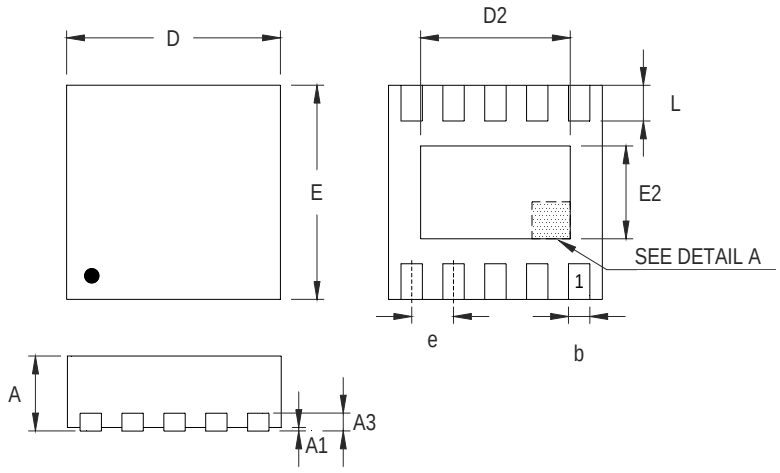
Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

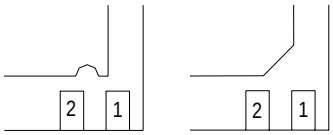
8-Lead SOP (Exposed Pad) Plastic Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.810	1.100	0.032	0.043
A1	0.000	0.100	0.000	0.004
A2	0.750	0.950	0.030	0.037
b	0.170	0.270	0.007	0.011
D	2.900	3.100	0.114	0.122
e	0.500		0.020	
E	4.800	5.000	0.189	0.197
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
U	1.300	1.700	0.051	0.067
V	1.500	1.900	0.059	0.075

10-Lead MSOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)

5F, No. 95, Minchiuan Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)86672399 Fax: (8862)86672377

Email: marketing@richtek.com