

# SCAN182245A

## Non-Inverting Transceiver with 25Ω Series Resistor Outputs

### General Description

The SCAN182245A is a high performance BiCMOS bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

### Features

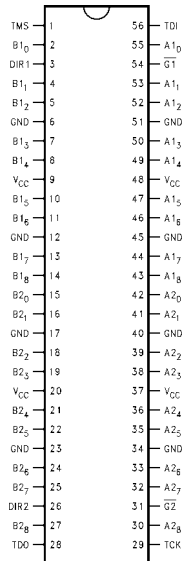
- High performance BiCMOS technology
- 25Ω series resistors in outputs eliminate the need for external terminating resistors
- Dual output enable control signals
- 3-STATE outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- IEEE 1149.1 (JTAG) Compliant
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power Up 3-STATE for hot insert
- Member of Fairchild's SCAN Products

### Ordering Code:

Order Number	Package Number	Package Description
SCAN182245ASSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
SCAN182245AMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Names	Description
A1 <sub>(0-8)</sub>	Side A1 Inputs or 3-STATE Outputs
B1 <sub>(0-8)</sub>	Side B1 Inputs or 3-STATE Outputs
A2 <sub>(0-8)</sub>	Side A2 Inputs or 3-STATE Outputs
B2 <sub>(0-8)</sub>	Side B2 Inputs or 3-STATE Outputs
G1, G2	Output Enable Pins (Active LOW)
DIR1, DIR2	Direction of Data Flow Pins

SCAN182245A Non-Inverting Transceiver with 25Ω Series Resistor Outputs

### Truth Tables

Inputs		A1(0-8)	B1(0-8)
G1 (Note 1)	DIR1		
L	L	H ← H	
L	L	L ← L	
L	H	H → H	
L	H	L → L	
H	X	Z	Z

Inputs		A2(0-8)	B2(0-8)
G2 (Note 1)	DIR2		
L	L	H ← H	
L	L	L ← L	
L	H	H → H	
L	H	L → L	
H	X	Z	Z

H = HIGH Voltage Level  
L = LOW Voltage Level

X = Immaterial  
Z = High Impedance

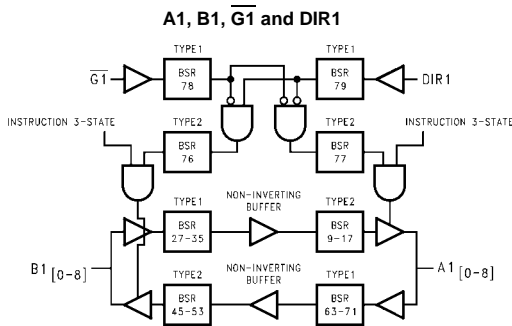
Note 1: Inactive-to-Active transition must occur to enable outputs upon power-up.

### Functional Description

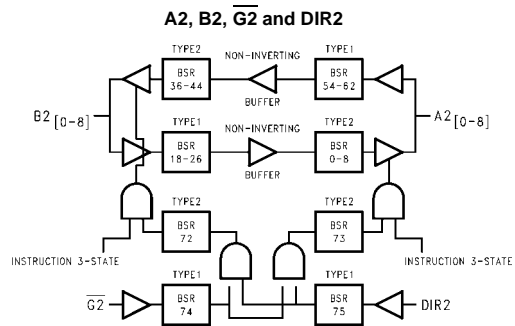
The SCAN182245A consists of two sets of nine non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B Ports to A Ports,

when HIGH enables data from A Ports to B Ports. The Output Enable pins (G1 and G2) when HIGH disables both A and B Ports by placing them in a high impedance condition.

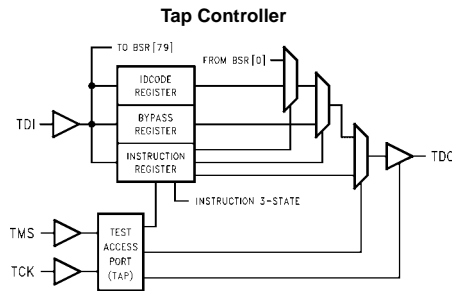
### Block Diagrams



Note: BSR stands for Boundary Scan Register.



Note: BSR stands for Boundary Scan Register.



## Description of BOUNDARY-SCAN Circuitry

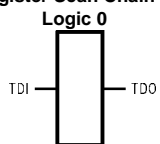
The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data.

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

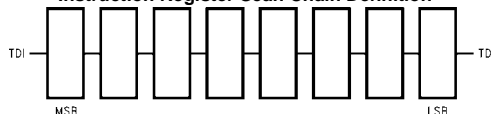
### Bypass Register Scan Chain Definition



**SCAN182245A Product IDCODE  
(32-Bit Code per IEEE 1149.1)**

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000000000	00000001111	1
<b>MSB</b>				<b>MSB</b>

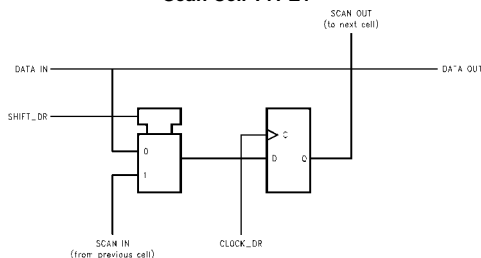
### Instruction Register Scan Chain Definition



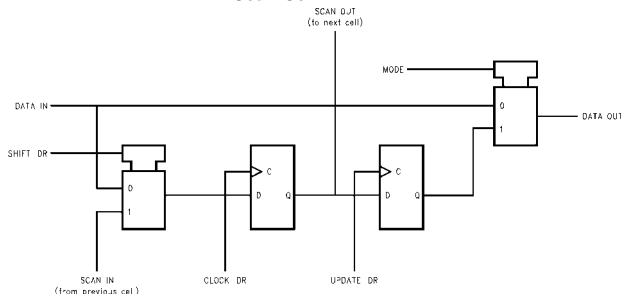
MSB → LSB

Instruction Code	Instruction
00000000	EXTTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

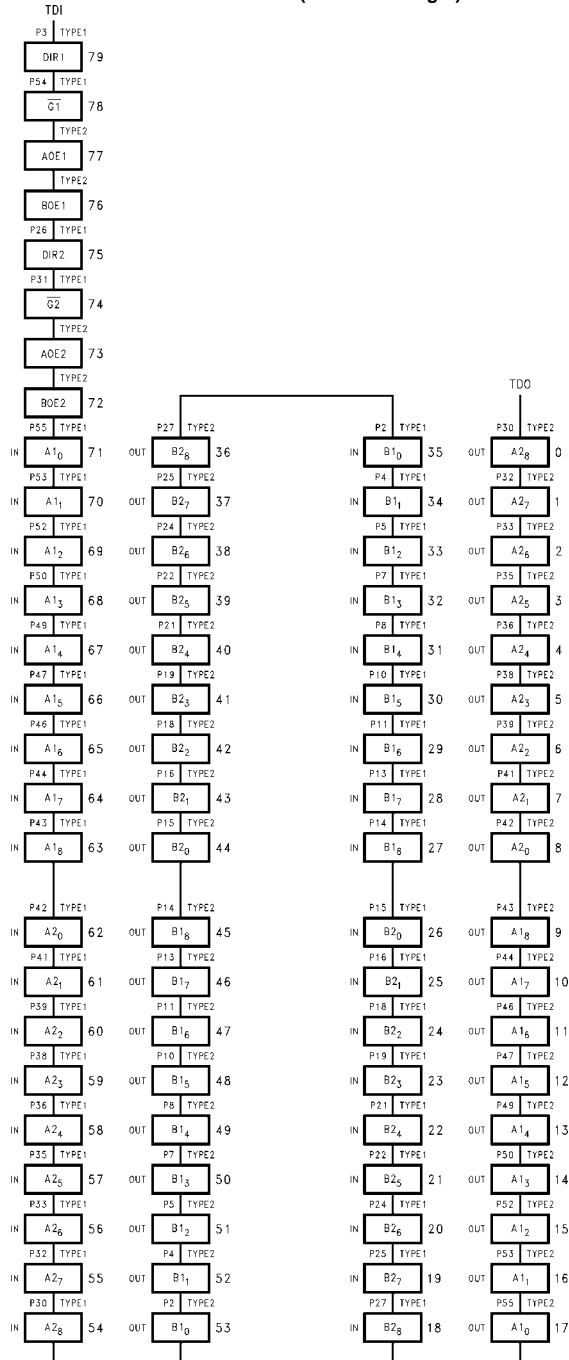
### Scan Cell TYPE1



### Scan Cell TYPE2

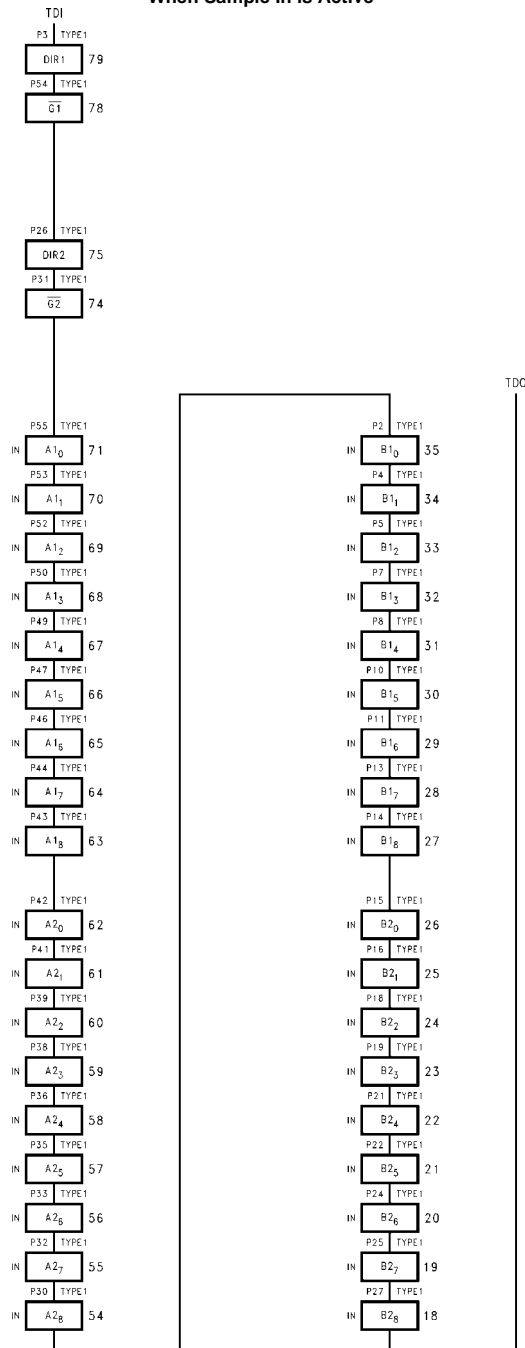


**Description of BOUNDARY-SCAN Circuitry** (Continued)  
**BOUNDARY-SCAN Register**  
**Scan Chain Definition (80 Bits in Length)**

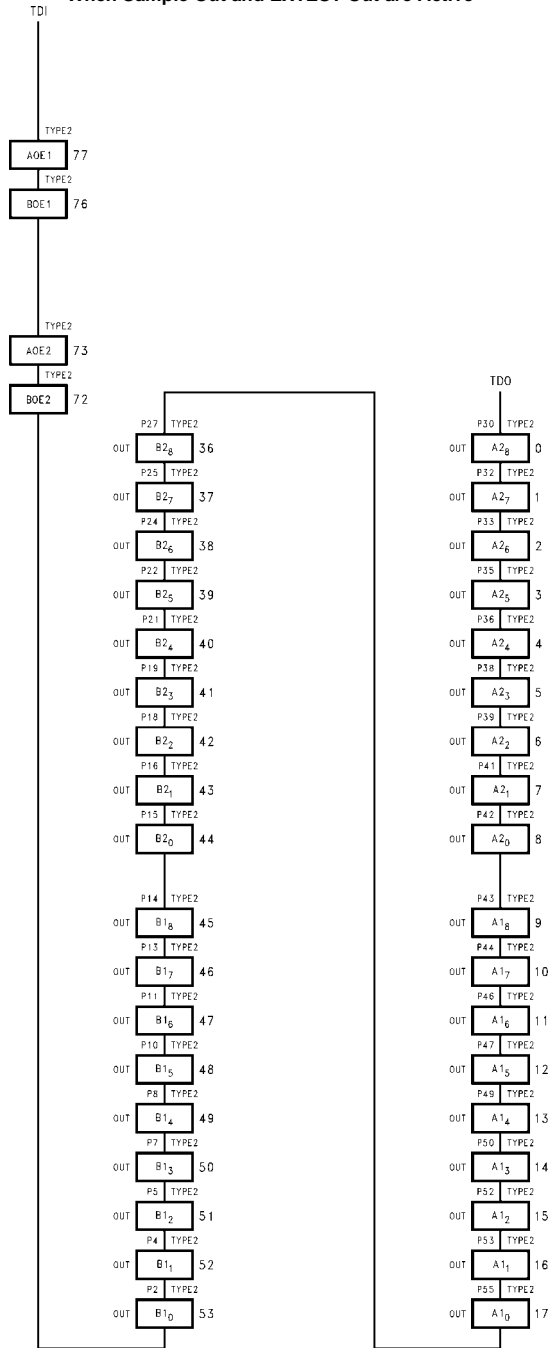


**Description of BOUNDARY-SCAN Circuitry** (Continued)  
**Input BOUNDARY-SCAN Register**  
**Scan Chain Definition (40 Bits in Length)**  
**When Sample In is Active**

SCAN182245A



**Description of BOUNDARY-SCAN Circuitry** (Continued)  
**Output BOUNDARY-SCAN Register**  
**Scan Chain Definition (40 Bits in Length)**  
**When Sample Out and EXTEST-Out are Active**



**Description of BOUNDARY-SCAN Circuitry** (Continued)  
**BOUNDARY-SCAN Register Definition Index**

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	Control Signals
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE <sub>1</sub>		Internal	TYPE2	
76	BOE <sub>1</sub>		Internal	TYPE2	
75	DIR2	26	Input	TYPE1	
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE <sub>2</sub>		Internal	TYPE2	
72	BOE <sub>2</sub>		Internal	TYPE2	
71	A1 <sub>0</sub>	55	Input	TYPE1	A1-in
70	A1 <sub>1</sub>	53	Input	TYPE1	
69	A1 <sub>2</sub>	52	Input	TYPE1	
68	A1 <sub>3</sub>	50	Input	TYPE1	
67	A1 <sub>4</sub>	49	Input	TYPE1	
66	A1 <sub>5</sub>	47	Input	TYPE1	
65	A1 <sub>6</sub>	46	Input	TYPE1	
64	A1 <sub>7</sub>	44	Input	TYPE1	
63	A1 <sub>8</sub>	43	Input	TYPE1	
62	A2 <sub>0</sub>	42	Input	TYPE1	A2-in
61	A2 <sub>1</sub>	41	Input	TYPE1	
60	A2 <sub>2</sub>	39	Input	TYPE1	
59	A2 <sub>3</sub>	38	Input	TYPE1	
58	A2 <sub>4</sub>	36	Input	TYPE1	
57	A2 <sub>5</sub>	35	Input	TYPE1	
56	A2 <sub>6</sub>	33	Input	TYPE1	
55	A2 <sub>7</sub>	32	Input	TYPE1	
54	A2 <sub>8</sub>	30	Input	TYPE1	
53	B1 <sub>0</sub>	2	Output	TYPE2	B1-out
52	B1 <sub>1</sub>	4	Output	TYPE2	
51	B1 <sub>2</sub>	5	Output	TYPE2	
50	B1 <sub>3</sub>	7	Output	TYPE2	
49	B1 <sub>4</sub>	8	Output	TYPE2	
48	B1 <sub>5</sub>	10	Output	TYPE2	
47	B1 <sub>6</sub>	11	Output	TYPE2	
46	B1 <sub>7</sub>	13	Output	TYPE2	
45	B1 <sub>8</sub>	14	Output	TYPE2	
44	B2 <sub>0</sub>	15	Output	TYPE2	B2-out
43	B2 <sub>1</sub>	16	Output	TYPE2	
42	B2 <sub>2</sub>	18	Output	TYPE2	
41	B2 <sub>3</sub>	19	Output	TYPE2	
40	B2 <sub>4</sub>	21	Output	TYPE2	
39	B2 <sub>5</sub>	22	Output	TYPE2	
38	B2 <sub>6</sub>	24	Output	TYPE2	
37	B2 <sub>7</sub>	25	Output	TYPE2	
36	B2 <sub>8</sub>	27	Output	TYPE2	

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
35	B1 <sub>0</sub>	2	Input	TYPE1	B1-in
34	B1 <sub>1</sub>	4	Input	TYPE1	
33	B1 <sub>2</sub>	5	Input	TYPE1	
32	B1 <sub>3</sub>	7	Input	TYPE1	
31	B1 <sub>4</sub>	8	Input	TYPE1	
30	B1 <sub>5</sub>	10	Input	TYPE1	
29	B1 <sub>6</sub>	11	Input	TYPE1	
28	B1 <sub>7</sub>	13	Input	TYPE1	
27	B1 <sub>8</sub>	14	Input	TYPE1	
26	B2 <sub>0</sub>	15	Input	TYPE1	B2-in
25	B2 <sub>1</sub>	16	Input	TYPE1	
24	B2 <sub>2</sub>	18	Input	TYPE1	
23	B2 <sub>3</sub>	19	Input	TYPE1	
22	B2 <sub>4</sub>	21	Input	TYPE1	
21	B2 <sub>5</sub>	22	Input	TYPE1	
20	B2 <sub>6</sub>	24	Input	TYPE1	
19	B2 <sub>7</sub>	25	Input	TYPE1	
18	B2 <sub>8</sub>	27	Input	TYPE1	
17	A1 <sub>0</sub>	55	Output	TYPE2	A1-out
16	A1 <sub>1</sub>	53	Output	TYPE2	
15	A1 <sub>2</sub>	52	Output	TYPE2	
14	A1 <sub>3</sub>	50	Output	TYPE2	
13	A1 <sub>4</sub>	49	Output	TYPE2	
12	A1 <sub>5</sub>	47	Output	TYPE2	
11	A1 <sub>6</sub>	46	Output	TYPE2	
10	A1 <sub>7</sub>	44	Output	TYPE2	
9	A1 <sub>8</sub>	43	Output	TYPE2	
8	A2 <sub>0</sub>	42	Output	TYPE2	A2-out
7	A2 <sub>1</sub>	41	Output	TYPE2	
6	A2 <sub>2</sub>	39	Output	TYPE2	
5	A2 <sub>3</sub>	38	Output	TYPE2	
4	A2 <sub>4</sub>	36	Output	TYPE2	
3	A2 <sub>5</sub>	35	Output	TYPE2	
2	A2 <sub>6</sub>	33	Output	TYPE2	
1	A2 <sub>7</sub>	32	Output	TYPE2	
0	A2 <sub>8</sub>	30	Output	TYPE2	

## SCAN ABT Live Insertion and Power Cycling Characteristics

SCAN ABT is intended to serve in Live Insertion backplane applications. It provides 2nd Level Isolation<sup>1</sup> which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V<sub>CC</sub> and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN ABT provides control of output enable pins during power cycling via the circuit in Figure 1. It essentially controls the  $\overline{G}_n$  pin until V<sub>CC</sub> reaches a known level.

During power-up, when V<sub>CC</sub> ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V<sub>CC</sub>, the Power-On-Reset circuitry, (POR), in Figure 1 becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop. The output,  $\overline{Q}$ , of the flip-flop then goes high and disables the NOR gate from an incidental low input on the  $\overline{G}_n$  pin. After 1.8V V<sub>CC</sub>, the POR circuitry becomes inactive and ceases to

control the flip-flop. To bring the device out of high impedance, the  $\overline{G}_n$  input must receive an inactive-to-active transition, a high-to-low transition on  $\overline{G}_n$  in this case to change the state of the flip-flop. With a low on the  $\overline{Q}$  output of the flip-flop, the NOR gate is free to allow propagation of a  $\overline{G}_n$  signal.

During power-down, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V<sub>CC</sub>. Again, the  $\overline{Q}$  output of the flip-flop returns to a high and disables the NOR gate from inputs from the  $\overline{G}_n$  pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V<sub>CC</sub>.

Some suggestions to help the designer with live insertion issues:

- The  $\overline{G}_n$  pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The  $\overline{G}_n$  pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of Figure 2.

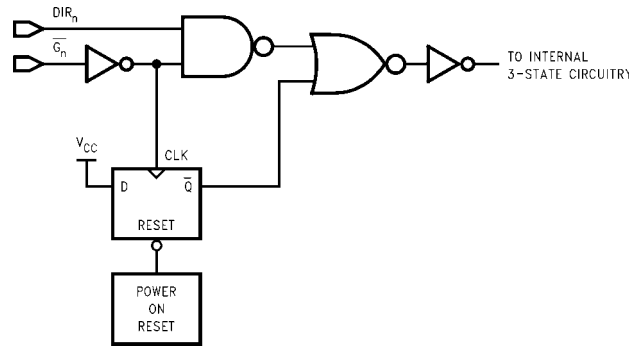
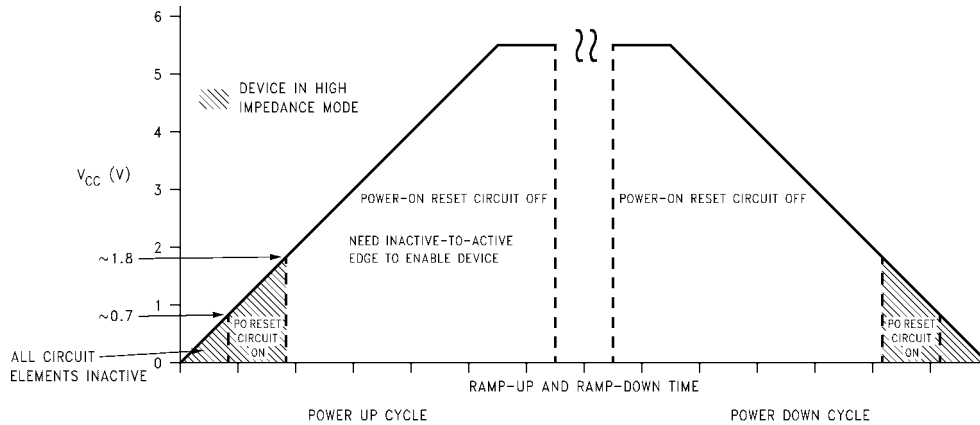


FIGURE 1.



<sup>1</sup>Section 7, "Design Consideration for Fault Tolerant Backplanes", Application Note AN-881.  
SCAN ABT includes additional power-on reset circuitry not otherwise included in ABT devices.

FIGURE 2.



### Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to +5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	Twice the Rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min.	2000V

### Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub>	Min	Typ	Max	Units	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V	Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage	Min			-1.2	V	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	Min	2.5			V	I <sub>OH</sub> = -3 mA
		Min	2.0			V	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage	Min			0.8	V	I <sub>OL</sub> = 15 mA
I <sub>IH</sub>	Input HIGH Current	All Others	Max		5	μA	V <sub>IN</sub> = 2.7V (Note 4)
			Max		5	μA	V <sub>IN</sub> = V <sub>CC</sub>
			TMS, TDI	Max		5	μA
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	Max			7	μA	V <sub>IN</sub> = 7.0V
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)	Max			100	μA	V <sub>IN</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current	All Others	Max		-5	μA	V <sub>IN</sub> = 0.5V (Note 4)
			Max		-5	μA	V <sub>IN</sub> = 0.0V
			TMS, TDI	Max		-385	μA
V <sub>ID</sub>	Input Leakage Test	0.0	4.75			V	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current	Max			50	μA	V <sub>OUT</sub> = 2.7V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current	Max			-50	μA	V <sub>OUT</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current	Max			50	μA	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current	Max			-50	μA	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	Max	-100		-275	mA	V <sub>OUT</sub> = 0.0V
I <sub>CEx</sub>	Output HIGH Leakage Current	Max			50	μA	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test	0.0			100	μA	V <sub>OUT</sub> = 5.5V, All Others GND
I <sub>CCH</sub>	Power Supply Current	Max			250	μA	V <sub>OUT</sub> = V <sub>CC</sub> ; TDI, TMS = V <sub>CC</sub>
		Max			1.0	mA	V <sub>OUT</sub> = V <sub>CC</sub> ; TDI, TMS = GND
I <sub>CCL</sub>	Power Supply Current	Max				mA	V <sub>OUT</sub> = LOW; TDI, TMS = V <sub>CC</sub>
		Max			65.8	mA	V <sub>OUT</sub> = LOW; TDI, TMS = GND
I <sub>CCZ</sub>	Power Supply Current	Max			250	μA	TDI, TMS = V <sub>CC</sub>
		Max			1.0	mA	TDI, TMS = GND
I <sub>CCt</sub>	Additional I <sub>CC</sub> /Input	All Other Inputs	Max		2.9	mA	V <sub>IN</sub> = V <sub>CC</sub> - 2.1V
		TDI, TMS inputs	Max		3	mA	V <sub>IN</sub> = V <sub>CC</sub> - 2.1V
I <sub>CCD</sub>	Dynamic I <sub>CC</sub>	No Load	Max		0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

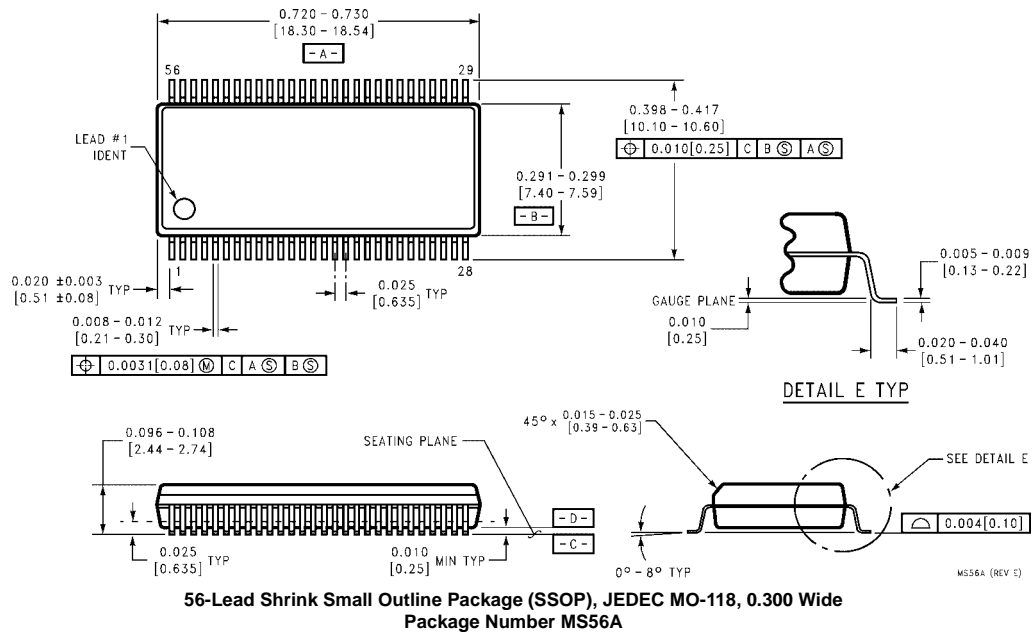
**Note 4:** Guaranteed not tested.

AC Electrical Characteristics						
Normal Operation:						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			Units
			Min	Typ	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A to B, B to A	5.0	1.0 1.5	3.1 4.4	5.2 6.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time	5.0	1.5 1.5	4.8 5.2	8.6 8.9	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Enable Time	5.0	1.5 1.5	5.5 4.6	9.1 8.2	ns
<b>Note 5:</b> Voltage Range 5.0V ± 0.5V						
AC Electrical Characteristics						
Scan Test Operation						
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			Units
			Min	Typ	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay TCK to TDO	5.0	2.9 4.2	6.1 7.7	10.2 12.1	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time TCK to TDO	5.0	2.1 3.3	5.9 7.4	10.7 12.5	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Enable Time TCK to TDO	5.0	4.6 2.8	8.7 6.8	13.7 11.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay TCK to Data Out during Update-DR State	5.0	2.8 4.5	6.3 8.2	10.7 13.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay TCK to Data Out during Update-IR State	5.0	3.3 5.0	7.2 9.3	12.2 14.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	3.7 5.7	8.4 10.8	14.0 17.2	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time TCK to Data Out during Update-DR State	5.0	2.8 3.5	7.6 8.4	13.9 14.5	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time TCK to Data Out during Update-IR State	5.0	3.6 3.8	8.7 9.2	15.1 15.9	ns
t <sub>PLZ</sub> t <sub>PHZ</sub>	Disable Time TCK to Data Out during Test Logic Reset State	5.0	4.0 4.2	9.8 9.9	17.1 16.6	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Enable Time TCK to Data Out during Update-DR State	5.0	4.4 3.0	9.3 7.5	15.5 13.3	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Enable Time TCK to Data Out during Update-IR State	5.0	5.2 3.9	10.7 9.0	17.4 15.4	ns
t <sub>PZL</sub> t <sub>PZH</sub>	Enable Time TCK to Data Out during Test Logic Reset State	5.0	5.7 3.0	12.0 10.2	19.8 17.6	ns
<b>Note 6:</b> Voltage Range 5.0V ± 0.5V						
<b>Note:</b> All Propagation Delays involving TCK are measured from the falling edge of TCK.						

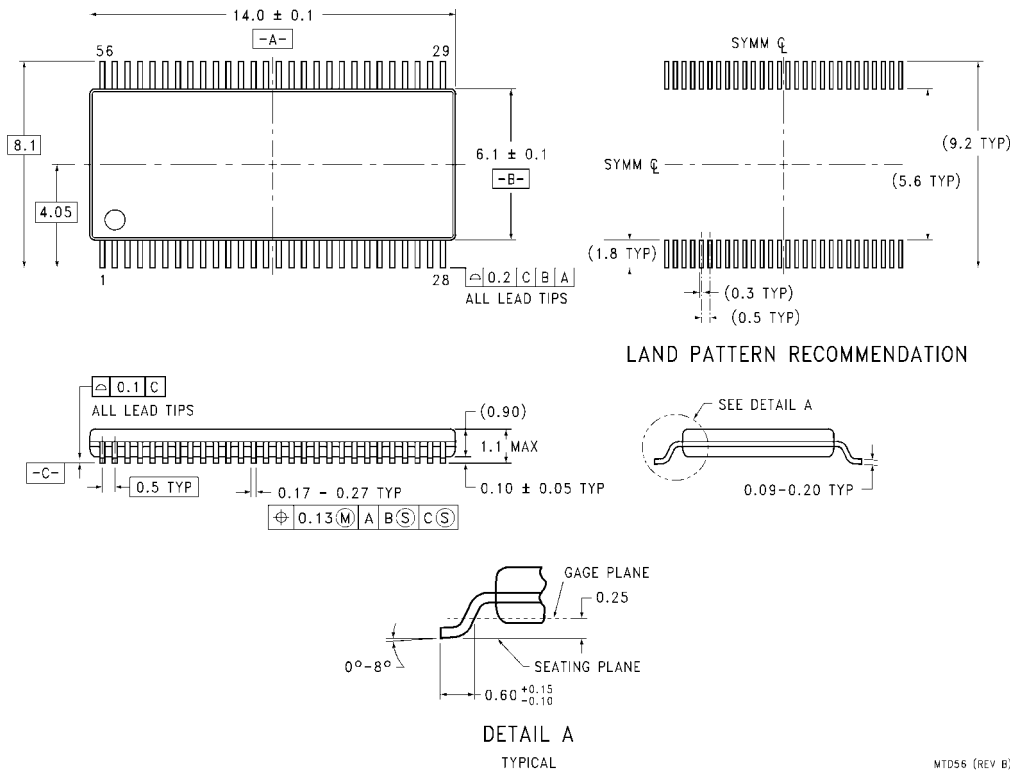
AC Operating Requirements				
Scan Test Operation				
Symbol	Parameter	V <sub>CC</sub> (V) (Note 7)	T <sub>A</sub> = -40°C to +85°C	Units
			C <sub>L</sub> = 50 pF Guaranteed Minimum	
t <sub>S</sub>	Setup Time Data to TCK (Note 8)	5.0	4.8	ns
t <sub>H</sub>	Hold Time Data to TCK (Note 8)	5.0	2.5	ns
t <sub>S</sub>	Setup Time, H or L $\overline{G1}$ , $\overline{G2}$ to TCK (Note 9)	5.0	4.1	ns
t <sub>H</sub>	Hold Time, H or L TCK to $\overline{G1}$ , $\overline{G2}$ (Note 9)	5.0	1.7	ns
t <sub>S</sub>	Setup Time, H or L DIR1, DIR2 to TCK (Note 10)	5.0	4.2	ns
t <sub>H</sub>	Hold Time, H or L TCK to DIR1, DIR2 (Note 10)	5.0	2.3	ns
t <sub>S</sub>	Setup Time Internal OE to TCK (Note 11)	5.0	3.8	ns
t <sub>H</sub>	Hold Time, H or L TCK to Internal OE (Note 10)	5.0	2.3	ns
t <sub>S</sub>	Setup Time, H or L TMS to TCK	5.0	8.7	ns
t <sub>H</sub>	Hold Time, H or L TCK to TMS	5.0	1.5	ns
t <sub>S</sub>	Setup Time, H or L TDI to TCK	5.0	6.7	ns
t <sub>H</sub>	Hold Time, H or L TCK to TDI	5.0	5.0	ns
t <sub>W</sub>	Pulse Width TCK:	H L	10.2 8.5	ns
f <sub>MAX</sub>	Maximum TCK Clock Frequency	5.0	50	MHz
t <sub>PU</sub>	Wait Time, Power Up to TCK	5.0	100	ns
t <sub>DN</sub>	Power Down Delay	0.0	100	ms
<p><b>Note 7:</b> Voltage Range 5.0V ± 0.5V</p> <p><b>Note 8:</b> Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0-8, 9-17, 18-26, 27-35, 36-44, 45-53, 54-62, 63-71).</p> <p><b>Note 9:</b> Timing pertains to BSR 74 and 78 only.</p> <p><b>Note 10:</b> Timing pertains to BSR 75 and 79 only.</p> <p><b>Note 11:</b> Timing pertains to BSR 72, 73, 76 and 77 only.</p> <p><b>Note:</b> All Input Timing Delays involving TCK are measured from the rising edge of TCK.</p>				
Capacitance				
Symbol	Parameter	Typ	Units	Conditions, T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.9	pF	V <sub>CC</sub> = 0.0V ( $\overline{G_n}$ , DIR <sub>n</sub> )
C <sub>I/O</sub> (Note 12)	Output Capacitance	13.7	pF	V <sub>CC</sub> = 5.0V (A <sub>n</sub> , B <sub>n</sub> )
<p><b>Note 12:</b> C<sub>I/O</sub> is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.</p>				

SCAN182245A

**Physical Dimensions** inches (millimeters) unless otherwise noted



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)