Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

March 2016

FDC30N20DZ

Dual N-Channel PowerTrench® MOSFET

30 V, 4.6 A, 31 mΩ

Features

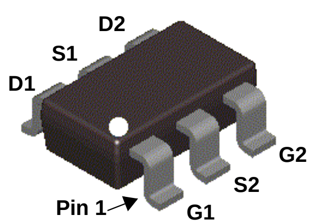
- Max $r_{DS(on)}$ = 31 mΩ at V_{GS} = 10 V, I_D = 4.6 A
- Max $r_{DS(on)}$ = 38 mΩ at V_{GS} = 4.5 V, I_D = 4.2 A
- High Performance Trench® Technology for Extremely Low $r_{DS(on)}$
- Fast Switching Speed
- 100% UIL Tested
- Typical CDM ESD protection level > 2.0 kV (Note 5)
- RoHS Compliant

General Description

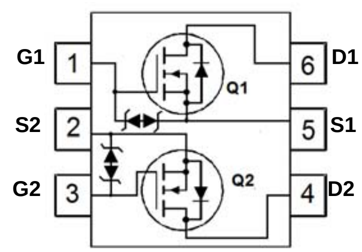
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Load Switch
- Synchronous Rectifier



SuperSOT™ -6



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		30	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	4.6	A
	-Pulsed	(Note 4)	30	A
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	3	mJ
P_D	Power Dissipation	(Note 1a)	0.96	W
	Power Dissipation	(Note 1b)	0.69	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	130	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	180	

Package Marking and Ordering Information

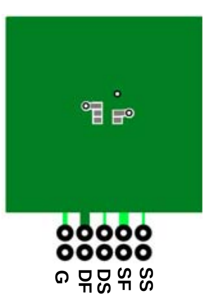
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.30N20	FDC30N20DZ	SSOT-6	7 "	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

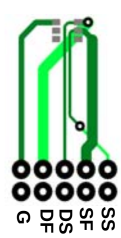
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	1	1.7	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C		-4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.6 A		23	31	mΩ
		V_{GS} = 4.5 V, I_D = 4.2 A		27	38	
		V_{GS} = 10 V, I_D = 4.6 A, T_J = 125 °C		31	42	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 4.6 A		23		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		356	535	pF
C_{oss}	Output Capacitance			110	165	pF
C_{rss}	Reverse Transfer Capacitance			18	30	pF
R_g	Gate Resistance		0.1	3.5	7.0	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 4.6 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13	21	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 4.6 A		5.6	7.9	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V		2.7	3.8	nC
Q_{gs}	Gate to Source Charge			0.9		nC
Q_{gd}	Gate to Drain “Miller” Charge			0.8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4.6 A (Note 2)		0.85	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 4.6 A, di/dt = 100 A/µs		10	20	ns
Q_{rr}	Reverse Recovery Charge			2	10	nC

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 180 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 µs, Duty cycle < 2.0%.
3. E_{AS} of 3 mJ starting T_J = 25 °C; N-ch: L = 0.1 mH, I_{AS} = 8 A, V_{DD} = 27 V, V_{GS} = 10 V.
4. Pulse Id measured at td <= 250µs, refer to SOA graph for more details.
5. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted.

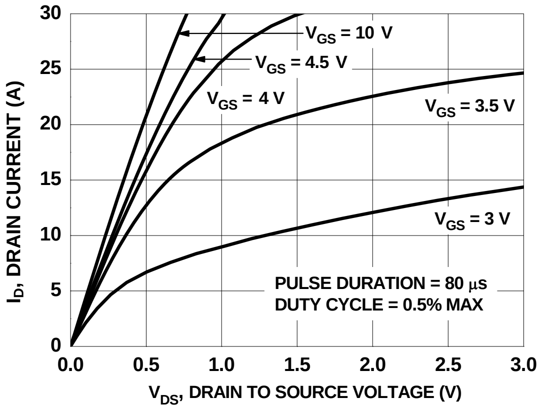


Figure 1. On-Region Characteristics

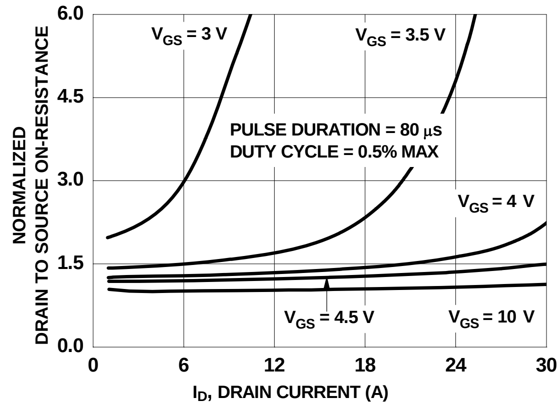


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

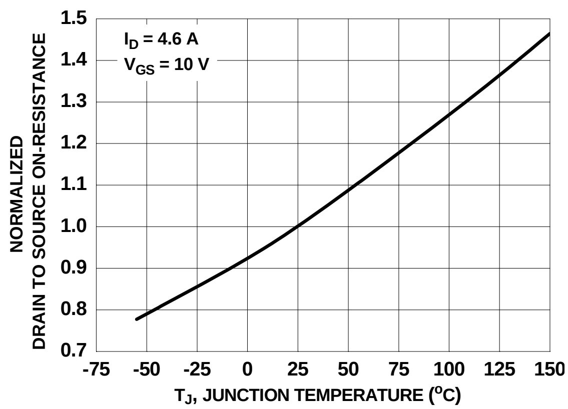


Figure 3. Normalized On-Resistance vs. Junction Temperature

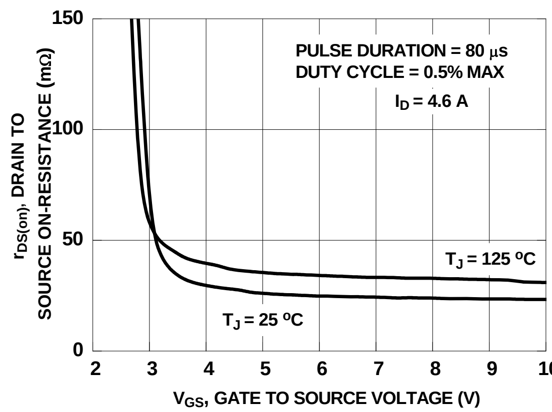


Figure 4. On-Resistance vs. Gate to Source Voltage

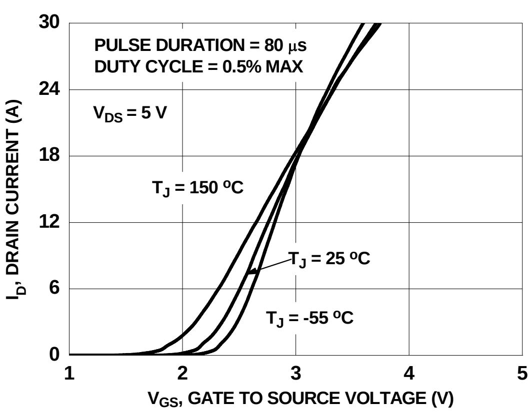


Figure 5. Transfer Characteristics

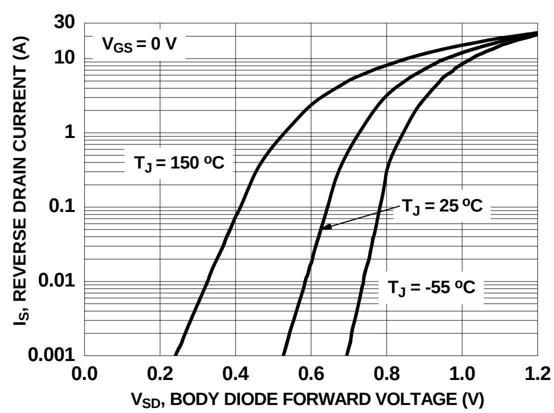


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

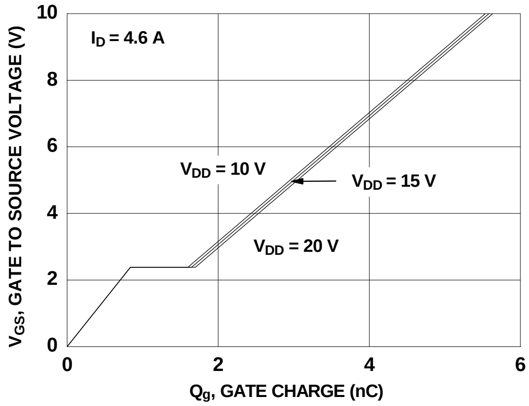


Figure 7. Gate Charge Characteristics

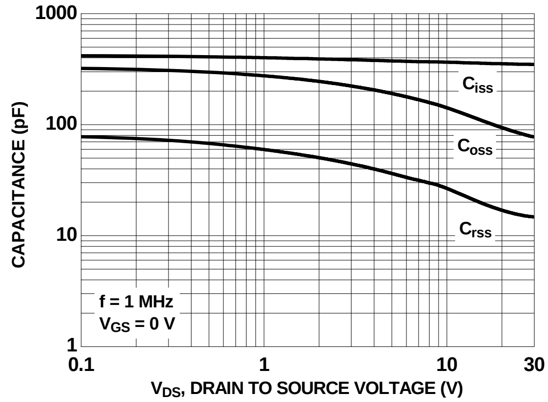


Figure 8. Capacitance vs. Drain to Source Voltage

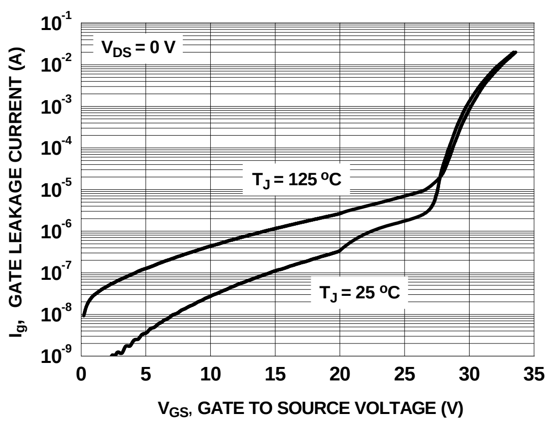


Figure 9. Gate Leakage Current vs Gate to Source Voltage

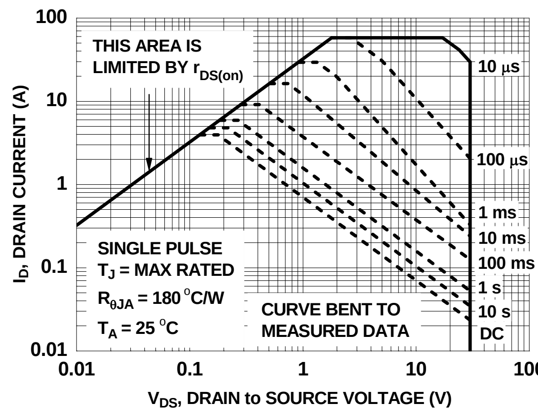


Figure 10. Forward Bias Safe Operating Area

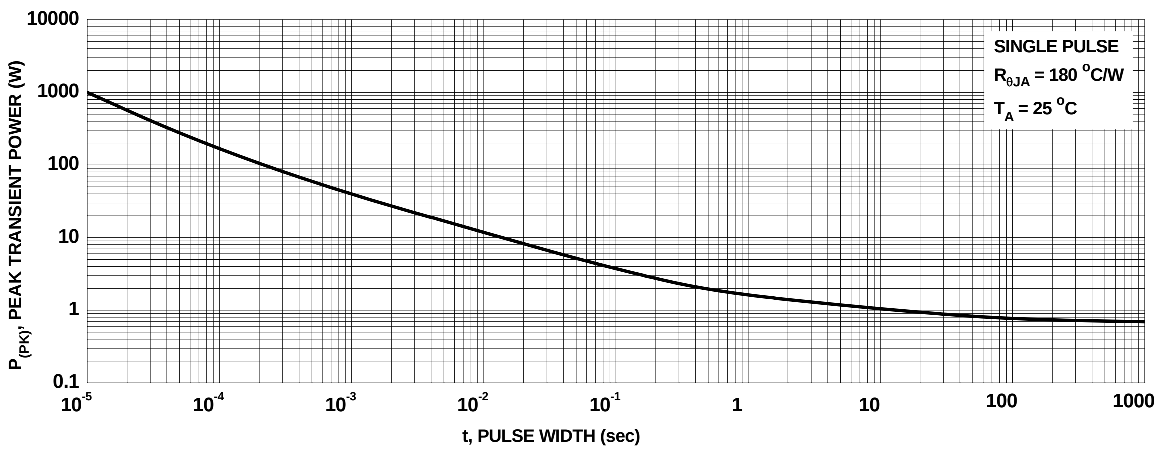


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted.

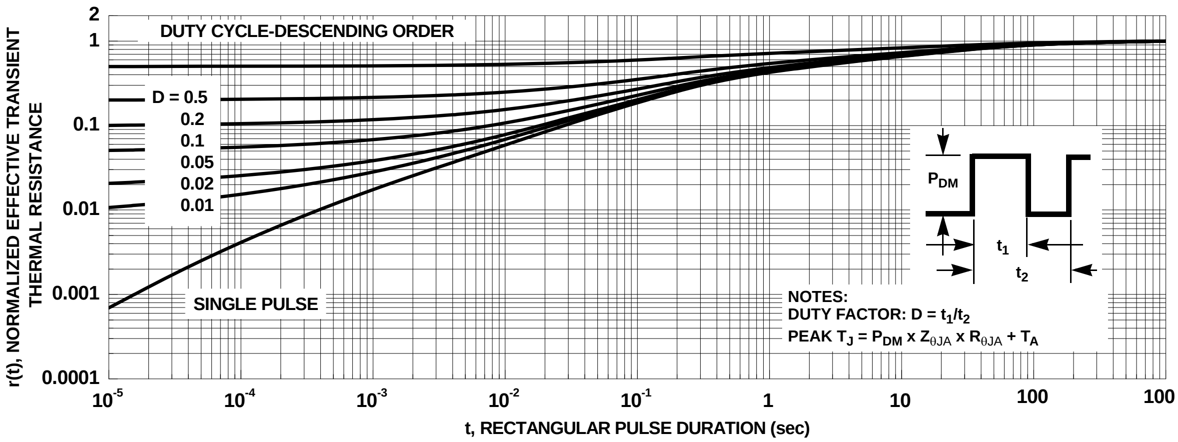
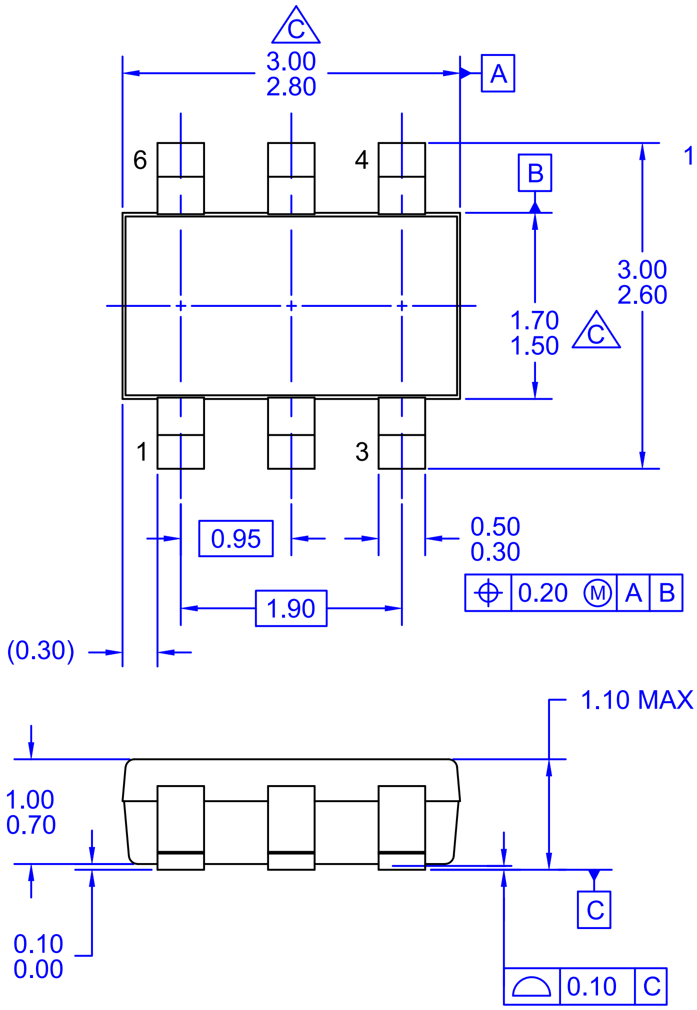
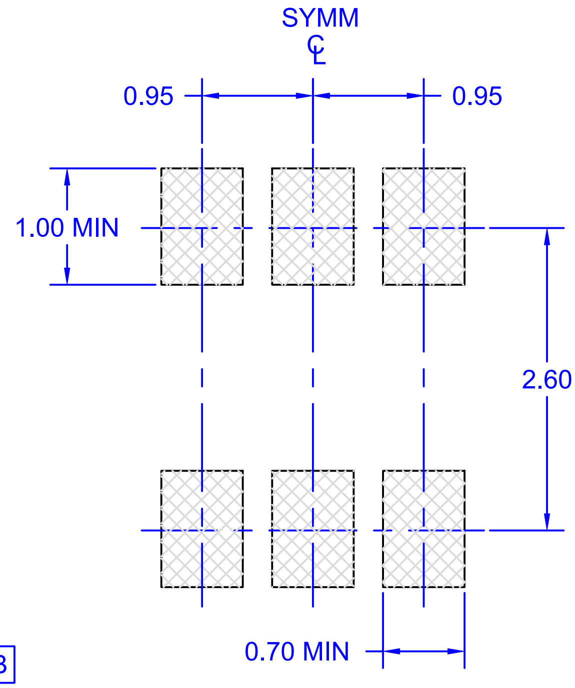
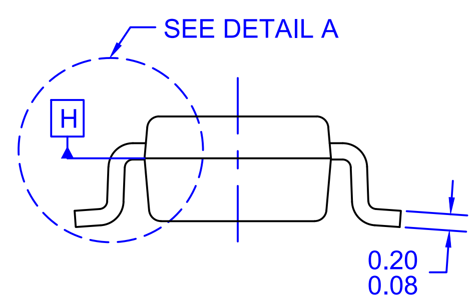


Figure 12. Junction to Ambient Transient Thermal Response Curve

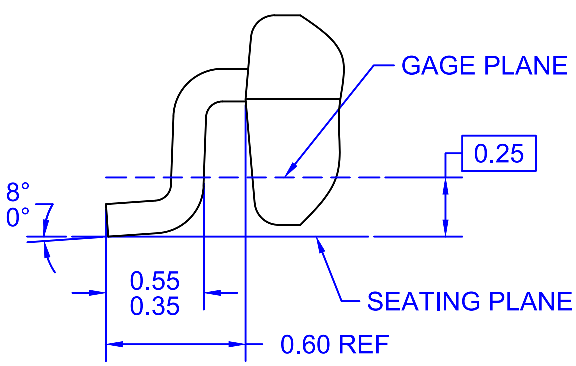




LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE E.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25mm PER END. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE. PACKAGE LENGTH AND WIDTH DIMENSIONS ARE DETERMINED AT DATUM H.
- D) DRAWING FILE NAME: MKT-MA06AREVF



DETAIL A
SCALE: 50X

ON Semiconductor

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative