

# BLU9H0408L-800P

UHF power LDMOS transistor

Rev. 1 — 26 March 2020

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

A 800 W LDMOS power transistor for UHF radar applications in the frequency range from 400 MHz to 800 MHz.

**Table 1. Typical performance**

*RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 100\ \mu\text{s}$ ;  $\delta = 10\%$ ;  $I_{Dq} = 1300\ \text{mA}$ ; in a class-AB demo circuit.*

Test signal	f	$I_{Dq}$	$V_{DS}$	$P_L$	$G_p$	$\eta_D$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
pulsed RF	410 to 460	1300	50	800	21.9	70.4
	700	1300	50	750	20.3	67.2

### 1.2 Features and benefits

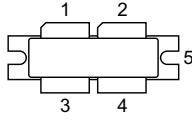
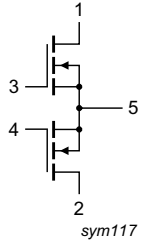
- Designed for broadband in UHF radar applications
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

### 1.3 Applications

- RF power amplifiers for UHF radar applications in the 400 MHz to 800 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLU9H0408L-800P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<sup>[1]</sup>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; V_{DS} = 50\text{ V}; P_L = 300\text{ W}$	0.13	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 2.4\text{ mA}$	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 240\text{ mA}$	1.5	2.2	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	41	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 8.5\text{ A}$	-	90	-	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: pulsed RF;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$  at  $V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production circuit measured at frequency of 700 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 750\text{ W}$	19.5	20.5	-	dB
$RL_{in}$	input return loss	$P_L = 750\text{ W}$	-	-7	-	dB
$\eta_D$	drain efficiency	$P_L = 750\text{ W}$	64	67.5	-	%

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLU9H0408L-800P is capable of withstanding a load mismatch corresponding to  $VSWR = 20 : 1$  through all phases under the following conditions:  $V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $P_L = 750\text{ W}$  (pulsed CW);  $f = 700\text{ MHz}$ . Pulsed conditions:  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\%$ .

7.2 Test circuit

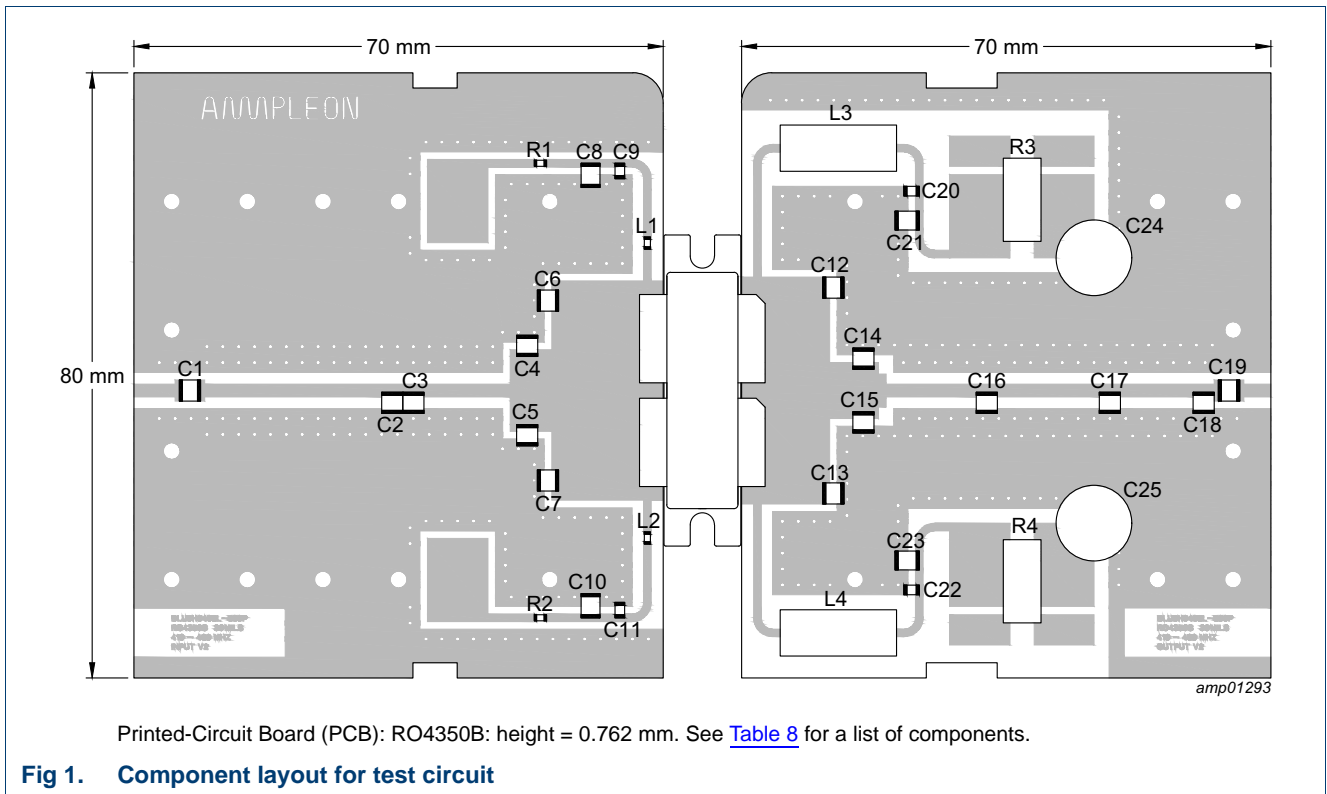


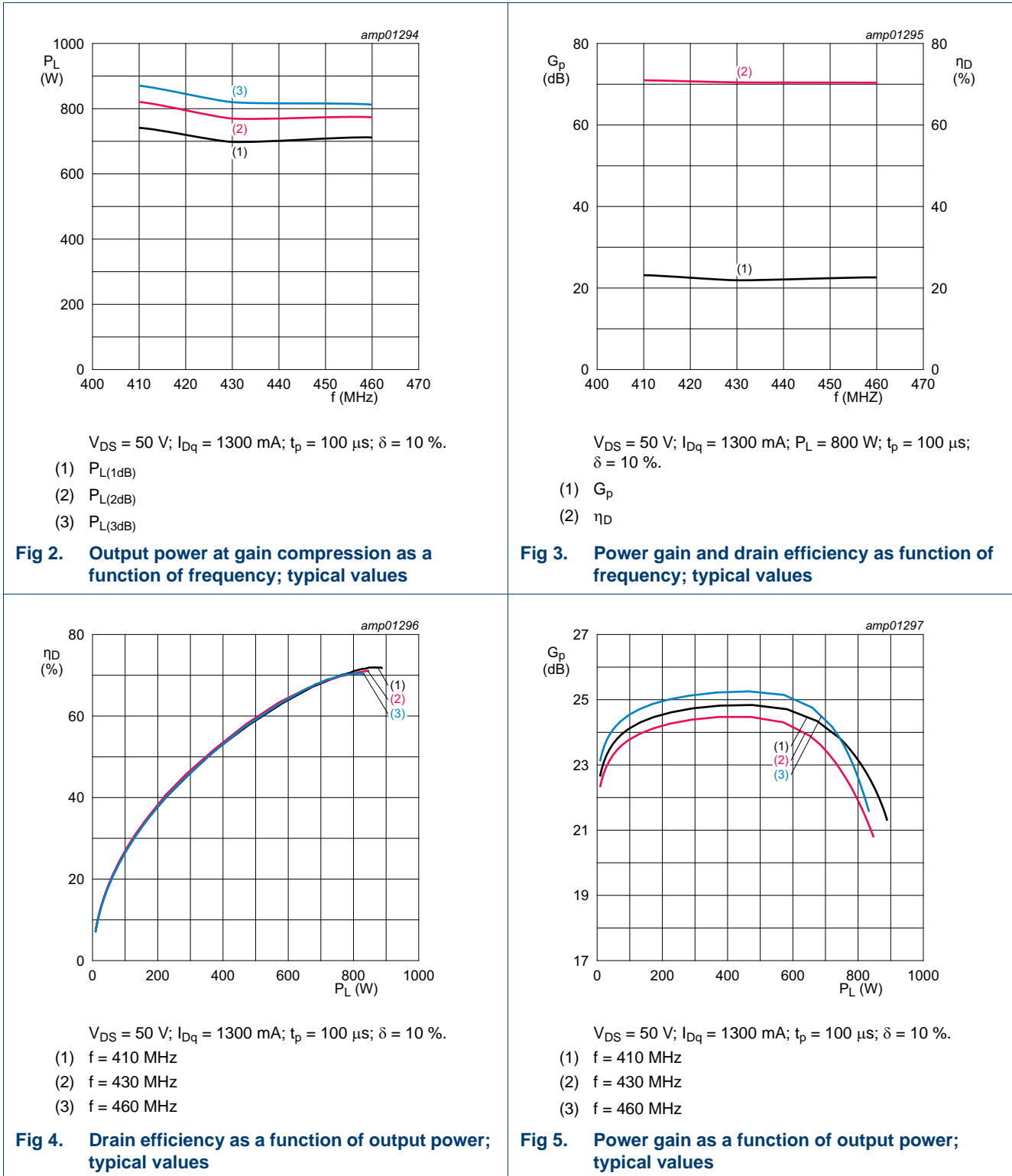
Fig 1. Component layout for test circuit

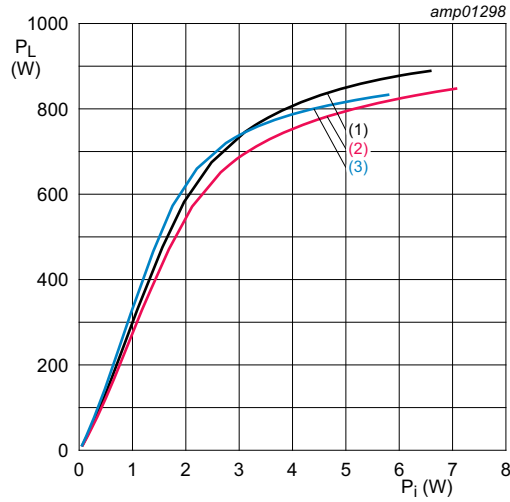
Table 8. List of components  
See [Figure 1](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	36 pF	
C2	multilayer ceramic chip capacitor	3.6 pF	
C3	multilayer ceramic chip capacitor	24 pF	
C4, C5	multilayer ceramic chip capacitor	33 pF	
C6, C7	multilayer ceramic chip capacitor	56 pF	
C8, C10, C21, C23	multilayer ceramic chip capacitor	4.7 $\mu$ F	
C9, C11, C20, C22	multilayer ceramic chip capacitor	0.1 $\mu$ F	
C12, C13	multilayer ceramic chip capacitor	13 pF	
C14, C15	multilayer ceramic chip capacitor	56 pF	
C16	multilayer ceramic chip capacitor	20 pF	
C17	multilayer ceramic chip capacitor	1.0 pF	
C18	multilayer ceramic chip capacitor	1.8 pF	
C19	multilayer ceramic chip capacitor	11 pF	
C24, C25	electrolytic capacitor	1000 $\mu$ F	
L1, L2	wire wound surface mount inductor	56 nH	
L3, L4	6 turn air core inductor	150 nH	
R1, R2	surface mount resistor	5.6 $\Omega$	
R3, R4	current sense resistor	5 m $\Omega$	

7.3 Graphical data

7.3.1 Pulsed CW performance (f = 410 MHz to 460 MHz)

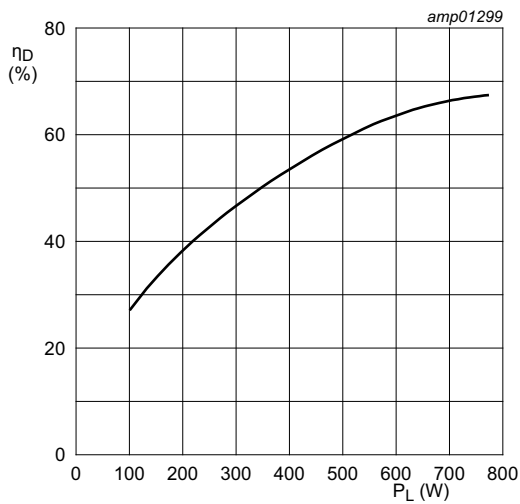




$V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .  
 (1)  $f = 410\text{ MHz}$   
 (2)  $f = 430\text{ MHz}$   
 (3)  $f = 460\text{ MHz}$

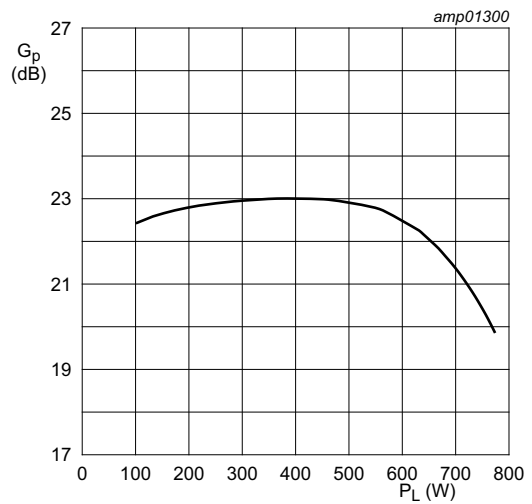
Fig 6. Output power as a function of input power; typical values

7.3.2 Pulsed CW performance (f = 700 MHz)



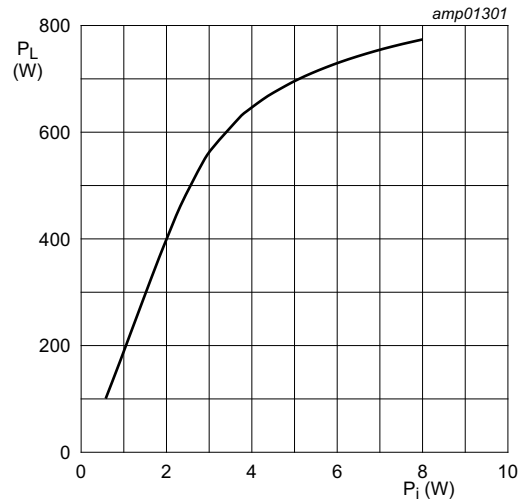
$V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

Fig 7. Drain efficiency as a function of output power; typical values



$V_{DS} = 50\text{ V}$ ;  $I_{Dq} = 1300\text{ mA}$ ;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 10\text{ }\%$ .

Fig 8. Power gain as a function of output power; typical values



$V_{DS} = 50 \text{ V}$ ;  $I_{Dq} = 1300 \text{ mA}$ ;  $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 10 \text{ \%}$ .

**Fig 9. Output power as a function of input power; typical values**

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

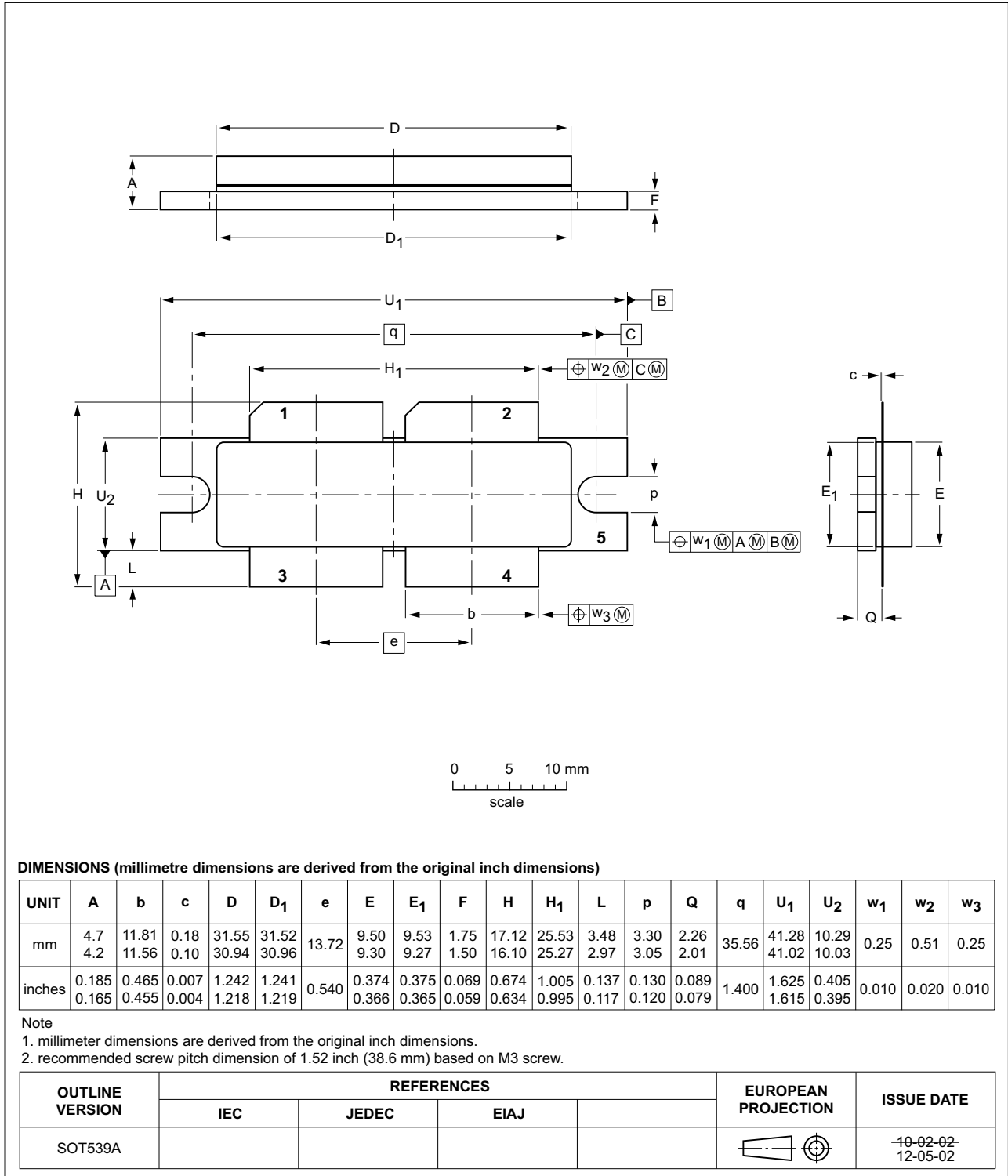


Fig 10. Package outline SOT539A



## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.  
Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 9. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLU9H0408L-800P v.1	20200326	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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