Synchronous Rectifier Driver with Power Up/Down Control, Output OVP, Error Amplifier and Precision Reference

DESCRIPTION

The SiP11203/SiP11204 provide the secondary side error amplifier, reference voltage and synchronous rectifier drivers for isolated converter topologies. Both ICs are capable of being powered via conventional bias supplies (output inductor winding or power transformer winding), or from a pulse transformer supplying the gate timing signals, and both parts generate a regulated supply for powering the error amplifier and control circuitry.

During power-up the SiP11203/SiP11204 ensure that the synchronous rectifiers are held off until the supply voltages are adequate to guarantee effective operation of the driver circuits. During the soft-start interval, a gradual ramp-up of the synchronous rectifier conduction time is provided. Both ICs also allow control of the discharge rate of the synchronous rectifier driver outputs during power-down.

The SiP11203 and SiP11204 are available in a Pb-free MLP44-16 package and are rated to handle the industrial ambient temperature range of - 40 to 85 °C.

FEATURES

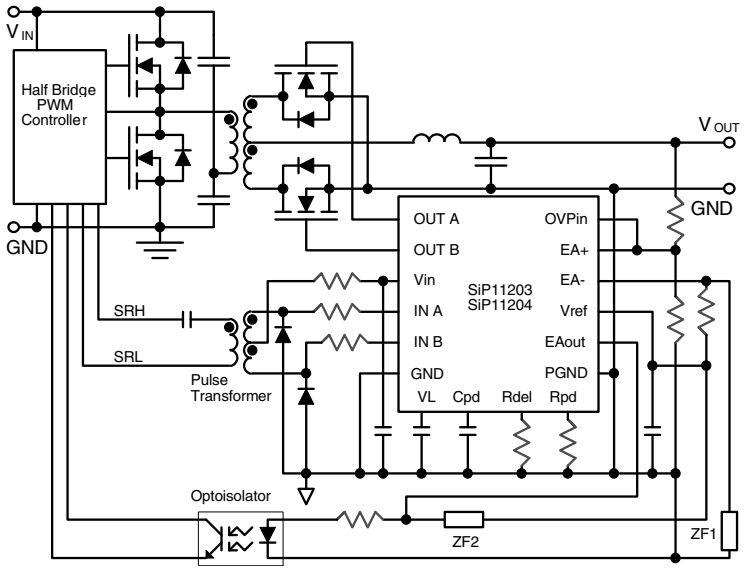
Pb-free

- High Current synchronous rectifier drivers
  - 2.2 A source and 4 A sink
- Driver switching synchronized with primary controller
- Full output control during power-up and power-down
- 5.5 V to 13 V operating voltage range
- 1.225 V on board bandgap voltage reference
- Can be powered from the pulse transformer supplying synchronous rectifier timing signals
- On-chip ground-sensing error amplifier
- Programmable rising edge delay
- Output over-voltage protection (OVP)
  - SiP11203 turns synchronous rectifiers on
  - SiP11204 turns synchronous rectifiers off
- Secondary-side companion chip for the Si9122 Half-Bridge Controller IC

APPLICATIONS

- High efficiency DC-DC Converter Modules and Bricks
- Telecom and Server Power Supplies
- High Efficiency Intermediate Bus Converters (IBC)
- Half-bridge, full-bridge, or push-pull primary DC-DC topologies
- Center-tapped or current-doubler secondary configurations

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V_{IN}, IN_A, IN_B		15	V
V_{REF}, Linear Inputs		- 0.3 to V_L + 0.3	
Storage Temperature		- 65 to + 160	°C
Junction Temperature		- 40 to + 125	
Package Thermal Impedance ($R\theta_{JA}$)	16 Pin 44MLP	47	°C/W
	Package Power Dissipation (package)[a]	745	mW

Notes:
a. Device mounted with all leads soldered to printed circuit board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Limit	Unit
V_{IN}	5.5 to 13	V
C_{VIN}	1	µF
C_{VL}	1	
C_{REF}	0.1	
Linear Inputs (EA+, EA-, OVP_{IN})	0 to V_L	
Error Amplifier Output Voltage	0 to 3.5	V
Logic Inputs (IN_A, IN_B)	0 to 13	
Reference voltage output current	10	µA
R_{PD}	> 15	kΩ
C_{PD}	1 to 10	nF

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 5.5 V ≤ V_{IN} ≤ 13 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Power Supply						
V_L Output Voltage	V_L	Output disabled (Note e)	4.75	5	5.25	V
V_L Temperature Coefficient	TC1	(Note c)		160		µV/°C
V_L Line Regulation	V_{L_LNR}	I_L = 0 mA		3	8	mV
V_L Load Regulation	V_{L_LDR}	I_L = 0 mA to 3.3 mA, V_{IN} = 5.5 V		1.2	10	
V_L Supply PSRR	V_{L_PSRR}	f_{TEST} =100 Hz, (Note c)		70		dB
Supply Current	I_{IN}	V_{IN} = 5.5 V, $C_{LOAD(A)}$ = $C_{LOAD(B)}$ = 6 nF (Note c, d)		12		mA
		V_{IN} = 7.5 V, $C_{LOAD(A)}$ = $C_{LOAD(B)}$ = 6 nF (Note c, d)		15.5		
Quiescent Current	I_Q	Device switching disabled (Note e)		3.5	4.5	
Start-up Current Capability	$I_{STARTUP}$	Current sourced from V_{IN} to V_L, V_L = 0 V	35	45	55	
Reference Voltages						
V_{REF} Voltage	V_{REF}	I_{REF2} = 0 mA, T_A = 25 °C	1.212	1.225	1.238	V
		I_{REF2} = 0 mA	1.188	1.225	1.262	
V_{REF} Temperature Coefficient	TC2	(Note c)		160		µV/°C
V_{REF} Load Regulation	V_{REF_LDR}	V_{IN} = 5.5 V, I_{REF} = 0 to 10 µA		1.5	2.5	mV
V_{REF} PSRR	V_{REF_PSRR}	f_{TEST} = 100 Hz, (Note c)		60		dB
Internal Buffered Reference Voltage	V_{REFINT}	V_{IN} = 5.5, measured at R_{PD} pin	2.320	2.5	2.570	V

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 5.5 V ≤ V_{IN} ≤ 13 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Logic Inputs - IN A and IN B						
Input High	V_{IH}	Rising	4	2.5		V
Input Low	V_{IL}	Falling		2.1	1	
Input Resistance	R_{IN}	V_{IN} = 13 V, 13 V at INA and/or INB	3	3.8	4.5	kΩ
Input Frequency Range (INA and INB)	f_{IN}	(Note c)	100		500	kHz
Error Amplifier - DC Electrical Characteristics						
Voltage Gain	A_V	20 log ($\Delta V_{OUT}/\Delta V_{OS}$) for V_{OUT} = 0.5 V to 3 V	65	70		dB
Common Mode Rejection Ratio	CMRR	Input CMR = 0 V to 3.5 V	60	65		
Input Offset Voltage	V_{OS}	V_{CM} = 1.225 V, R_{LOAD} = 10 kΩ to V_{CM}		± 3	± 15	mV
V_{OS} Temperature Coefficient	TC3	(Note c)		30		µV/°C
Input Bias Current	I_{BIAS}	V_{CM} = 1.225 V		2	10	nA
Input Offset Current	I_{OS}	(I_{EA+}) - (I_{EA-}), (Note c)		± 0.3		
Output Voltage	V_{OL}	Output sinking 0.8 mA		225	400	mV
	V_{OH}	Output sourcing 0.8 mA	3	3.45		V
Output Current	I_{OH}	Sourcing, EA_{OUT} = 1 V, EA+ overdrive = 500 mV	3.5	4.7		mA
	I_{OL}	Sinking, EA_{OUT} = 2.5 V, EA+ overdrive = 500 mV	0.8	1.3		
Error Amplifier - AC Electrical Characteristics						
Gain-Bandwidth Product	BW	(Note c)		1		MHz
Slew Rate	SR+	Rising, R_{LOAD} = 2 kΩ II 1 nf to Ground		0.75		V/µs
	SR-	Falling, R_{LOAD} = 2 kΩ II 1 nf to Ground		1		
MOSFET Drivers						
Driver Impedance	$R_{D(SOURCE)}$	V_{IN} = 5.5 V, I_{OUT} = 100 mA, T_J = 25 °C		2.3	3.7	Ω
	$R_{D(SINK)}$			1.5	2.4	
	$R_{D(SOURCE)}$	V_{IN} = 7.5 V, I_{OUT} = 100 mA, T_J = 25 °C		2.1	3.4	
	$R_{D(SINK)}$			1.4	2.2	
Peak Drive Current	$I_{PK(SOURCE)}$	V_{IN} = 5.5 V, T_J = 25 °C (Note c)		1.2		A
	$I_{PK(SINK)}$			2.4		
	$I_{PK(SOURCE)}$	V_{IN} = 7.5 V, T_J = 25 °C (Note c)		2.2		
	$I_{PK(SINK)}$			4		
Rise Time	t_r	10 % to 90 %, V_{IN} = 5.5 V, C_{LOAD} = 6 nF, (Note c)		45		ns
		10 % to 90 %, V_{IN} = 7.5 V, C_{LOAD} = 6 nF, (Note c)		42		
Fall Time	t_f	90 % to 10 %, V_{IN} = 5.5 V, C_{LOAD} = 6 nF, (Note c)		35		
		90 % to 10 %, V_{IN} = 7.5 V, C_{LOAD} = 6 nF, (Note c)		32		
IN to OUT Propagation Delay	t_{pdr}	INA/INB rising to OUTA/OUTB rising, 50 % to 50 % V_{IN} = 5.5 V, R_{DEL} connected to V_L, C_{LOAD} = 0 nF	20	32	55	
	t_{pdf}	INA/INB falling to OUTA/OUTB falling, 50 % to 50 % V_{IN} = 5.5 V, R_{DEL} connected to V_L, C_{LOAD} = 0 nF	20	34	55	
Additional Rising Edge OUT A/B Delay vs. R_{DEL}	Δt_{DELAY}	R_{DEL} connected to V_L			0	
		R_{DEL} = 25 kΩ to GND, C_{LOAD} = 0 nF (Note d)	28	38	48	
Power-down Detection Timeout	t_{PDDET}	IN A and IN B low to OUT A/OUT B low R_{PD} = 25 kΩ, C_{PD} = 1 nF (Note c)		25		µs
Power-up Output Hold-off Current	I_{HOFF}	No forcing voltage on V_{IN} or V_L, both V_{IN} and V_L bypassed by 1 µF to GND, INA or INB = 5 V, other input = 0 V, force 1 V at active output (A or B)	350	530		mA

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified 5.5 V ≤ V_{IN} ≤ 13 V, T_A = - 40 °C to 85 °C	Limits Min.[a]	Typ.[b]	Max.[a]	Unit
Under Voltage Lockout Section						
UVLO Threshold (Rising)	$UVLO_R$	V_{IN} Rising until output transitions on	4.3	4.45	4.6	V
UVLO Threshold (Falling)	$UVLO_F$	V_{IN} Falling until output transitions off	2.9	3.05	3.2	
UVLO Hysteresis	$V_{HYS(UVLO)}$	$UVLO_R$ - $UVLO_F$, I_L = 0 mA	1.25	1.40	1.55	
Output Overvoltage Protection						
Force Outputs On Threshold	OVP_R	Rising voltage on OVP_{IN} to force OUTA and OUTB high	1.40	1.47	1.55	V
Resume Normal Operation Threshold	OVP_F	Falling voltage on OVP_{IN} to allow OUTA and OUTB to go low	1.06	1.13	1.20	
Hysteresis	$V_{HYS(OVP)}$	OVP_R - OVP_F	0.30	0.35	0.40	
Housekeeping Supply Section						
IC logic enable	$CUVLO_R$	V_{IN} Rising until current at V_{IN} > 1 mA	3.35	3.55	3.70	V
IC logic disable	$CUVLO_F$	V_{IN} Falling until current at V_{IN} < 0.25 mA	2.90	3.05	3.20	
Hysteresis	$V_{HYS(CUVLO)}$	$CUVLO_R$ - $CUVLO_F$	0.35	0.50	0.65	

Notes:

a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum and over - 40 °C to 85 °C.

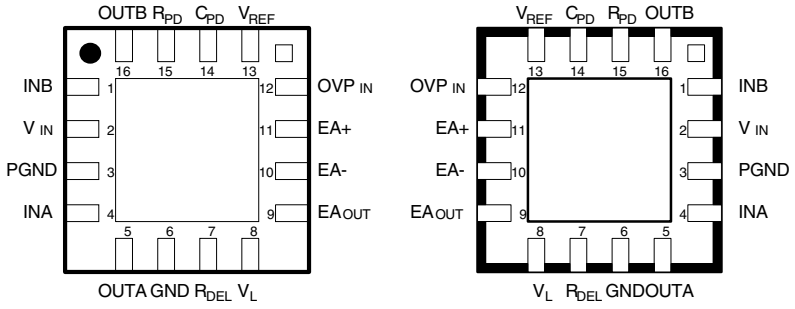
b. Typical values are specified for 25 °C operation, and are for design reference only.

c. Not 100 % tested in production. This information is provided for reference only.

d. IN A or IN B switching at 250 kHz, R_{DEL} = 25 kΩ to ground.

e. IN A = step 5 to 0 V and IN B = 5 V or vice versa, R_{DEL} = 25 kΩ to ground, error amplifier configured as voltage follower with EA+ connected to V_{REF}.

PIN CONFIGURATION



Top View Bottom View

MLP44-16

ORDERING INFORMATION

Part Number	Marking	Ambient Temperature Range
SiP11203DLP-T1-E3	11203	- 40 ° to 85 °C
SiP11204DLP-T1-E3	11204	

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	INB	Logic input for output driver B
2	V_{IN}	Input supply voltage
3	PGND	Power ground
4	INA	Logic input for output driver A
5	OUTA	Driver output A
6	GND	Analog ground (connect GND to the exposed pad of the IC package)
7	R_{DEL}	Sets output rising edge delay
8	V_L	5 V supply voltage for internal circuitry
9	EA_{OUT}	Error amplifier output
10	EA-	Error amplifier inverting input
11	EA+	Error amplifier non inverting input
12	OVP_{IN}	Input pin for over voltage detection
13	V_{REF}	1.225 V reference voltage for converter output voltage regulating setting
14	C_{PD}	Capacitor value sets power down detection time in conjunction with R_{PD}
15	R_{PD}	Resistor value sets currents for power down detection timer and for power down discharge of outputs
16	OUTB	Driver output B

FUNCTIONAL BLOCK DIAGRAM

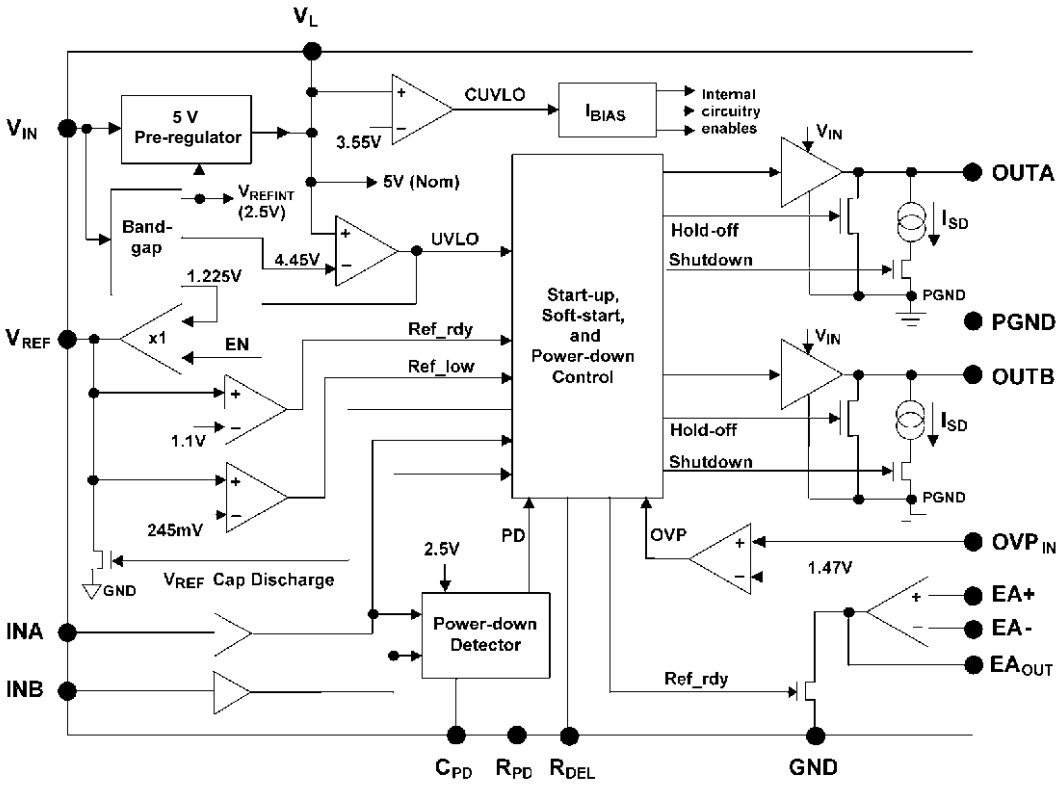


Figure 1.

DETAILED OPERATION

SUPPLY VOLTAGE (V_{IN})

The SiP11203/SiP11204 are designed to operate at an input voltage (V_{IN}) between 5.5 V and 13 V. The synchronous rectifier drivers (OUTA and OUTB) are powered directly from V_{IN}, to facilitate setting the gate drive voltage for the rectifier MOSFETs. Due to the high peak currents available from the SiP11203/ SiP11204 outputs, careful attention must be paid to the bypassing of V_{IN} to PGND.

Internal Supply (V_L)

In order to provide the internal circuitry of the SiP11203/SiP11204 with a stable supply voltage (V_L), the SiP11203/SiP11204 incorporate a linear pre-regulator. Operating from V_{IN}, the pre-regulator provides a fixed V_L of 5 V for use by the majority of the chip. V_L is regulated by V_{REFINT}, and therefore does not depend upon the voltage at the V_{REF} pin. For proper IC operation, a bypass capacitor on the order of 1µF should be connected between V_L and GND.
In normal operation, V_L is intended to accommodate the internal light load requirements, such as bias networks and the sourcing capability of the error amplifier's output.

Start-up Considerations

The average pre-regulator output current available to charge the V_L bypass capacitor, and the value of that capacitor, play an important part in the start-up sequencing of the SiP11203/SiP11204. Until V_L reaches the Chip Undervoltage Lockout threshold (CUVLO), the part is held in a low-current standby state. When V_L exceeds the CUVLO voltage of 3.55 V, the majority of the on-chip circuitry is enabled, with the exception of the reference voltage buffer and the output drivers (OUTA and OUTB). Finally, when the main Undervoltage Lockout threshold ($UVLO_R$) is reached, which occurs when V_L reaches 90 % of its final value, the V_{REF} buffer and the output drivers are enabled. This in turn allows the V_{REF} pin to source current, and the outputs to respond to the INA and INB inputs. See Figure 4, in the Applications Information Section.

The I-V characteristic of the pre-regulator approximates that of a constant current source. With V_{IN} = 7.5 V, the typical I_{OUT} at the V_L pin for voltages between 0 V and the final regulated voltage of 5 V is 35 mA.

REFERENCE VOLTAGE (V_{REF})

The SiP11203/SiP11204 incorporate an internal voltage reference of 2.5 V. This is scaled and buffered to drive the V_{REF} pin at 1.225 V. The accuracy of V_{REF} is ± 1 % at 25 °C, with a temperature coefficient of ± 160 µV/°C, yielding a worst-case accuracy over temperature of ± 3 % (- 40 °C to + 85 °C).

Start-up and Soft-Start Considerations

V_{REF} is held at 0 V until V_L has exceeded its $UVLO_R$ threshold. This allows a soft-start function to be implemented by controlling the rate of rise of voltage on the V_{REF} pin, which in turn causes a gradual rise in the target voltage of the error amplifier and its associated voltage control loop. See Figure 4, in the Applications Information Section.
The charging rate (dV/dt) of V_{REF} is user-settable by choice of V_{REF} bypass capacitor value. The I-V characteristic of the reference output approximates that of a constant current source, with the typical I_{OUT} at the V_{REF} pin for voltages between 0 V and the final regulated voltage of 1.225 V being 410 µA. See the graph "V_{REF} Start-up."

ERROR AMPLIFIER

The error amplifier is biased from the internal 5 V supply (V_L). The input common mode range extends down to ground and up to 3.5 V. The output stage can source in excess of 4 mA and can sink 1 mA. The output stage is comprised of a class-A source follower working into a 1 mA pull down (current sink), and is designed to drive light loads such as an optocoupler and the series resistor. The output source current I_{OH} is limited by an internal 500 Ω resistor, to protect the output in the event of a short to GND. When sourcing current in excess of 1 mA, the voltage drop across this resistor should be taken into account (see graph of V_{OH} vs. I_{LOAD}). The 1 MHz amplifier has 75 degrees of phase margin, and a large signal slew rate is (1 V/µs) in a unitygain configuration. The input offset voltage is typically 3 mV at 25 °C, and the offset voltage temperature coefficient is typically 30 uV/°C. Due to its CMOS inputs, the amplifier has low input bias and offset currents. Both amplifier inputs as well as the output are accessible, to facilitate meeting the compensation requirements of specific applications. Note that the error amplifier output is clamped low until the V_L voltage has increased past the $CUVLO_R$ voltage level.

MOSFET RECTIFIER DRIVERS

Start-Up

At converter start-up, V_L will typically be at or near 0 V. Until such time as the $UVLO_R$ threshold is exceeded, the main synchronous rectifier drivers are disabled, as the supply voltage for the IC may be insufficient to ensure that the output drivers will fully respond to input commands. Without precautionary measures, capacitive coupling between the drains and gates of the synchronous rectifiers could cause spurious conduction in the rectifiers. To prevent this, special hold-off MOSFETs are switched in until the main drivers are enabled. These internal hold-off MOSFETs, which connect from OUTA to PGND and OUTB to PGND, can typically conduct in excess of 400 mA with 1 V on OUTA or OUTB ($Z_{OUT} \cong 2.5\ \Omega$). Once V_L rises above $UVLO_R$, the main drivers are enabled and the part assumes its normal mode of operation, with pulses at INA being used to control OUTA and pulses at INB being used to control OUTB. Figure 3 and its related text provide additional details on this topic.

Normal Operation

When enabled, the main driver outputs are non-inverting with respect to the input signal. The drivers are designed to provide the high peak currents (2 - 4 A) required to rapidly charge and discharge the gates of large synchronous rectifier MOSFETs, with a greater turn-off (pull-down) current than turn-on (pull-up) current, to prevent shoot-through in the synchronous rectifiers.

Shut-Down

In the typical application circuit, cessation of primary timing signals at INA and INB would cause both OUTA and OUTB to be pulled high, which at the system level would short-circuit of the converter output to ground via the synchronous rectifiers. To avoid possible negative effects of such an event, the SiP11203/SiP11204 uses a missing-pulses detector to monitor INA and INB and, if necessary, set the main output drivers to a high-impedance state. At the same time that the main drivers are disabled, a pull-down device (current sink) of user-settable value is enabled on each output, to gradually discharge OUTA and OUTB, thereby performing a soft turn-off of the rectifier MOSFETs. The pull-down current is set by the R_{PD} resistor, and is given by the formula $I_{PULL\text{-}DOWN} = 500\ V/R_{PD}$. Such an event also causes bypass capacitor at the the V_{REF} pin to be discharged, preparing the IC for a voltage-loop soft-start should the primary resume sending timing signals. Further details are given in the Applications Information section.

Synchronous Rectifier Phase-In

With a resistor connected between the R_{DEL} pin and ground, the SiP11203/SiP11204 will increase the low-to-high propagation delay time from INA and INB to OUTA and OUTB by an amount ΔT_{DEL}. This interval is proportional to the resistance used, and inversely proportional to the voltage on V_{REF} ($\Delta T_{DEL} = k \times R_{DEL}/V_{REF}$). As this delay occurs for high-going input transitions only, it constitutes a hold-off time for the synchronous rectifiers. As can be seen, ΔT_{DEL} decreases as V_{REF} ramps from a low level to its final 1.225 V level at start-up, or following any soft-start event. If ΔT_{DEL} is set to start at a sufficient value to allow only diode-mode conduction in the rectifier MOSFETs, the result will be a gentle transition from diode-mode operation to fully synchronous rectification, thereby avoiding a sudden change in the average voltage drop seen at the output rectifiers. Conventional operation can be achieved by tying the R_{DEL} pin to V_L. The synchronous rectifier phase-in function is explained in more detail in the Applications Information section.

Output Over-voltage Protection: SiP11203 versus SiP11204

For maximum flexibility in the way that the SiP11203/SiP11204 parts react to an output over-voltage event, the input to the over-voltage protect comparator (OVP_{IN}) is brought out separately from the error amplifier inputs. Additionally, **the outputs of the SiP11203 and the SiP11204 respond differently to an over-voltage**: the SiP11203 is designed to rapidly discharge an output bus that is experiencing an over-voltage, while the SiP11204 is designed to avoid sinking current from other supplies feeding the same bus, relying instead upon system-level intervention to provide complete load protection. The OVP_{IN} function is explained in more detail in the Applications Information section.

APPLICATIONS INFORMATION

Powering SiP11203/SiP11204

The SiP11203/SiP11204 has an internal pre-regulator to provide 5 V at V_L, which biases many of the internal sub-circuits. This allows the IC to operate from any input voltage within the allowable V_{IN} range. At the same time, V_{IN} provides the supply voltage to the gate driver outputs (OUTA and OUTB) directly. The gate drive level to the synchronous rectifier MOSFETs is determined by V_{IN}

The V_{IN} voltage can be derived using conventional methods, such as an extra winding on the power transformer or on the output inductor. Alternatively, this supply can be derived from the pulse transformer used to transmit synchronous rectifier timing signals from the primary to the secondary, as shown in Figure 2 below. The voltage level on V_{IN} will be determined by the turn ratio of the pulse transformer and the differential voltage between SRL of the Si9122, Si9122A, Si9122E and SRH of of the Si9122, Si9122A, Si9122E. Note that this circuit will cause the voltages at INA and INB to be twice that of V_{IN}. Therefore it may be necessary to limit the voltage seen by INA and INB in order to avoid exceeding their recommended operating values.

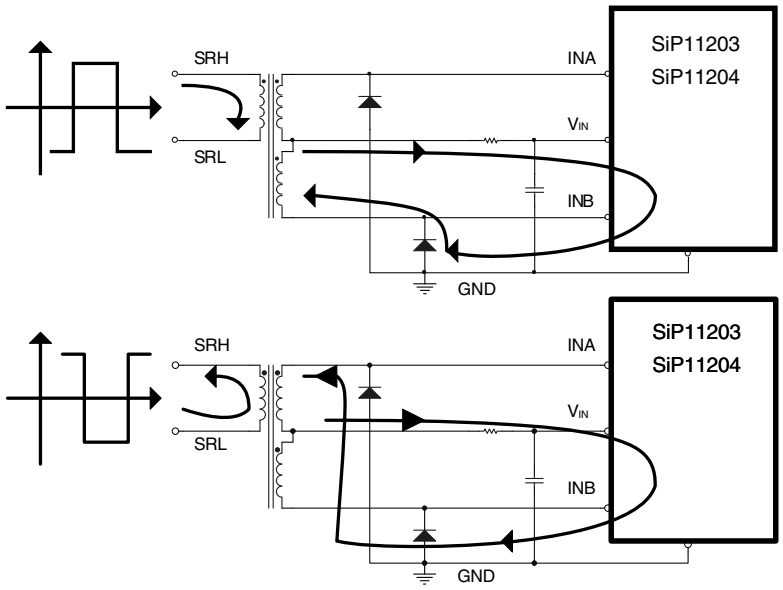


Figure 2. Typical schematic showing how the V_{IN} supply for SiP11203/SiP11204 is generated using the pulse transformer providing the synchronous rectifier timing signals

START-UP DRIVER OPERATION

During start-up of the SiP11203/SiP11204, the MOSFET drivers (OUTA and OUTB) are disabled until V_L is at 90 % of its final value. To fully prevent any spurious turn-on of the synchronous rectifier MOSFETs, the gates of the MOSFETs are held off during this start up period. Until the main drivers are enabled, the INA and INB drive paths are re-routed, or “swapped,” inside the IC. In conjunction with a dedicated n-channel hold-off MOSFET “inverter” placed in parallel with each main driver, this allows the IC to ground the appropriate synchronous rectifier gate at the necessary time. See Figure 3.

If the first two pulses coming through the pulse transformer are considered, the following sequence of events follows:

- INA goes low, which would normally command the OUTA driver to go low. This would prevent spurious turn-on of the associated synchronous rectifier. However, since the voltage to the IC is below its normal operating level, it cannot be guaranteed that OUTA can in fact go to its necessary state. For this reason, the OUTA and OUTB drivers are disabled while $V_L < UVLO_R$.
- When INA goes low, INB will be driven to a level of 2 x V_{IN}. This is due to the way in which the secondary of the pulse transformer is rectified to provide V_{IN}. Specifically, this results from the rectifier diodes clamping the secondary’s negative excursions one diode drop below ground (See Figure 2).

- While V_L is below the $UVLO_R$ threshold, the IC "swaps" the synchronous rectifier drive paths. This causes the high-going signal on INB to be applied to the gate of an n-channel hold-off MOSFET, which is in parallel with the main OUTA driver. This MOSFET inverts the signal from INB, which causes its drain to be pulled towards ground. This holds OUTA low.
- During the deadtime in which neither INB nor INA is driven high, the voltage on INA and that on INB will be equal to the voltage on V_{IN}. Depending upon the exact value of V_{IN}, this may or may not result in both OUTA and OUTB being pulled low by their associated inverter MOSFETs.
- During the next cycle of converter operation, all of the above applies with the exception that INB is now driven low, which will cause INA to be driven high. This will in turn cause the hold-off MOSFET in parallel with the main OUTB driver to conduct, thereby holding OUTB low.

In this way, the SiP11203/SiP11204 "swap and invert" function prevents any unwanted turn-on of the synchronous rectifiers during start-up. Once V_L reaches 90 % of its final value, the drive path inside the IC is no longer swapped, and the inverting hold-off MOSFETs are disabled.

FUNCTIONAL BLOCK DIAGRAM

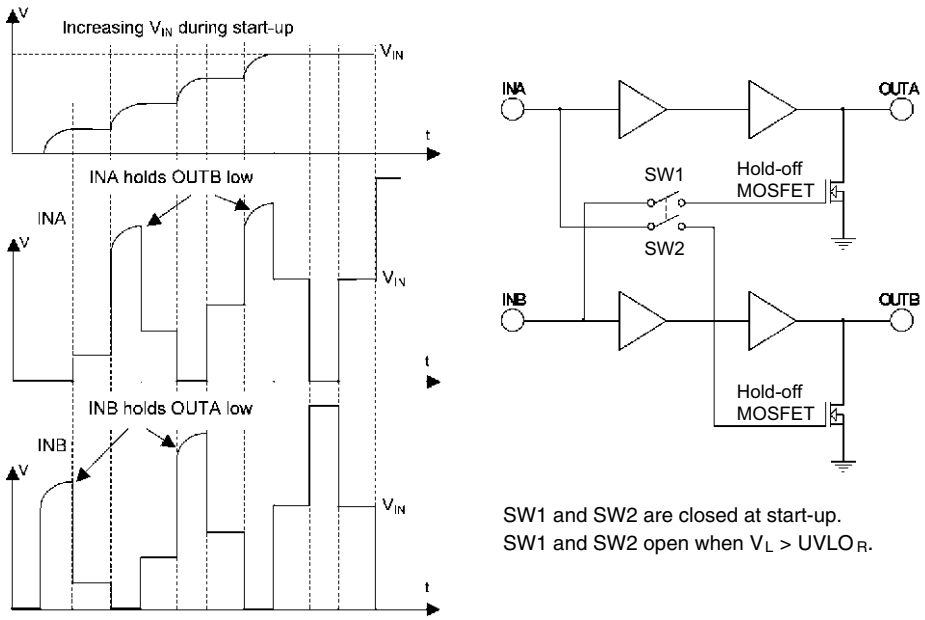


Figure 3. During converter startup, the synchronous MOSFET gate-driver outputs of the SiP11203/SiP11204 are reversed and inverted to prevent spurious MOSFET switching

START-UP DRIVER OPERATION

Assuming that V_{IN} rises with suitable rapidity to a voltage greater than 5.5 V, the factors controlling the rate of rise of V_L are the external V_L bypass capacitor value and the pre-regulator's current limit. This gives the following two equations:

- The time from start-up to $CUVLO_R \cong (4.45\ V/35\ mA) \times C_{VL}$, and
- The time from start-up to $UVLO_R \cong (4.45\ V/35\ mA) \times C_{VL}$.

Once V_L has reached 90 % of its final value, the clamp holding V_{REF} at 0 V is released, allowing the voltage on the V_{REF} pin to rise at a rate set by the value of the V_{REF} capacitor. This gives the following equation:

- The time from $UVLO_R$ to V_{REF} attaining a voltage of $1.1\ V \cong (1.1\ V/410\ \mu A) \times C_{VREF}$.

These relationships are shown in Figure 4.

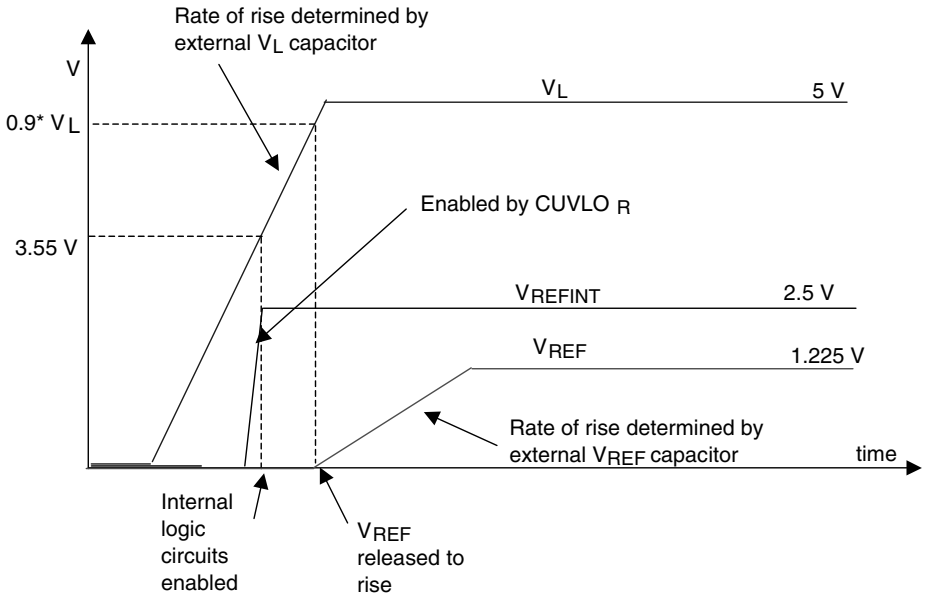


Figure 4. Soft-start parameters of the SiP11203/SiP11204 are programmable with external components

NORMAL DRIVER OPERATION

In normal operation, OUTA responds to INA, and OUTB to INB. The signal path from input to output is **non-inverting**. The output drivers have high and deliberately asymmetrical current sink and source capabilities (4 A I_{SINK}, 2.2 A I_{SOURCE}). The high currents allow driving large synchronous rectifiers at the switching frequencies found in modern power converters. At the same time, the driver asymmetry enforces a rapid turn-off of the rectifier MOSFETs relative to their turn-on, to avoid rectifier crossconduction, and the low driver impedances to PGND help ensure that the rectifier MOSFETs do not exhibit unwanted turn-on during converter operation.

As with most logic circuits, OUTA and OUTB do not exhibit indeterminate output states even the transitions at INA and INB are excessively slow. The solid and sharp driving signals from OUTA and OUTB will ensure the proper function of the rectifier MOSFETs in the final application circuit.

POWER-DOWN DRIVER OPERATION

If the timing pulses from the primary of the DC-DC converter cease, the SiP11203/SiP11204 must assume that the power to the primary of the DC-DC converter has failed. Upon detecting this condition, the part must put the main synchronous rectifier drivers into a “safe” condition, and simultaneously ensure that the rectifier MOSFETs are turned off. A unique feature of the SiP11203/SiP11204 is their ability to turn off the synchronous rectifiers via a controlled excursion through their linear region. This can help to prevent output ringing at turn-off.

A missing-pulses detector is provided on the IC to initiate the soft power down. This detector, which is enabled once the V_{REF} pin has reached 1.1 V, continually monitors INA and INB for lack of switching activity. An external resistor from R_{PD} to ground defines a current out of C_{PD} ($I = 2.5\ V/R_{PD}$), which is used to charge an external capacitor from C_{PD} to ground. The voltage on C_{PD} is internally compared to the 2.5 V developed by V_{REFINT}. Whenever either input goes low, the voltage at C_{PD} is reset to 0 V. However, if both inputs are high for a period of $R_{PD} \times C_{PD}$, the voltage at C_{PD} will exceed the 2.5 V comparison threshold, and the power-down latch will be set (See Figure 6).

- The V_{REF} pin bypass capacitor is discharged towards 0 V, to ensure an orderly soft-start cycle when operation resumes,
- The main drivers are forced into a high-impedance state,
- Internal pull-downs (current sinks) from the OUTA and OUTB pins to ground are enabled,
- The pull-down currents on OUTA and OUTB are set by R_{PD}, to allow a “soft” turn-off of the synchronous rectifiers.

POWER-DOWN DRIVER OPERATION (CONT'D)

The internal pull-downs ensure that the synchronous rectifiers are in the off state before the bias supply to the IC has collapsed (See Figure 5). Since these pull-downs have a lower current-sinking capability than the main OUTA and OUTB drivers, they can cause the rectifier MOSFETs to transition from full conduction to the off state via their linear region of operation. This soft turn-off allows the use of the gradually increasing rectifier channel impedances to help damp LC oscillations that might otherwise occur at the converter's output. The gate pull-down current value, and therefore the interval during which the rectifier MOSFETs are in transition from fully on to fully off, is programmed by the resistor from RPD to ground. This current is given by $I_{PULL\text{-}DOWN} = 200^* V_{REFINT}/R_{PD}$. This programmability allows the choice of a gate discharge time which best accommodates the design variables of L_{OUT}, C_{OUT}, and synchronous rectifier MOSFET characteristics.

The power-down latch will be reset, and a soft-start cycle will occur, when the logical and of two conditions is true:

- The voltage on the V_{REF} capacitor is 20 % (245 mV) of its nominal 1.225 V, and
- The exclusive-or of INA and INB is true, that is, one input is in low while the other is high.

Note that low values of R_{PD} will increase the main supply current. It is recommended that R_{PD} be kept ≥ 15 kΩ to prevent excessive power dissipation.

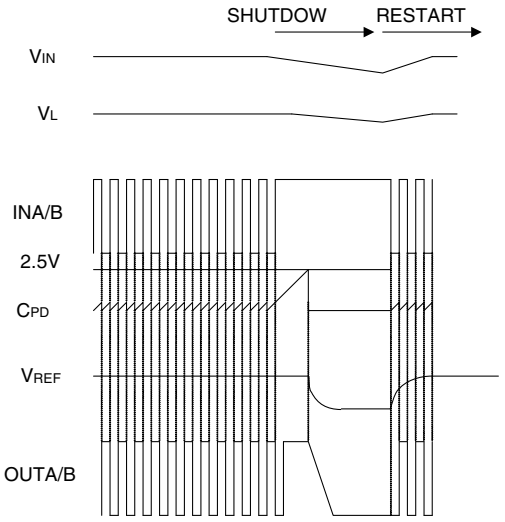


Figure 5. The shutdown sequence of SiP11203/SiP11204 prevents the synchronous MOSFET of a half-bridge converter from discharging a prebiased output when supplied power is removed

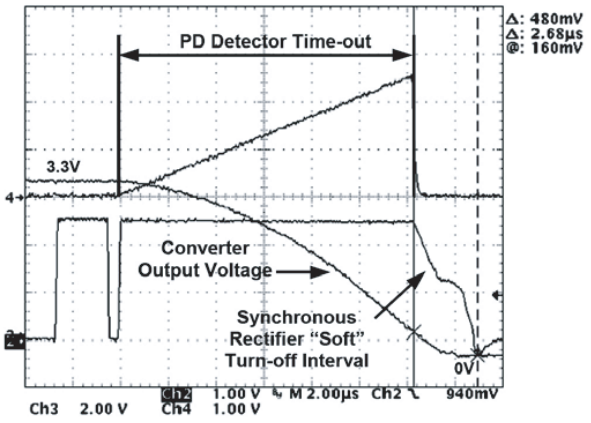


Figure 6. Power Down Detect and "Soft" Turn-Off

SYNCHRONOUS RECTIFIER PHASE-IN AND RISING EDGE DELAY

The SiP11203/SiP11204 has the ability to "phase in" the synchronous rectifiers at start-up. This causes the rectifier MOSFETs to initially be used as conventional PN (or Schottky) diodes, then as synchronous rectifiers for an increasing percentage of each switching cycle, until finally they are operating completely as synchronous switches. When this feature of the IC is used, the resistance R_{DEL}, which is connected between the R_{DEL} pin and ground, determines the time required for the transition from diode-mode operation to fully synchronous rectification.

To achieve this phase-in of the synchronous rectifiers, an internally extended propagation delay (ΔT_{DEL}) is introduced between the rising edge of each input (INA or INB) and the rising edge of the corresponding output (OUTA or OUTB). The length of this delay is proportional to R_{DEL} and inversely proportional to V_{REF}: $\Delta T_{DEL} \cong (1.5\text{ ns} \times R_{DEL} \times 1.225\text{ V})/(1\text{ k}\Omega \times V_{REF})$. Therefore ΔT_{DEL} decreases throughout the interval during which V_{REF} is rising (i.e., during the time following converter start-up or a SiP11203/SiP11204 soft-start event). When the phase-in period has ended, the final high-going propagation delay is $T_{DEL(FINAL)} = T_{pdr} + T_{DEL(FINAL)} = T_{pdr} + [(1.5\text{ ns} \times R_{DEL})/1\text{ k}\Omega)]$, as shown in the typical curves.

SYNCHRONOUS RECTIFIER PHASE-IN AND RISING EDGE DELAY (CONT'D)

The three modes of operation experienced during synchronous rectifier phase-in are, in order:

- Some number of converter switching cycles may occur during which $\Delta T_{DEL} \geq 2/f_{CONVERTER}$. During this interval, the synchronous rectifiers are held off for a long enough time that they will act as conven ional diodes only. This interval of operation will be some portion of the time it takes for the voltage on the V_{REF} pin to climb to its final 1.225 V value.
- Some number of converter switching cycles will occur during which $2/f_{CONVERTER} > \Delta T_{DEL} > \Delta T_{DEL(FINAL)}$. During this interval, the synchronous rectifiers are held off for a portion of their possible conduction interval, with that percentage decreasing in a 1/x fashion from 100 % of their possible conduction time to a percentage set by R_{DEL} and $f_{CONVERTER}$. This interval of operation will be the remainder of the time it takes for the voltage on the V_{REF} pin to climb to its final 1.225 V value.
- When V_{REF} is equal to 1.225 V, normal converter operation occurs, with the synchronous rectifiers being held off for a time $T_{DEL(FINAL)}$. This final delay time can be made equal to the inherent propagation delay of the IC's output drivers, as described below.

The synchronous rectifier phase-in is diagrammed in Figure 7.

Connecting R_{DEL} to V_L will completely disable the synchronous rectifier phase-in circuitry. The rectifier MOSFETs will then transition directly from diode-mode full synchronous rectifier operation when the IC's V_L supply exceeds the $UVLO_R$ threshold. The residual rising-edge delay otherwise introduced by R_{DEL} will also be set to zero. (Note: By examination of the above equations, grounding the R_{DEL} pin could be another means of setting ΔT_{DEL} to zero. Doing so is not recommended in practice as this will cause unnecessary power dissipation in the IC: the supply current will increase by 0.15 mA if R_{DEL} is connected to V_L, but by 0.5 mA if this pin is shorted to ground. Also, due to the internal circuitry of the ICs, the propagation delay time is reduced by several nanoseconds when the R_{DEL} pin is connected to V_L as opposed to when it is grounded.)

In some applications it is desirable to make use of the rectifier phase-in feature while eliminating the residual ΔT_{DEL}. To achieve this, the appropriate resistance should be connected from the R_{DEL} pin to ground, and the R_{DEL} pin should be pulled up to V_L using a suitable op-amp or comparator, such as the LMV321M7, once the output voltage of the converter approaches its final value. In such a circuit, V_{CC} for the op-amp or comparator should be obtained from V_L of the SiP11203/SiP11204.

The phase-in of synchronous rectification helps to prevent disturbances in the output voltage at start-up, which could occur due to the differential in output voltage drop which occurs when the rectifier MOSFETs make an abrupt transition from operation as diodes to operation as synchronous rectifiers.

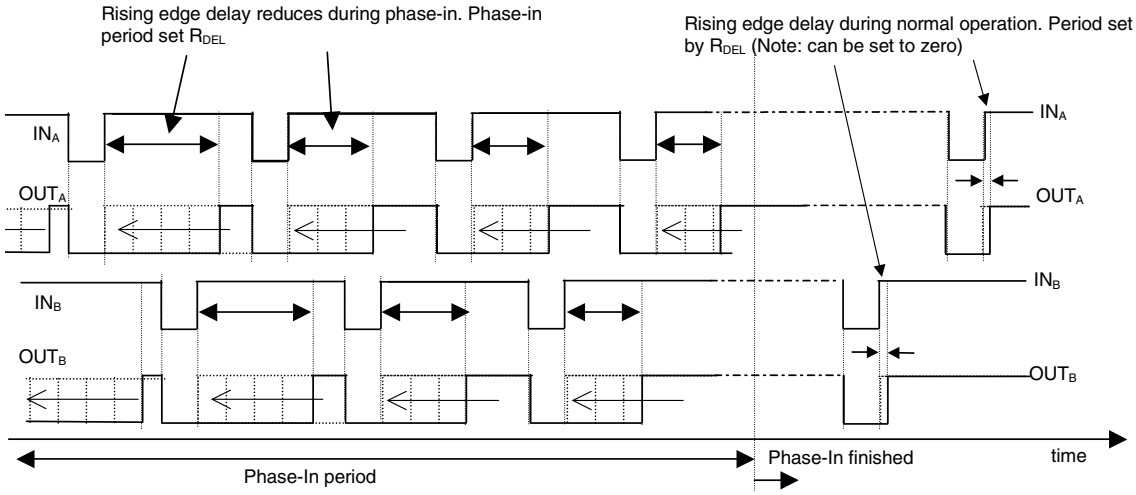


Figure 7. The SiP11203/SiP11204 gate-drive output signals are delayed during phase-in prevent disturbing the output voltage

The Figure 8 below shows how the rising edge delay is implemented in conjunction with the Si9122 and allows the effective BBM2 and BBM4 falling delays to be modified independently of rising delays BBM1 and BBM3. For definition of the BBM delays please see the Si9122 datasheet.

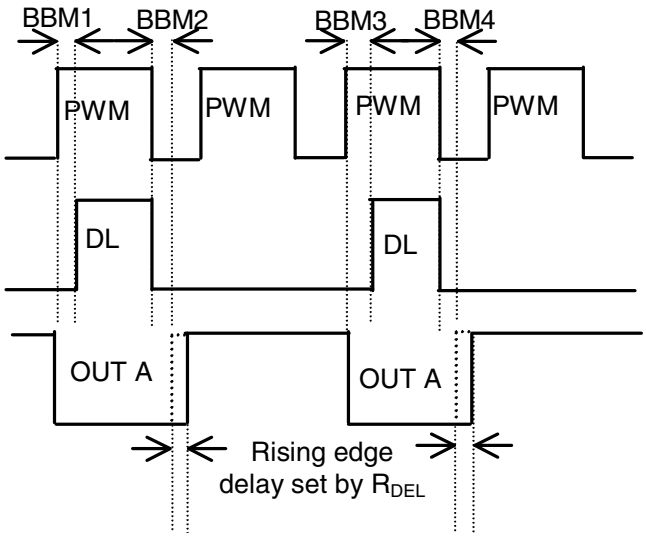


Figure 8. The delay of SiP11203 and SiP11204 gate-drive output signals compensate the break-before-make switching action discrepancies arising from propagation delays

OUTPUT OVER-VOLTAGE PROTECTION

The SiP11203/SiP11204 provide output over-voltage protection (OVP) by means of a dedicated internal comparator. One input of the OVP comparator is brought out to the OVP_{IN} pin, and the other is returned to an internal reference voltage that is fixed at 120 % of the 1.225 V V_{REF} value, or 1.47 V. A voltage in excess of 1.47 V at the OVP_{IN} pin indicates an OVP fault.

The OVP circuitry operates in two different ways, depending upon whether the SiP11203/SiP11204 is in start-up mode, or in normal operation. In this context, start-up mode is defined as device operation during that period for which V_{REF} is less than 90 % of its 1.225 V value, or 1.1 V.

Start-Up Mode:

If the 1.47 V OVP threshold is exceeded during start-up, the driver outputs OUTA and OUTB are held low until the voltage on the V_{REF} pin has exceeded 1.1 V. The driver outputs are then released to respond to INA and INB.

Normal Operation Mode:

If the OVP threshold is exceeded, or remains exceeded, after V_{REF} has reached 1.1 V, the OVP latch will be set. This will cause the driver outputs to be forced high for SiP11203, or forced low for SiP11204. At the same time, an on-chip transistor will discharge the bypass capacitor at the V_{REF} pin towards ground. The OVP latch is reset when the logical and of two conditions:

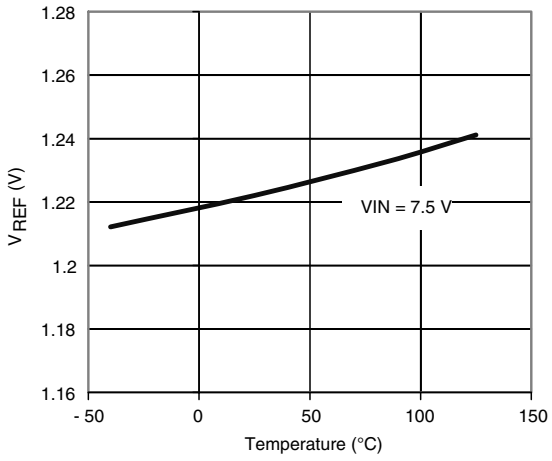
- The voltage on the V_{REF} pin must be ≤ 20 % (245 mV) of its nominal 1.225 V level, to ensure an orderly soft-start cycle when operation resumes, and
- The voltage at the OVP_{IN} pin must be 1.1 V, indicating that the OVP fault has been cleared.

When the OVP latch is reset, the SiP11203/SiP11204 will release their outputs, and return to normal operation via a soft-start cycle.

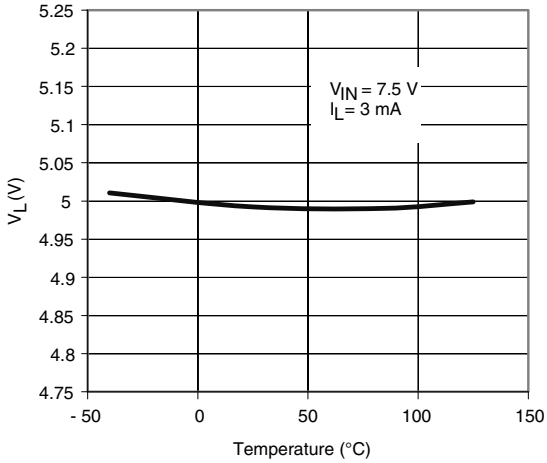
To prevent spurious activation of the over-voltage function, the over-voltage condition must be present for five switching instances, where a switching instance is defined as activity on either IN_A or IN_B. On the fifth switching instance the overvoltage condition is latched. If the over voltage condition disappears the IC will not recognize an over-voltage as being present and the counter will be reset to zero.

Note that the OVP_{IN} threshold voltage is derived from the internal 2.5 V reference voltage V_{REFINT}, which is derived from V_{IN}, and therefore is not delayed by the rise time of either V_L or V_{REF}.

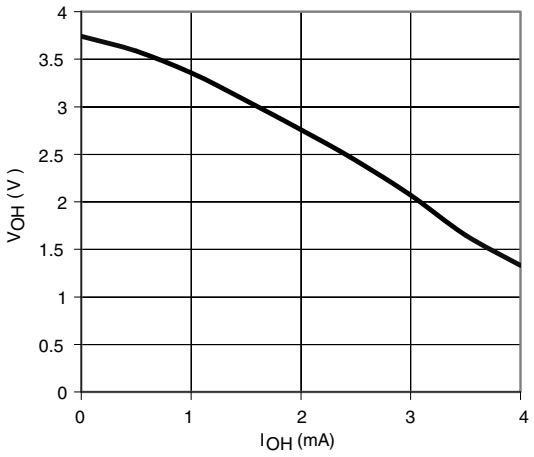
TYPICAL CHARACTERISTICS



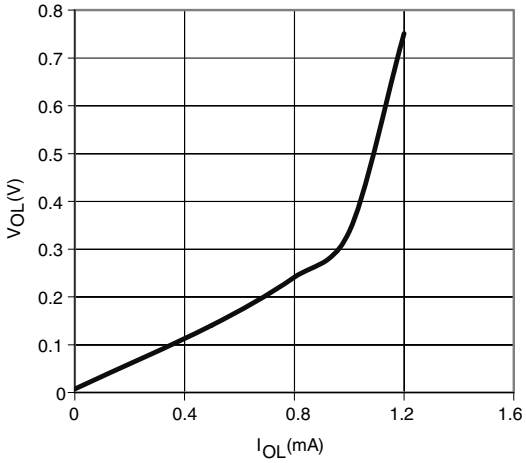
V_{REF} vs. Temperature



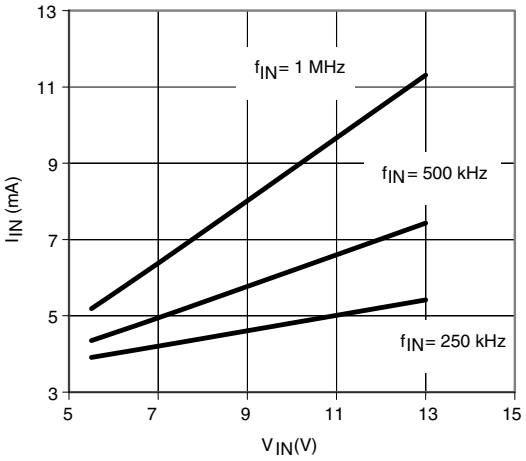
V_L vs. Temperature



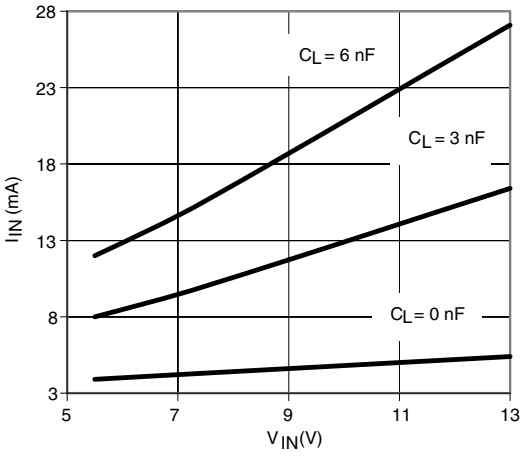
Error Amp V_{OH} vs. I_{OH}



Error Amp V_{OL} vs. I_{OL}

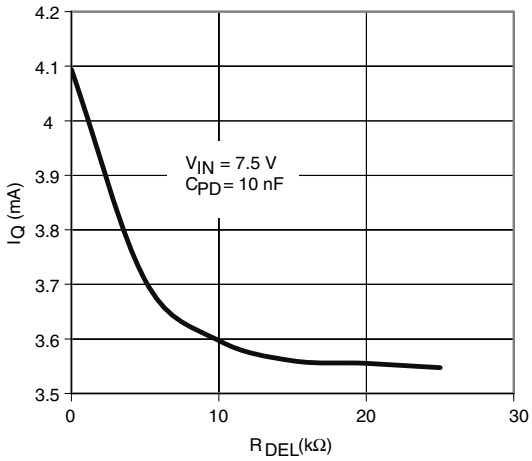


Supply Current Without Load vs. V_{IN}

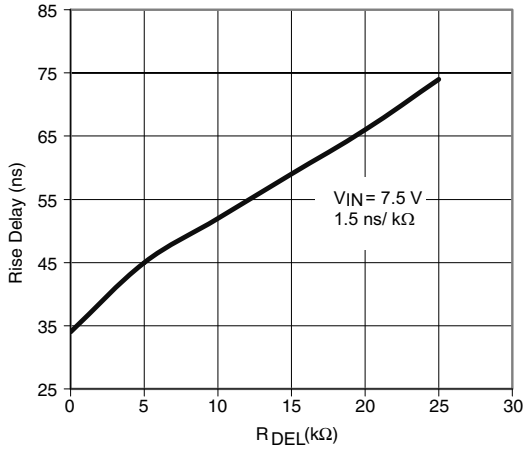


250 kHz Supply Current vs. C_L

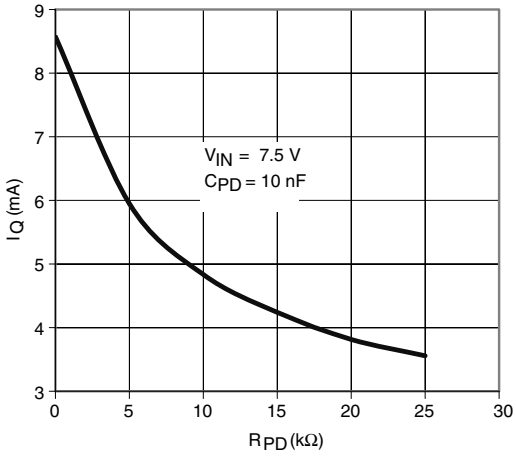
TYPICAL CHARACTERISTICS



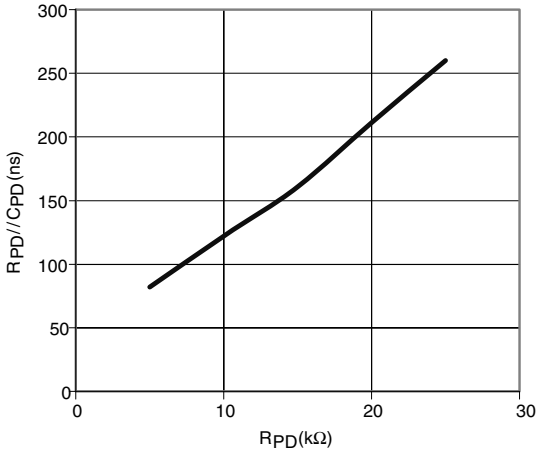
Quiescent Current vs. R_{DEL}



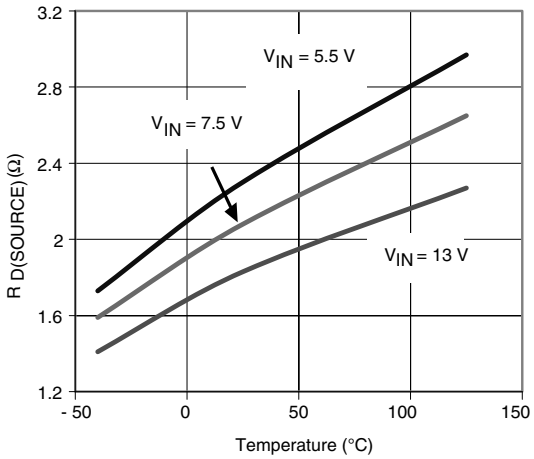
Rise Delay vs. R_{DEL}



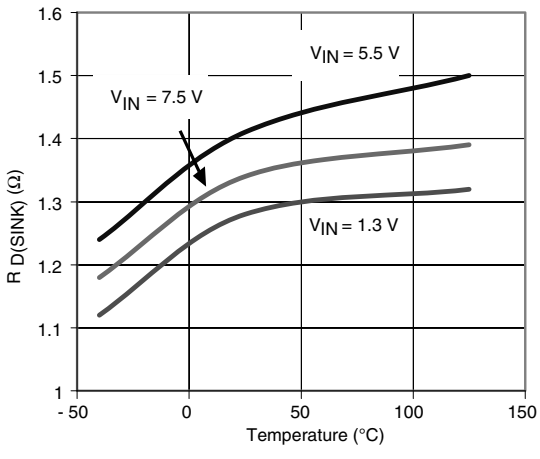
Quiescent Current vs. R_{PD}



Powerdown Timeout vs. R_{PD}



$R_{D(SOURCE)}$ vs. Temperature



$R_{D(SINK)}$ vs. Temperature

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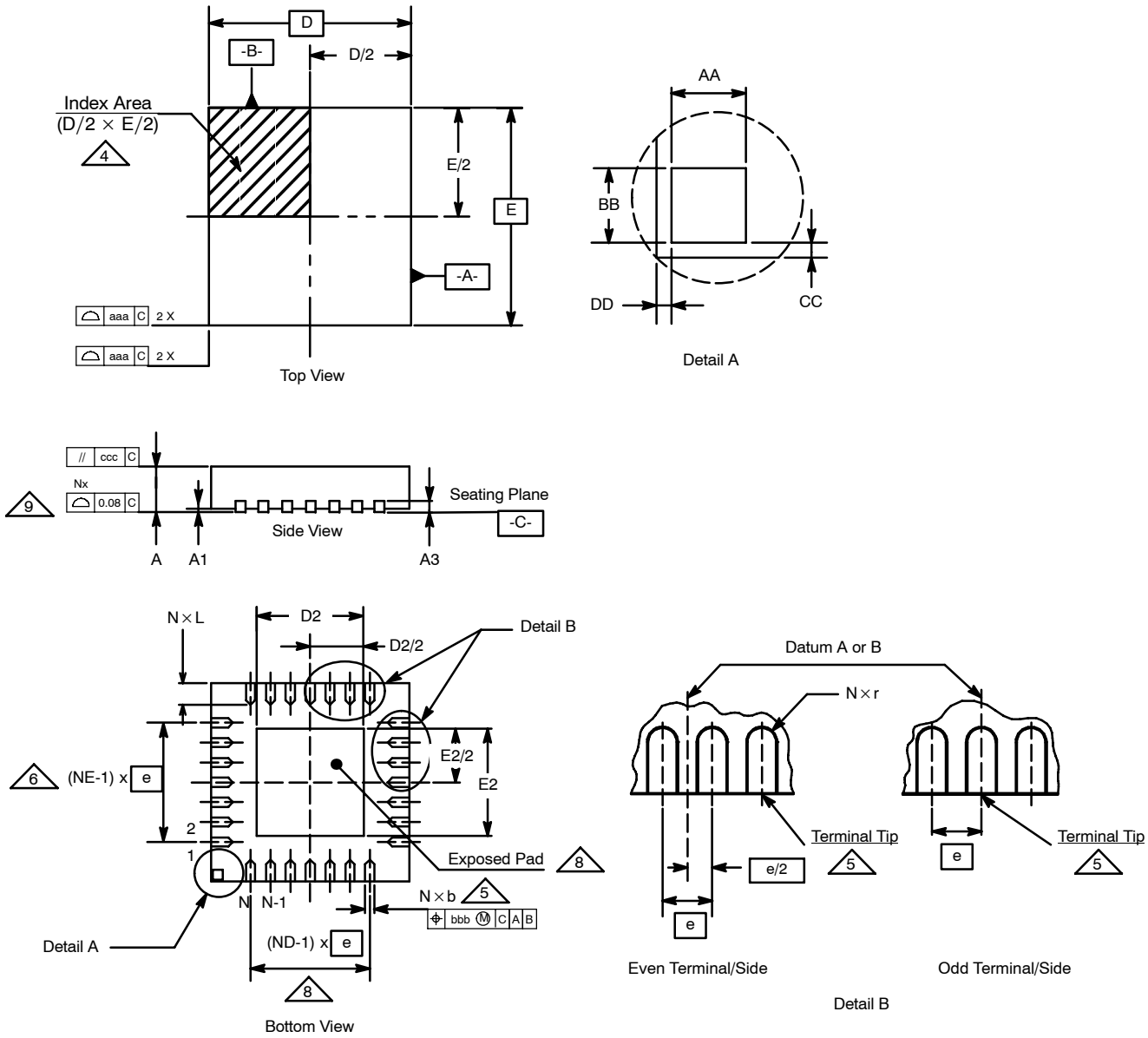
PowerPAK® MLP44-16 (POWER IC ONLY)

JEDEC Part Number: MO-220



PowerPAK® MLP44-16 (Power IC Only)

JEDEC Part Number: MO-220

Dim	MILLIMETERS*			INCHES			Notes
	Min	Nom	Max	Min	Nom	Max	
A	0.80	0.90	1.00	0.0315	0.0354	0.0394	
A1	0	0.02	0.05	0	0.0008	0.0020	
A3	–	0.20 Ref	–	–	0.0079	–	
AA	–	0.345	–	–	0.0136	–	
aaa	–	0.15	–	–	0.0059	–	
BB	–	0.345	–	–	0.0136	–	
b	0.25	0.30	0.35	0.0098	0.0118	0.138	5
bbb	–	0.10	–	–	0.0039	–	
CC	–	0.18	–	–	0.0071	–	
ccc	–	0.10	–	–	0.0039	–	
D		4.00 BSC			0.1575 BSC		
D2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
DD	–	0.18	–	–	0.0071	–	
E		4.00 BSC			0.1575 BSC		
E2	2.55	2.7	2.8	0.1004	0.1063	0.1102	
e		0.65 BSC			0.0256 BSC		
L	0.3	0.4	0.5	0.0118	0.0157	0.0197	
N		16			16		3, 7
ND	–	4	–	–	4	–	6
NE	–	4	–	–	4	–	6
r	b(min)/2	–	–	b(min)/2	–	–	

* Use millimeters as the primary measurement.

ECN: S-50794—Rev. B, 16-May-05
DWG: 5905

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angels are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a molded or marked feature. The X and Y dimension will vary according to lead counts.
5. Dimension b applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip.
6. ND and NE refer to the number of terminals on the D and E side respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Variation HHD is shown for illustration only.
9. Coplanarity applies to the exposed heat sink slug as well as the terminals.

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