



GaAs pHEMT MMIC 2 WATT POWER AMPLIFIER, 15 - 20 GHz

Typical Applications

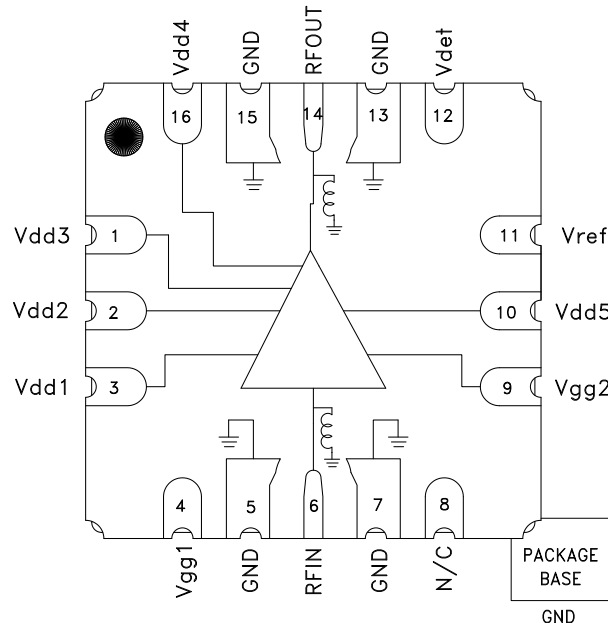
The HMC6981LS6 is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- SATCOM

Features

- P1dB Output Power: +32 dBm
- 25% PAE @ +34 dBm Pout
- Gain: 26 dB
- Output IP3: +43 dBm
- 50 Ohm Matched Input/Output
- Ceramic 6 x 6 mm High Frequency Air Cavity Package

Functional Diagram



General Description

The HMC6981LS6 is a four-stage GaAs pHEMT MMIC Power Amplifier with an integrated temperature compensated on-chip Power Detector, which operates between 15 and 20 GHz. The amplifier provides 26 dB of gain, +34 dBm of saturated output power, and 25% PAE from a +5.5V supply. With an excellent output IP3 of +43 dBm, the HMC6981LS6 is ideal for linear applications such as high capacity point-to-point or point-to-multi-point radios or SATCOM applications demanding +34 dBm of efficient saturated output power. The HMC6981LS6 is housed in a ceramic 6 x 6 mm high frequency air cavity package which exhibits low thermal resistance and is compatible with high volume surface mount manufacturing techniques. The RF I/Os are internally matched to 50 Ohms.

Electrical Specifications, $T_A = +25^\circ\text{C}$

$V_{dd} = V_{dd1}, V_{dd2}, V_{dd3}, V_{dd4}, V_{dd5} = +5.5\text{V}, I_{dd} = 1100\text{ mA}$ [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range	15 - 17		17 - 20				GHz
Gain	24	27		23	26		dB
Gain Variation Over Temperature	0.042		0.038				dB/ °C
Input Return Loss	9		13				dB
Output Return Loss	13		15				dB
Output Power for 1 dB Compression (P1dB)	30	32		30.5	32.5		dBm
Saturated Output Power (P _{sat})	34		34				dBm
Output Third Order Intercept (IP3) ^[2]	42		43				dBm
Total Supply Current (I _{dd})	1100		1100				mA

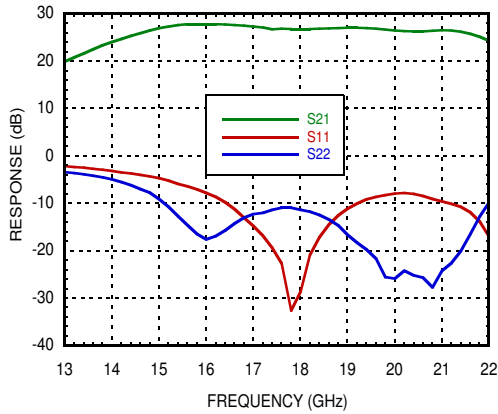
[1] Adjust V_{gg} between -2 to 0V to achieve I_{dd} = 1100 mA typical.

[2] Measurement taken at +5.5V @ 1100 mA, P_{out} / Tone = +20 dBm

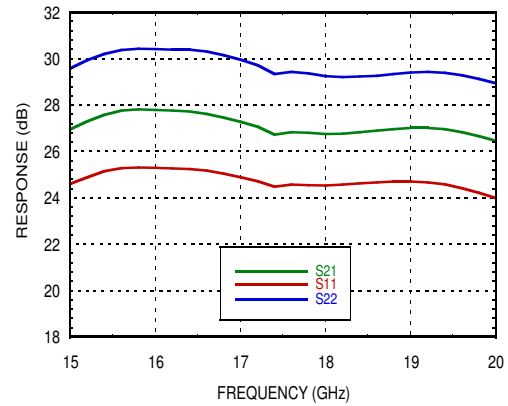


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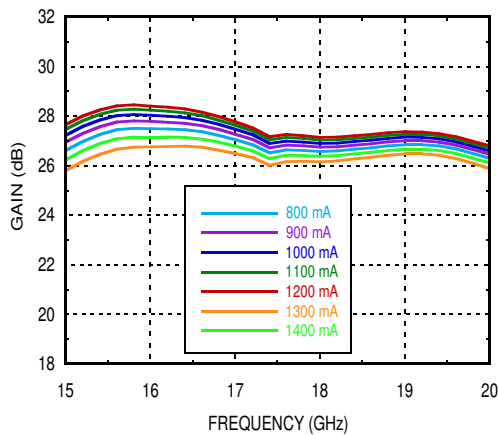
Gain & Return Loss



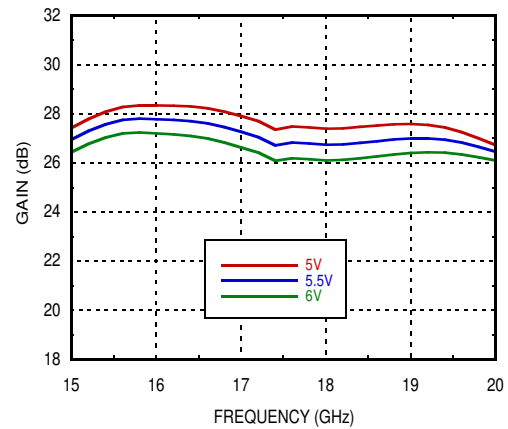
Gain vs. Temperature



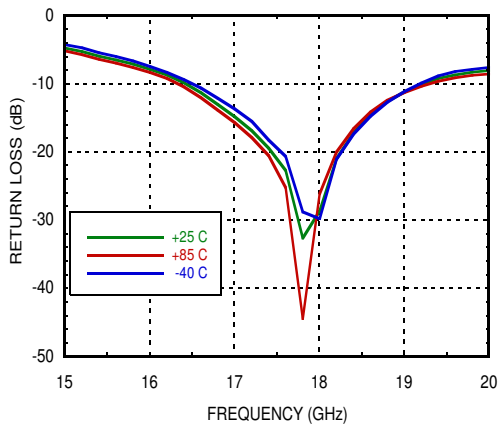
Gain vs. Supply Current



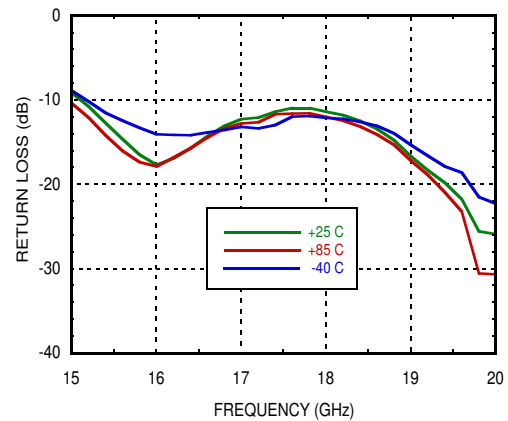
Gain vs. Supply Voltage



Input Return Loss vs. Temperature



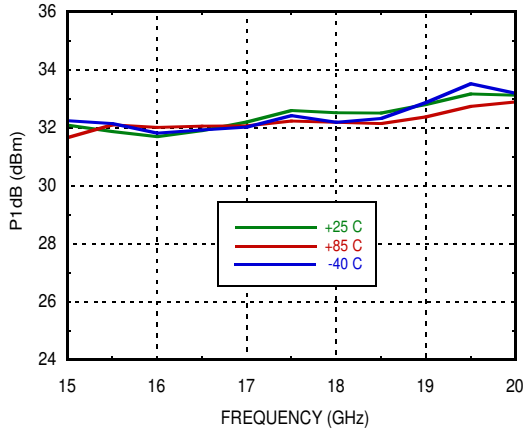
Output Return Loss vs. Temperature



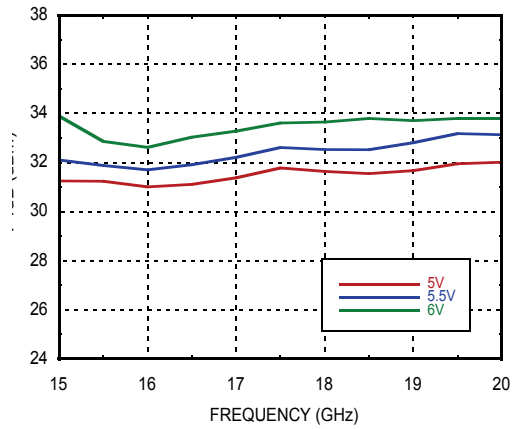


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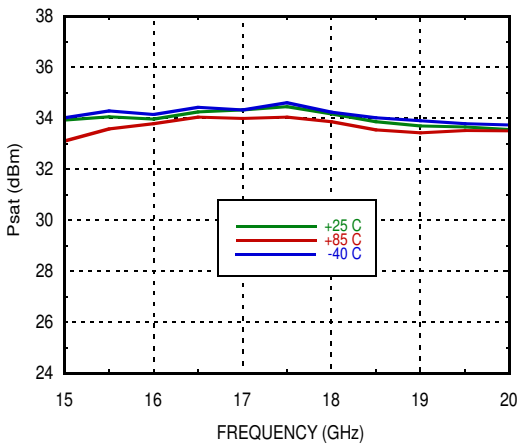
P1dB vs. Temperature



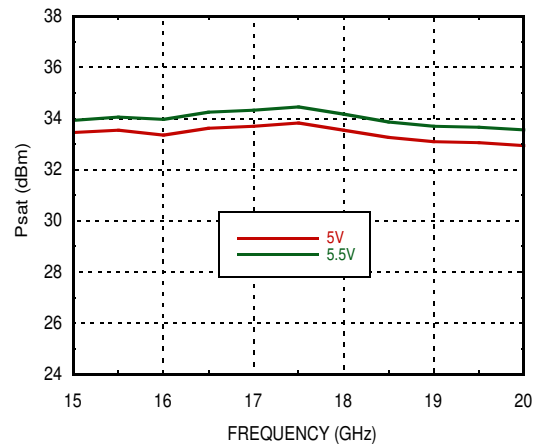
P1dB vs. Supply Voltage



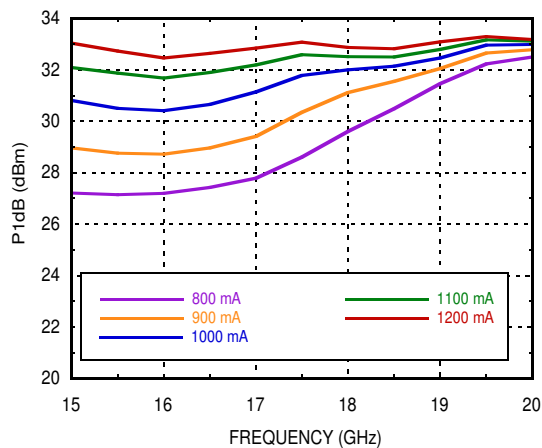
Psat vs. Temperature



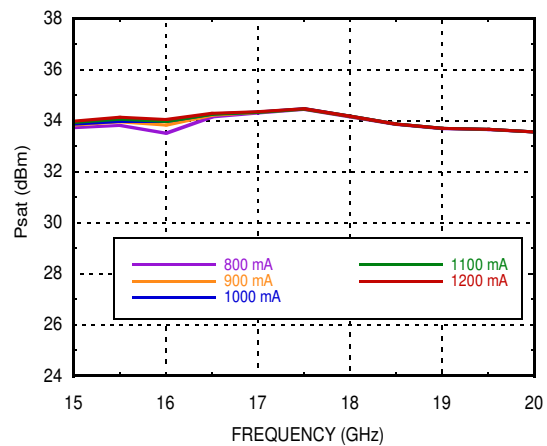
Psat vs. Supply Voltage



P1dB vs. Supply Current



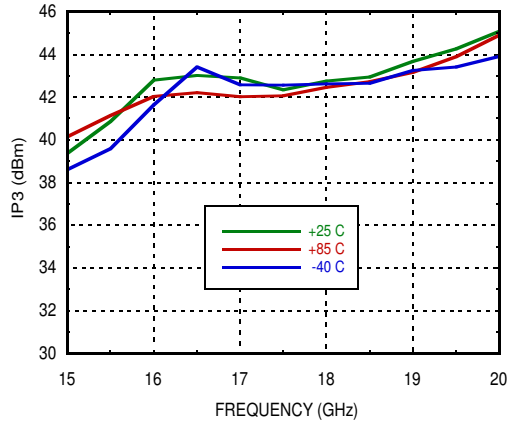
Psat vs. Supply Current



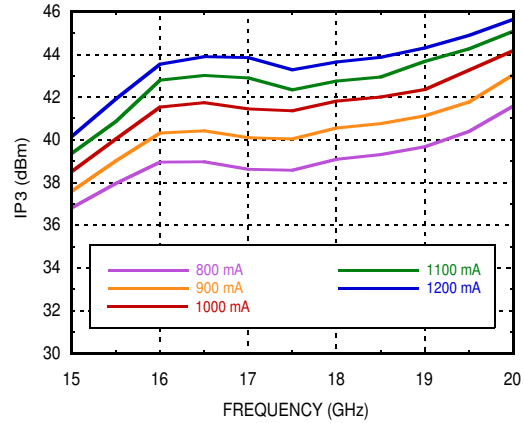


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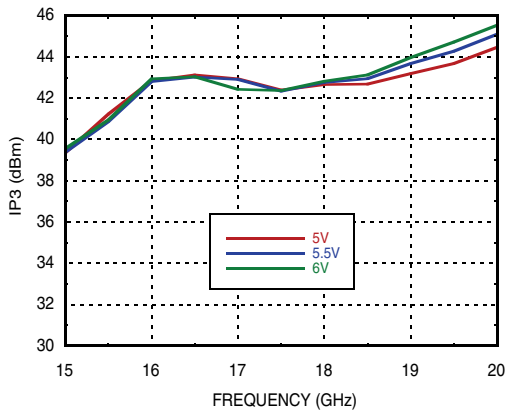
**Output IP3 vs. Temperature,
Pout/tone = +20 dBm**



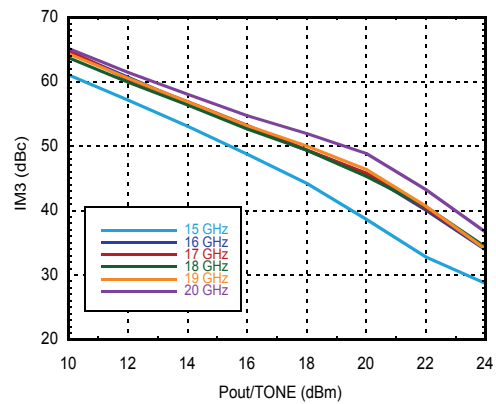
**Output IP3 vs. Supply Current,
Pout/tone = +20 dBm**



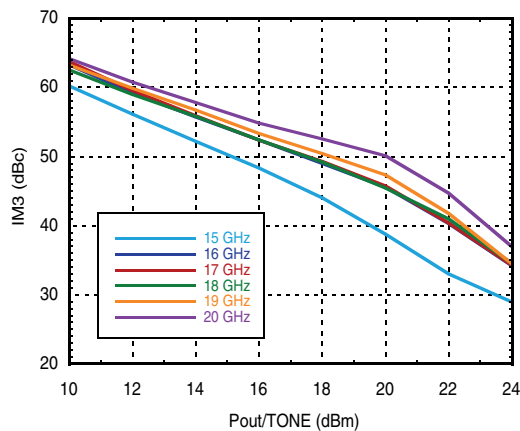
**Output IP3 vs. Supply Voltage,
Pout/tone = +20 dBm**



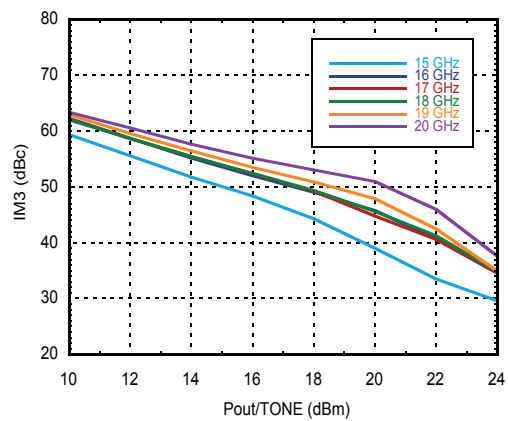
Output IM3 @ Vdd = +5V



Output IM3 @ Vdd = +5.5V



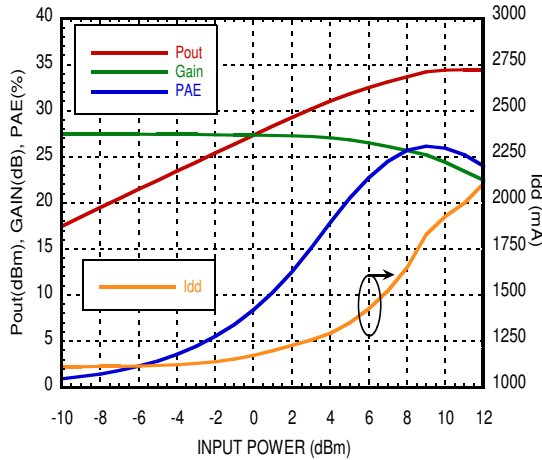
Output IM3 @ Vdd = +6V



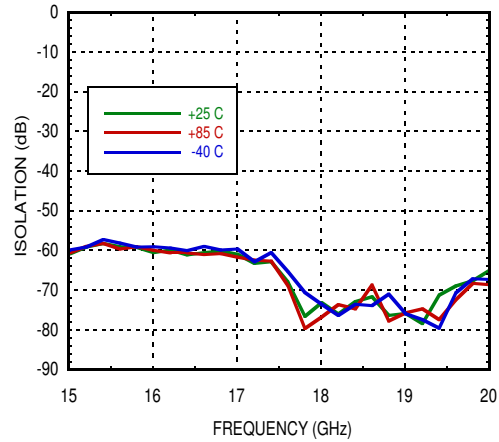


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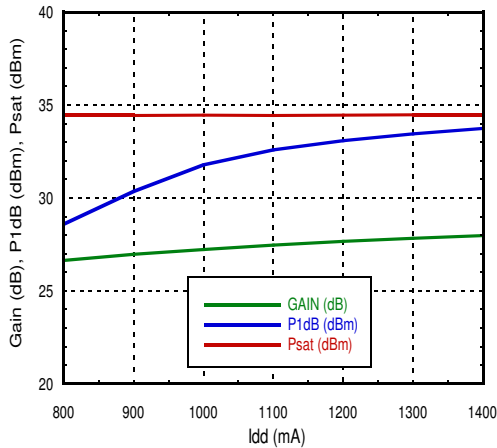
Power Compression @ 17.5 GHz



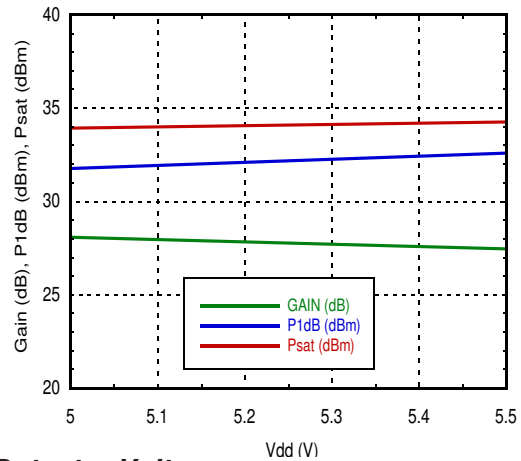
Reverse Isolation vs. Temperature



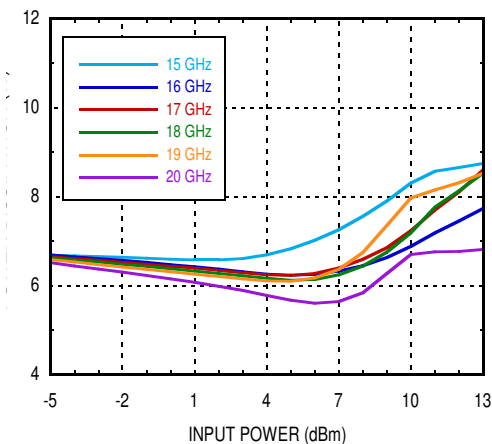
Gain & Power vs. Supply Current @ 17.5 GHz



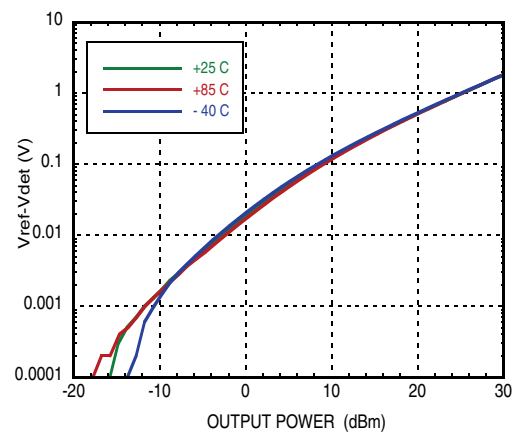
Gain & Power vs. Supply Voltage @ 17.5 GHz



Power Dissipation



Detector Voltage vs. Temperature @ 17.5 GHz

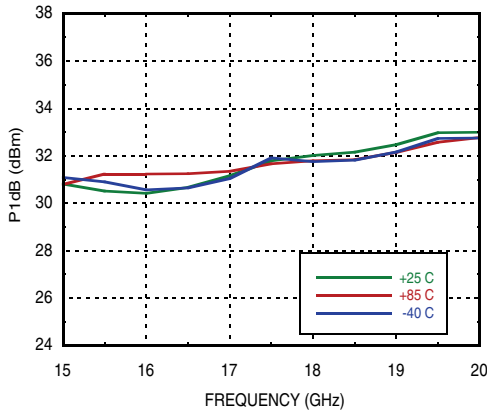




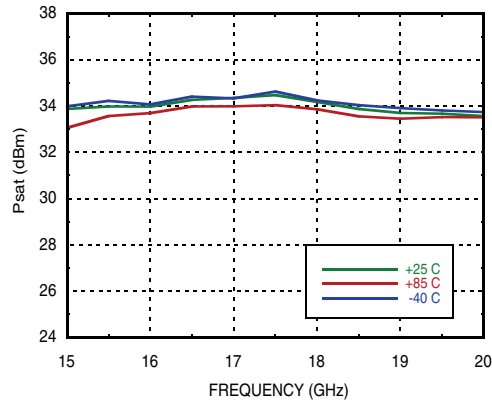
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Low DC Power Mode, Vdd = 5.5V, Idd = 1000 mA

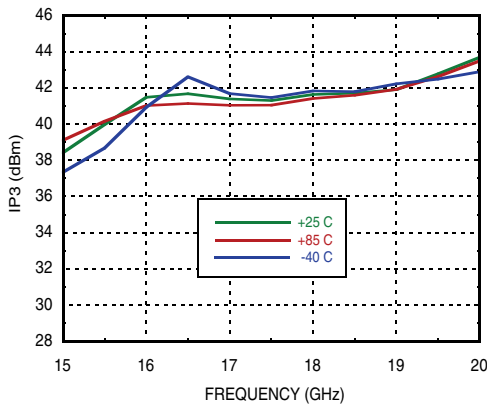
P1dB vs. Temperature



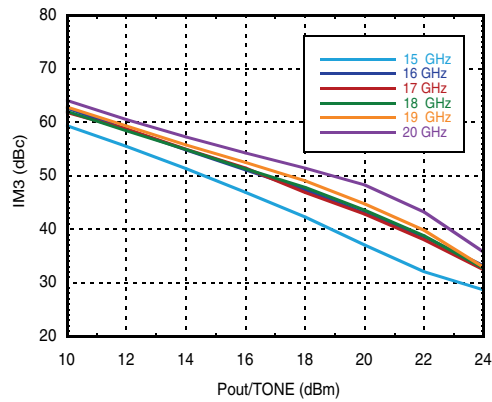
Psat vs. Temperature



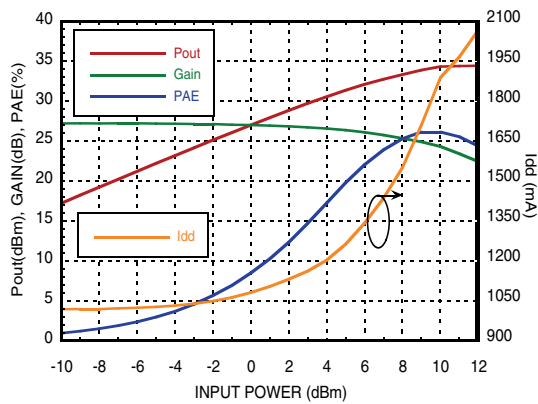
**Output IP3 vs. Temperature,
Pout/tone = +20 dBm**



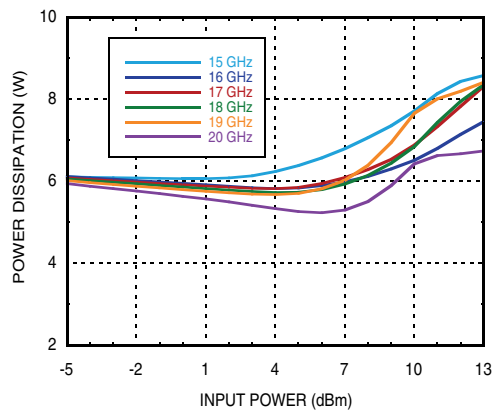
Output IM3 @ Vdd = +5.5V, 1000 mA



Power Compression @ 17.5 GHz



Power Dissipation



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Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+6.5 Vdc
Gate Bias Voltage (Vgg)	-3 to 0 Vdc
RF Input Power (RFIN)	+18 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 129 mW/°C above 85 °C)	11.7 W
Thermal Resistance (channel to ground paddle)	7.7 °C/W
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 0, Passed 150V

Typical Supply Current vs. Vdd

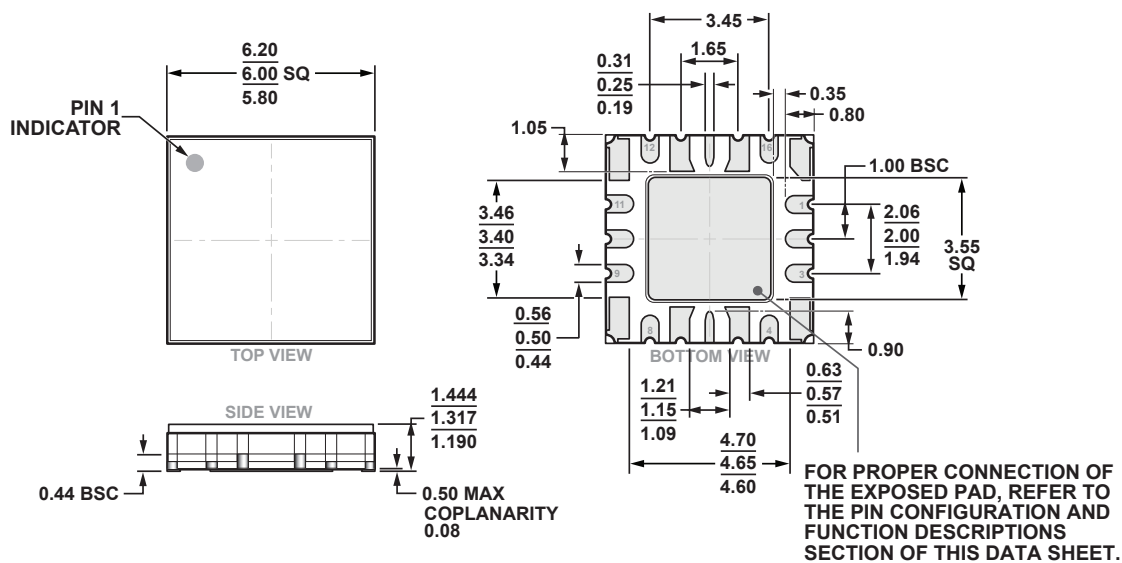
Vdd (V)	Idd (mA)
+5	1100
+5.5	1100
+6	1100

Adjust Vgg to achieve Idd = 1100 mA



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**

Outline Drawing



16-Terminal Ceramic Leadless Chip Carrier with Heat Sink [LCC_HS]
(EP-16-2)

Dimensions shown in millimeters.

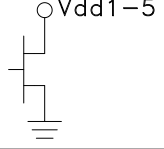
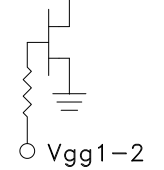
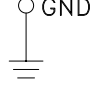
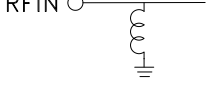
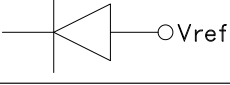
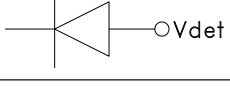
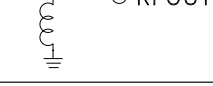
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating ^[2]	Package Marking ^[1]
HMC6981LS6	ALUMINA WHITE	Gold over Nickel	N/A	H6981 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

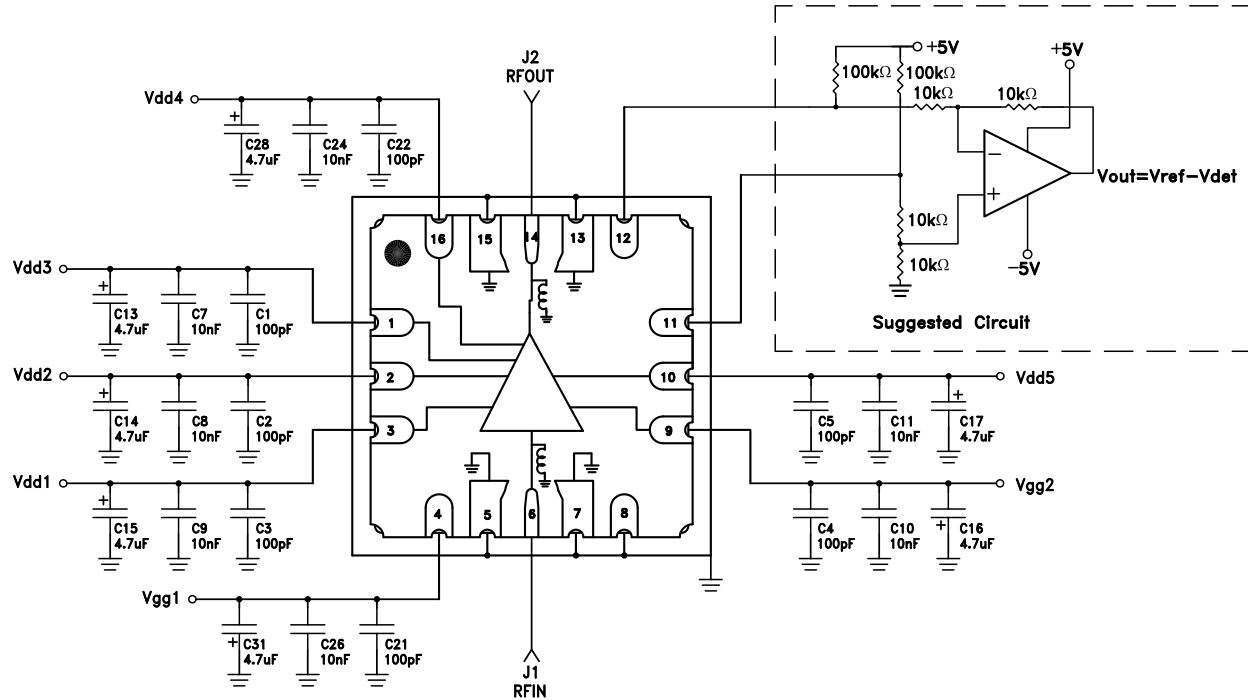

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Pin Descriptions

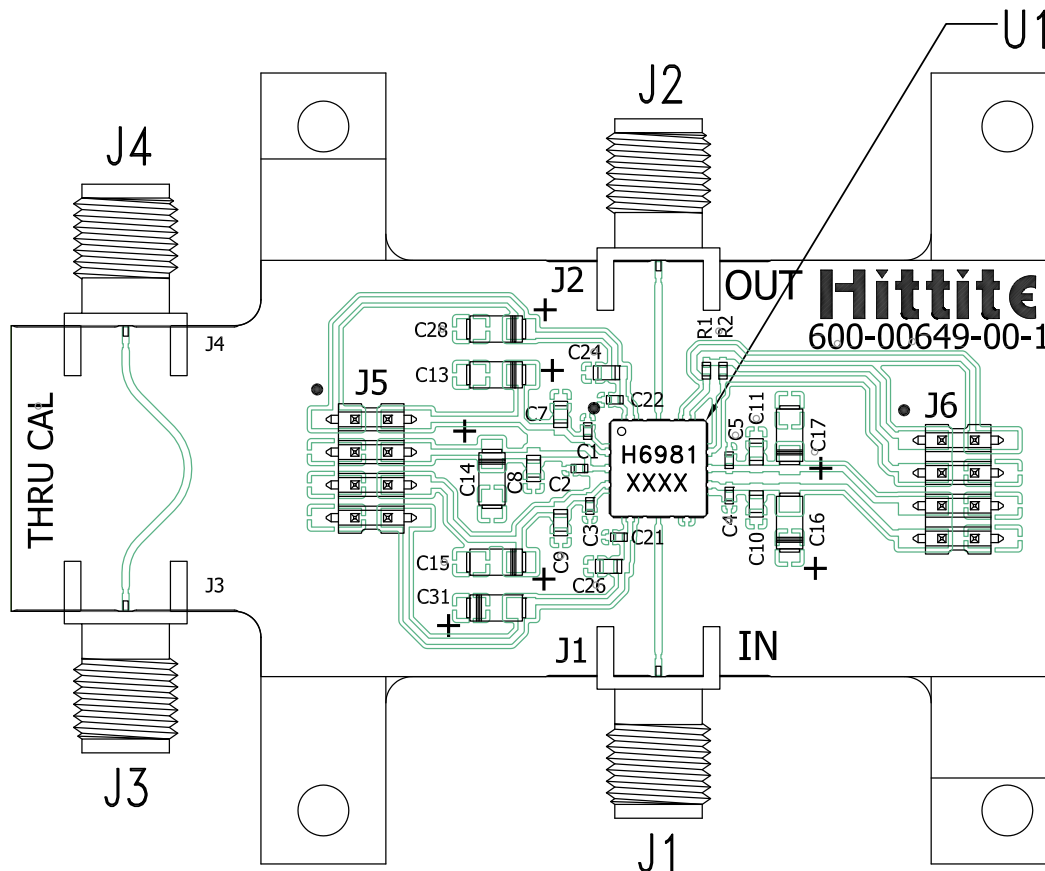
Pad Number	Function	Description	Interface Schematic
1, 2, 3, 10, 16	Vdd3, Vdd2, Vdd1, Vdd5, Vdd4	Drain bias voltage. External bypass capacitors of 100 pF, 10 nF, and 4.7 μ F are required for each pin.	
4, 9	Vgg1, Vgg2	Gate control for PA. Adjust Vgg to achieve recommended bias current. External bypass capacitors 100 pF, 10 nF, and 4.7 μ F are required. Apply Vgg bias to either pin 4 or pin 9.	
5, 7, 13, 15	GND	These pins and exposed ground paddle must be connected to RF/DC ground.	
6	RFIN	This pin is DC coupled and matched to 50 Ohms.	
11	Vref	DC voltage of diode biased through external resistor used for temperature compensation of Vdet. See Application Circuit.	
12	Vdet	DC voltage representing RF output power rectified by diode which is biased through an external resistor. See Application Circuit.	
14	RFOUT	This pin is DC coupled and matched to 50 Ohms.	



**GaAs pHEMT MMIC 2 WATT
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Application Circuit



Evaluation PCB

List of Materials for Evaluation PCB EVAL01-HMC6981LS6 ^[1]

Item	Description
J1 - J4	"K" Connector, SRI
J5, J6	DC Pin
C1 - C5, C21, C22	100 pF Capacitor, 0402 Pkg.
C7 - C11, C24, C26	10000 pF Capacitor, 0603 Pkg.
C13 - C17, C28, C31	4.7 uF Capacitor, Case A Pkg.
R1, R2	42.6K Ohm Resistor, 0402 Pkg.
U1	HMC6981LS6 Amplifier
PCB ^[2]	600-00649-00 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, upon request.