FAIRCHILD SEMICONDUCTOR™

March 1995
Revised March 2001

GTLP16612
18-Bit TTL/GTLP Universal Bus Transceiver

General Description

The GTLP16612 is an 18-bit universal bus transceiver which provides TTL to GTLP signal level translation. The device is designed to provide a high speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control which minimizes signal settling times. GTLP is a Fairchild Semiconductor derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated. Its function is similar to BTL or GTL but with different driver output levels and receiver threshold. GTLP output low voltage is typically less than 0.5V, the output high is 1.5V and the receiver threshold is 1.0V.

Features

- Bidirectional interface between GTLP and TTL logic levels
- Designed with an edge rate control circuit to reduce output noise on GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustability
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible Driver and Control inputs
- Designed using Fairchild advanced CMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- 5V tolerant inputs and outputs on LVTTL port
- Open drain on GTLP to support wired-or connection
- Flow-through pinout optimizes PCB layout
- D-type flip-flop, latch and transparent data paths
- A Port outputs source/sink −32 mA/+32 mA

Ordering Code:

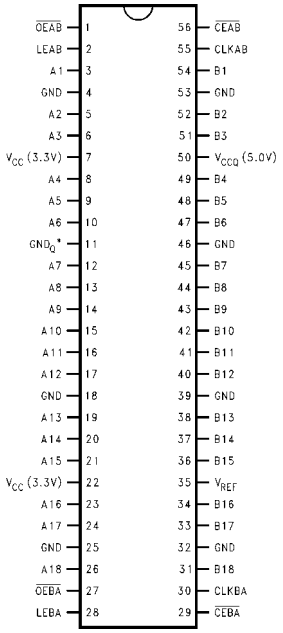
Order Number	Package Number	Package Description
GTLP16612MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
GTLP16612MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW)
$\overline{CEAB}$	A-to-B Clock Enable (Active LOW)
$\overline{CEBA}$	B-to-A Clock Enable (Active LOW)
LEAB	A-to-B Latch Enable (Transparent HIGH)
LEBA	B-to-A Latch Enable (Transparent HIGH)
CLKAB	A-to-B Clock Pulse
CLKBA	B-to-A Clock Pulse
V_{REF}	GTLP Input Reference Voltage
A1–A18	A-to-B TTL Data Inputs or
	B-to-A 3-STATE Outputs
B1–B18	B-to-A GTLP Data Inputs or
	A-to-B Open Drain Outputs

Connection Diagram



Functional Description

The GTLP16612 combines a universal transceiver function with a TTL to GTLP translation. The A Port and control pins operate at LVTTL or 5V TTL levels while the B Port operates at GTLP levels. The transceiver logic includes D-type latches and D-type flip-flops to allow data flow in transparent, latched and clock mode.

The functional operation is described in the truth table below.

Truth Table

(Note 1)

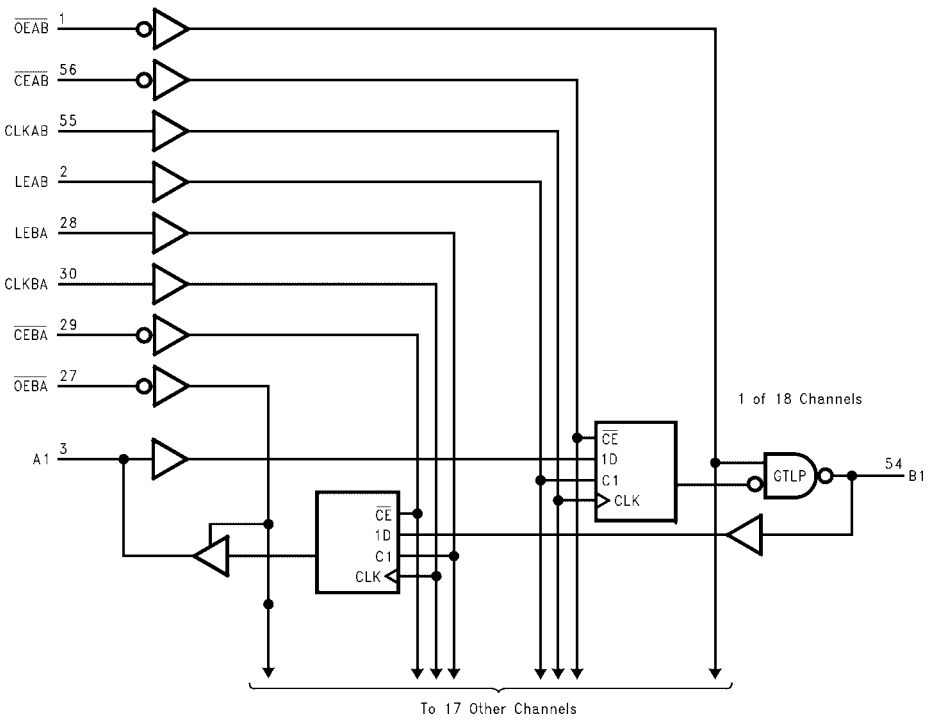
Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched
L	L	L	H	X	B_0(Note 2)	storage
L	L	L	L	X	B_0(Note 3)	of A data
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage
L	L	L	↑	H	H	of A data
H	L	L	X	X	B_0(Note 3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Note 3: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 4)

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +7.0V
Outputs Active (Note 5)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into	
A Port I_{OL}	64 mA
DC Output Source Current from	
A Port I_{OH}	−64 mA
DC Output Sink Current	
into B Port in the LOW State, I_{OL}	80 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
ESD Performance	>2000V

Recommended Operating Conditions (Note 6)

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}	4.75V to 5.25V
Bus Termination Voltage (V_{TT})	1.35V to 1.65V
Input Voltage (V_I)	
on A Port and Control Pins	0.0V to 5.5V
HIGH Level Output Current (I_{OH})	
A Port	−32 mA
LOW Level Output Current (I_{OL})	
A Port	+32 mA
B Port	+34 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (Unless Otherwise Noted).

Symbol		Test Conditions		Min	Typ (Note 7)	Max	Units
V_{IH}	B Port			V_{REF} +0.1		V_{TT}	V
	Others			2.0			V
V_{IL}	B Port			0.0		V_{REF} −0.1	V
	Others					0.8	
V_{REF}					1.0		V
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 8)	I_{OH} = −100 µA	V_{CC} − 0.2			V
		V_{CC} = 3.15V	I_{OH} = −8 mA	2.4			
		V_{CCQ} = 4.75V	I_{OH} = −32 mA	2.0			
V_{OL}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 8)	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 32 mA			0.5	
	B Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 34 mA			0.65	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 5.5V or 0V			±10	µA
	A Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = 5.5V			20	µA
			V_I = V_{CC}			1	
			V_I = 0			−30	
	B Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	µA
			V_I = 0			−5	
I_{OFF}	A Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	µA
$I_{I(hold)}$	A Port	V_{CC} = 3.15V, V_{CCQ} = 4.75V	V_I = 0.8V	75			µA
			V_I = 2.0V	−20			
I_{OZH}	A Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.45V			1	µA
	B Port		V_O = 1.5V			5	
I_{OZL}	A Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−20	µA
	B Port		V_O = 0.65V			−10	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 7)	Max	Units
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs HIGH		30	40	mA
			Outputs LOW		30	40	
			Outputs Disabled		30	40	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs HIGH		0	1	mA
			Outputs LOW		0	1	
			Outputs Disabled		0	1	
ΔI_{CC} (Note 9)	A Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V		0	1	mA
C_{IN}	Control Pins		V_I = V_{CCQ} or 0		8		pF
$C_{I/O}$	A Port		V_I = V_{CCQ} or 0		9		
$C_{I/O}$	B Port		V_I = V_{CCQ} or 0		6		

Note 7: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

Note 8: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 9: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

Symbol			Min	Max	Unit
f_{MAX}	Maximum Clock Frequency		150		MHz
t_W	Pulse Duration	LEAB or LEBA HIGH	3.0		ns
		CLKAB or CLKBA HIGH or LOW	3.2		
t_S	Setup Time	A before CLKAB↑	0.5		ns
		B before CLKBA↑	3.1		
		A before LEAB↓	1.3		
		B before LEBA↓	3.7		
		$\overline{CEAB}$ before CLKAB↑	0.4		
		$\overline{CEBA}$ before CLKBA↑	1.0		
t_H	Hold Time	A after CLKAB↑	1.5		ns
		B after CLKBA↑	0.0		
		A after LEAB↓	0.5		
		B after LEBA↓	0.0		
		$\overline{CEAB}$ after CLKAB↑	1.5		
		$\overline{CEBA}$ after CLKBA↑	1.7		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

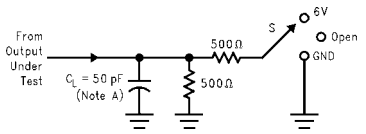
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 10)	Max	Unit
t_{PLH}	A	B	1.0	4.3	6.5	ns
t_{PHL}			1.0	5.0	8.2	
t_{PLH}	LEAB	B	1.8	4.5	6.7	ns
t_{PHL}			1.5	5.3	8.6	
t_{PLH}	CLKAB	B	1.8	4.6	6.7	ns
t_{PHL}			1.5	5.4	8.7	
t_{PLH}	$\overline{OEAB}$	B	1.6	4.4	6.2	ns
t_{PHL}			1.3	6.1	9.8	
t_{RISE}	Transition time, B outputs (20% to 80%)			2.6		ns
t_{FALL}	Transition time, B outputs (20% to 80%)			2.6		
t_{PLH}	B	A	2.0	5.6	8.2	ns
t_{PHL}			1.4	5.0	7.2	
t_{PLH}	LEBA	A	2.1	4.2	6.3	ns
t_{PHL}			1.9	3.3	5.0	
t_{PLH}	CLKBA	A	2.3	4.4	6.8	ns
t_{PHL}			2.2	3.5	5.2	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	1.5	5.0	6.2	ns
t_{PHZ}, t_{PLZ}			1.9	3.9	7.9	

Note 10: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C.

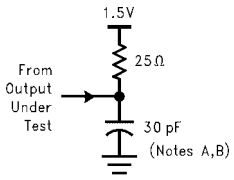
Test Circuits and Timing Waveforms

Test Circuit for A Outputs



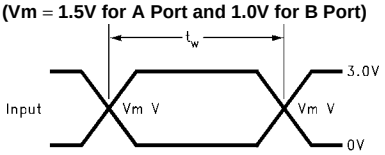
C_L includes probes and jig capacitance.

Test Circuit for B Outputs

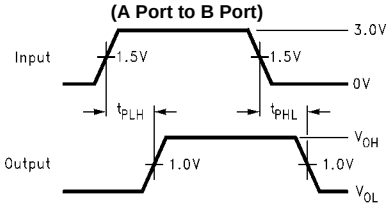


C_L includes probes and jig capacitance. For B Port outputs, C_L = 30 pF is used for worst case edge rate.

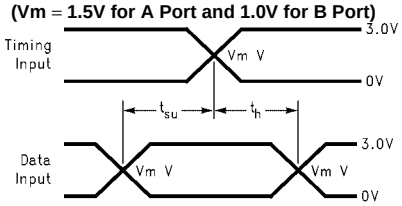
Voltage Waveforms Pulse Duration (Vm = 1.5V for A Port and 1.0V for B Port)



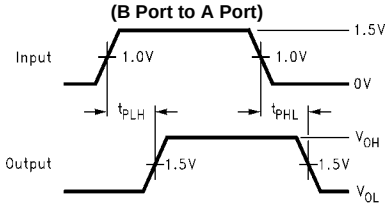
Voltage Waveforms Propagation Delay Times (A Port to B Port)



Voltage Waveforms Setup and Hold Times (Vm = 1.5V for A Port and 1.0V for B Port)

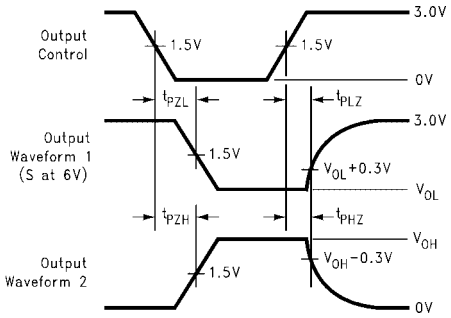


Voltage Waveforms Propagation Delay Times (B Port to A Port)



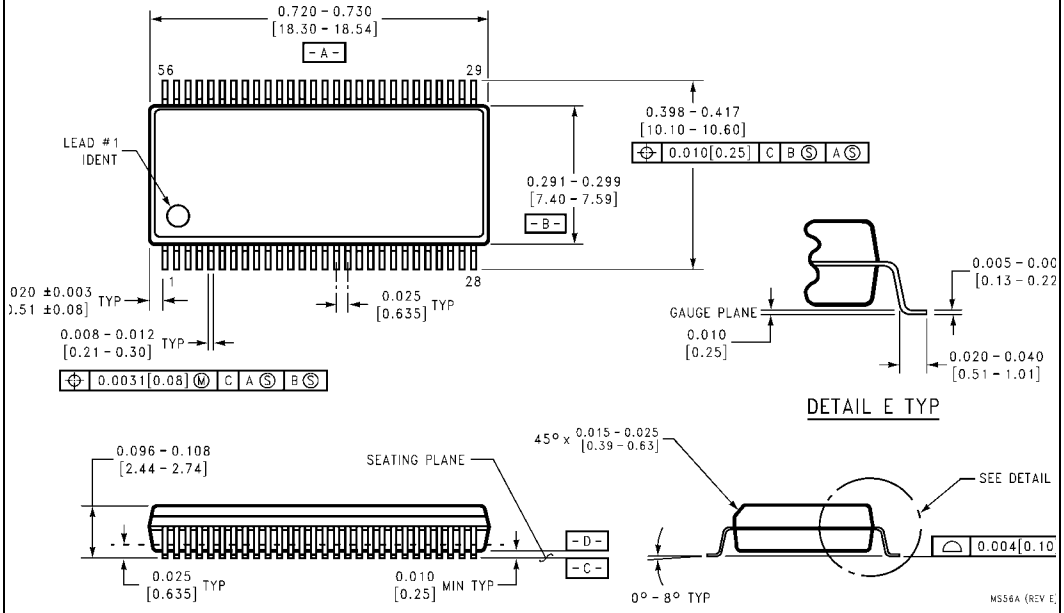
All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

Voltage Waveforms Enable and Disable Times (A Port)



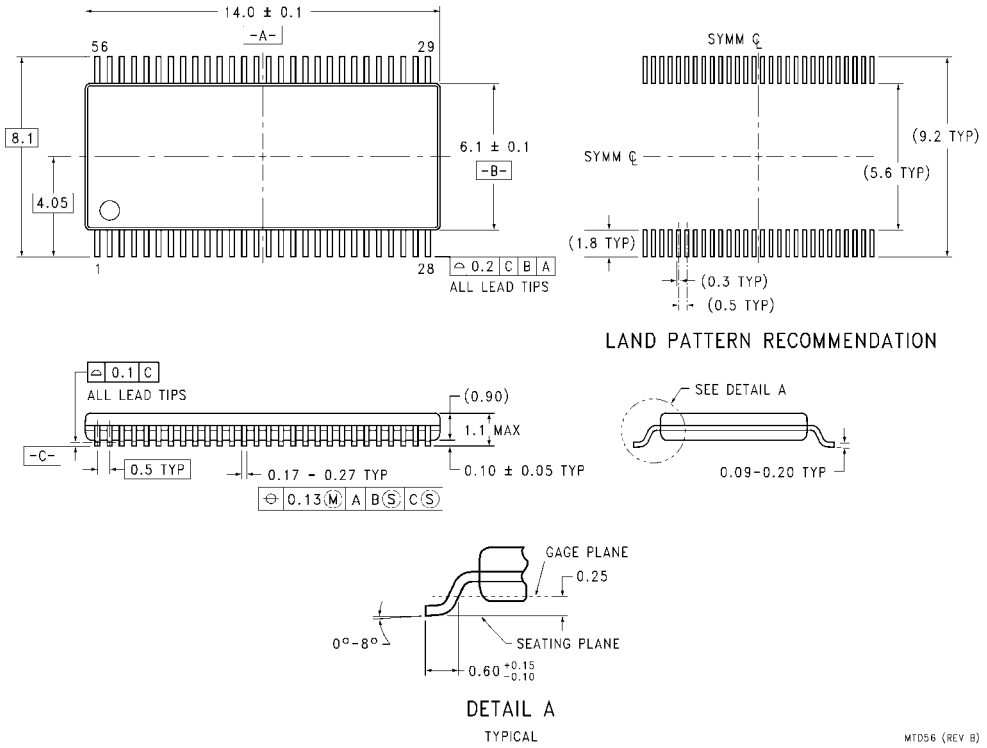
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control. All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω. The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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GTLP16612

CMOS 18-Bit TTL/GTLP Universal Bus Transceiver

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- A Port outputs source/sink -32 mA/+32 mA

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Product status/pricing/packaging BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
GTLP16612MEA	Full Production	Full Production	$6.29	SSOP	56	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: GTLP16612
GTLP16612MEAX	Full Production	Full Production	$6.29	SSOP	56	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: GTLP16612
GTLP16612MEAX_NL	Full Production	Full Production	N/A	SSOP	56	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: GTLP16612
GTLP16612MTD	Full Production	Full Production	$6.29	TSSOP	56	RAIL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: GTLP16612
GTLP16612MTDX	Full Production	Full Production	$6.29	TSSOP	56	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &**2** (2-Digit Date Code) &**T** (Die Trace Code) Line 2: GTLP16612

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product GTLP16612 is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Vcc range	Software version	Revision date
HSPICE					
TSSOP-56	Slow	-40°C to 85°C	3.15V to 3.45V	97.1	Jun 1, 1998
	Fast	-40°C to 85°C	3.15V to 3.45V	97.1	Jun 1, 1998
	Typical	-40°C to 85°C	3.15V to 3.45V	97.1	Jun 1, 1998
IBIS					
SSOP-56	All	-40°C to 85°C	3V to 3.6V	2.1	Feb 22, 1999
TSSOP-56	All	-40°C to 85°C	3V to 3.6V	2.1	Feb 22, 1999

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Application notes

AN-1065: GTLP: An Interface Technology for Bus and Backplane Applications (93 K) Jul 27, 2007
AN-1070: GTLP vs. GTL: A Performance Comparison from a System Perspective (108 K) Jul 27, 2007
AN-1070K: Korean Translation: Fairchild's GTLP vs. TI's GTL: A Performance Comparison from a System Perspective (525 K) Jul 27, 2007
AN-1070SC: Chinese Translation: Fairchild's GTLP vs. TI's GTL: A Performance Comparison from a Systems Perspective (595 K) Jul 27, 2007
AN-1072: GTLP Output Control Circuitry: Reduces Noise and Enhances System Performance (79 K) Jul 27, 2007
AN-1072J: Japanese Translation: GTLP Output Control Circuitry: Reduces Noise and Enhances System Performance (416 K) Jul 27, 2007
AN-1097: GTLP: Understanding Output Drive (43 K) Jul 27, 2007
AN-5002: GTLP: Single vs. Multiple Output Switching Technical Discussion (38 K) Jul 27, 2007
AN-5013: GTLP in BTL Applications (54 K) Jul 27, 2007
MS-507: Extended Characterization Data for GTLP16612, GTLP16616, GTLP16617 (45 K) Jul 27, 2007
MS-537: Interface Products Ordering Information and Physical Dimensions (581 K) Jul 27, 2007
MS-548: GTLP AC Loading Circuits and Waveforms (27 K) Jul 27, 2007
MS-550: GTLP Product Feature Matrix (18 K) Jul 27, 2007
MS-565: Backplane Designer's Guide - Section 5 - Backplane Signal Conditioning (260 K) Jul 27, 2007

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Qualification Support

Click on a product for detailed qualification data

Product
GTLP16612MEA
GTLP16612MEAX
GTLP16612MEAX_NL
GTLP16612MTD
GTLP16612MTDX

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