AK9242NK
Application notes

This document shows circuit and layout diagrams of the AK9242 as the reference design.

■ Circuit Diagram
It shows compositions of power supply decoupling capacitors.

Peripheral Parts/Pattern Details
C7,C8 : Decoupling Capacitor for VDD
C9,C10 : Decoupling Capacitor for DRVDD
C11,C12: Decoupling Capacitor for VREFP-VREFN
C13 : Decoupling Capacitor for LDO0
C14 : Decoupling Capacitor for LDO1

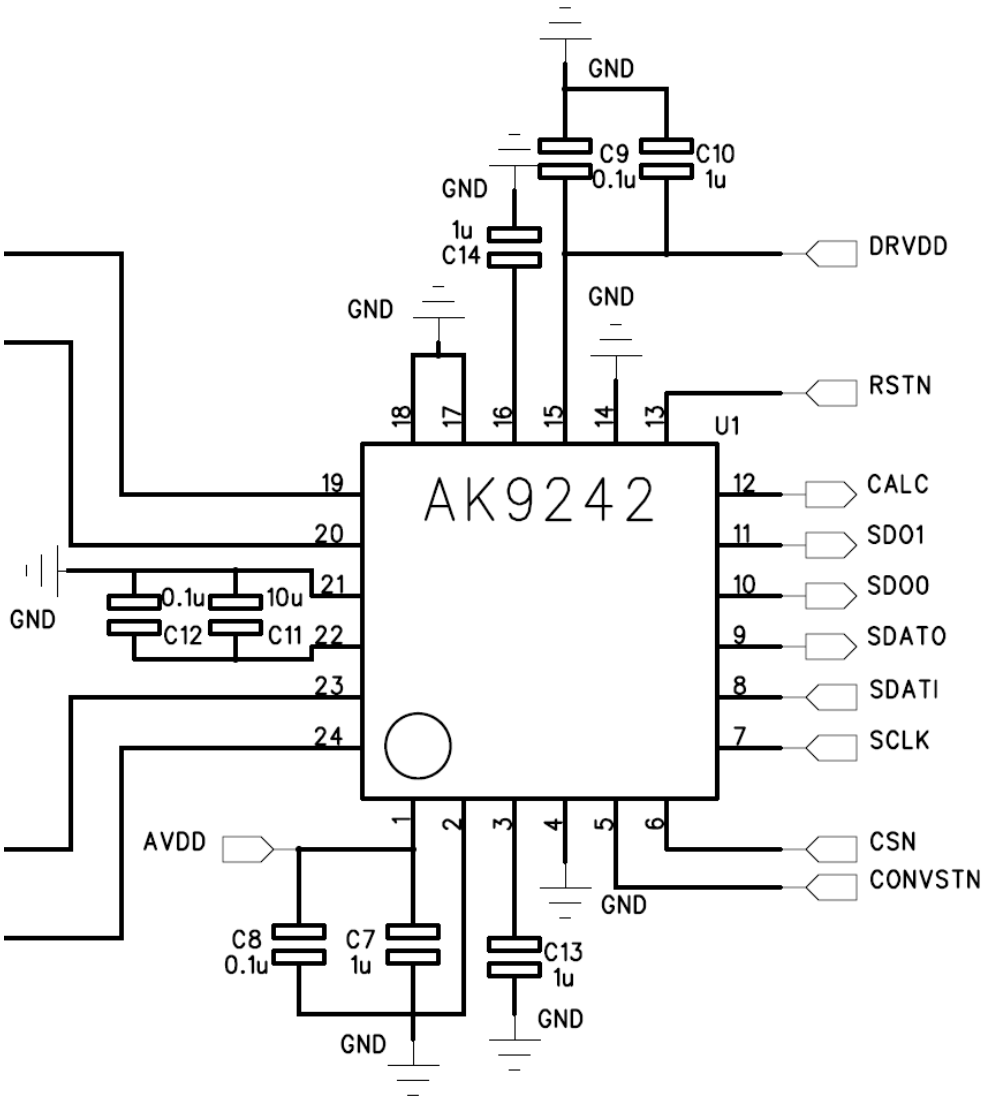


Figure 1 Circuit Diagram

■ **Layout**

Four layered printing board is used. The second layer is for the ground and the third layer is for power supply. VDD and DRVDD are separated on the power supply layer.
All areas except parts and wirings are GND in the first and the fourth layers.
All used chip parts here are located as 1005 (1.0mm x 0.5mm) size layout.

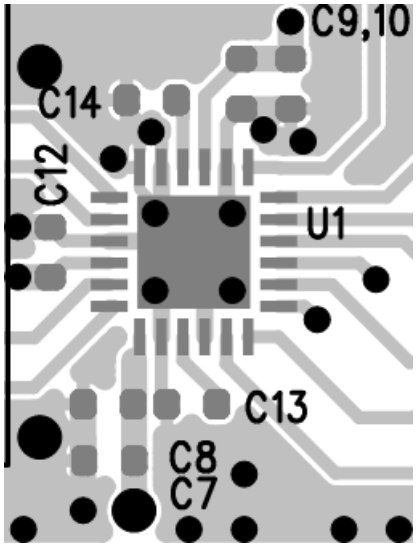


Figure 2 First Layer Layout

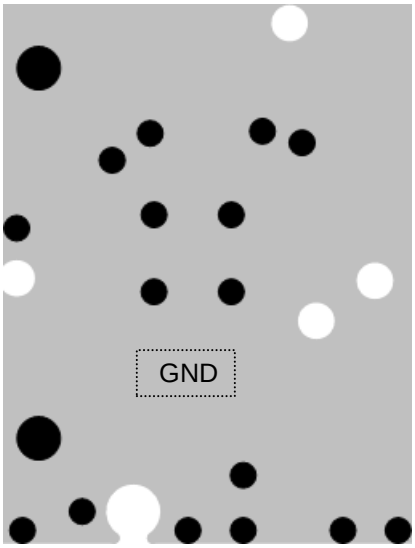


Figure 3 Second Layer Layout

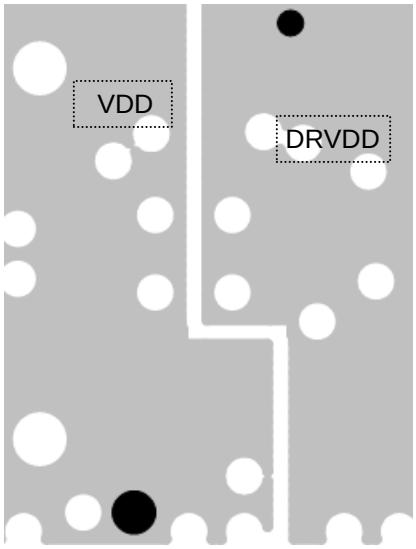


Figure 4 Third Layer Layout

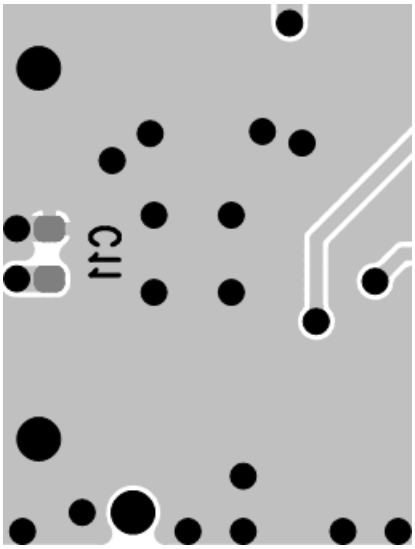


Figure 5 Fourth Layer Layout (Reverse Side)

Digital wiring reduction method for the AK9242 is shown in this document.

The AK9242 have a CONVSTN, CSN, SDATI, SDATO, SDO0, SDO1 and CALC pins. Wiring can be reduced according to the application and the environment. Maximum four digital wiring can be eliminated.

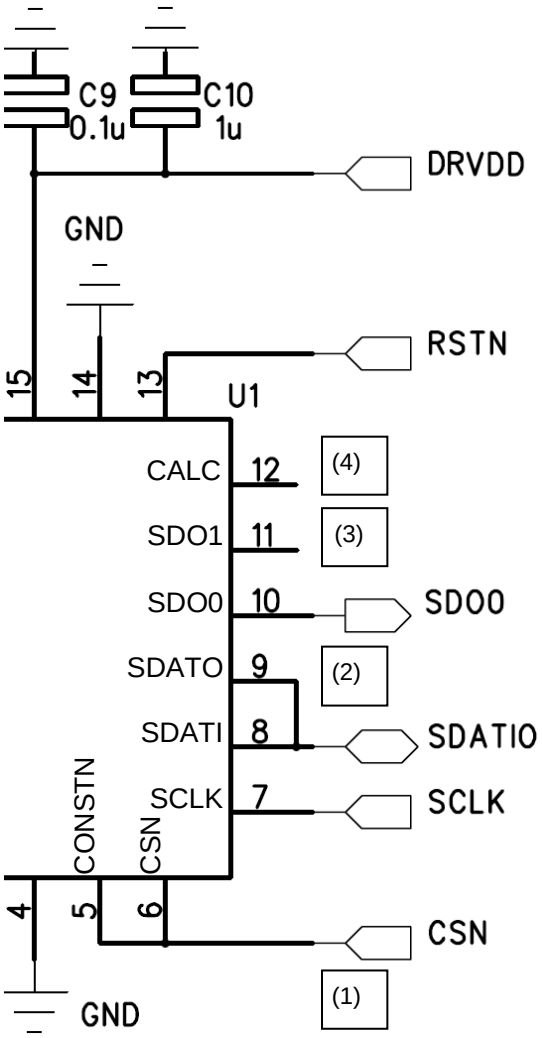


Figure 6. Circuit Diagram

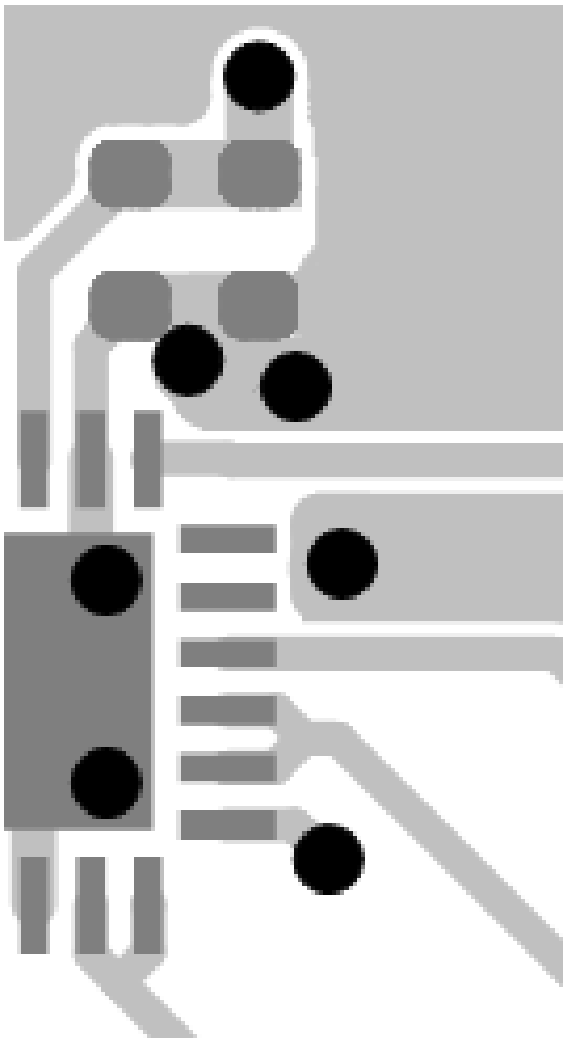


Figure 7. Layout

(1) Short of CONVSTN/CSN Pins

The CONVSTN pin and the CSN pin can be shorted and used as a common pin.
Data sampled on a falling edge of the CONVSTN/CSN pin will be output from the SDOx pin on the next falling edge of the CONVSTN/CSN pin.
The SCLK pin must be set to “H” when setting the CSN pin to “L”.
Figure 8 shows an example of the AK9242.

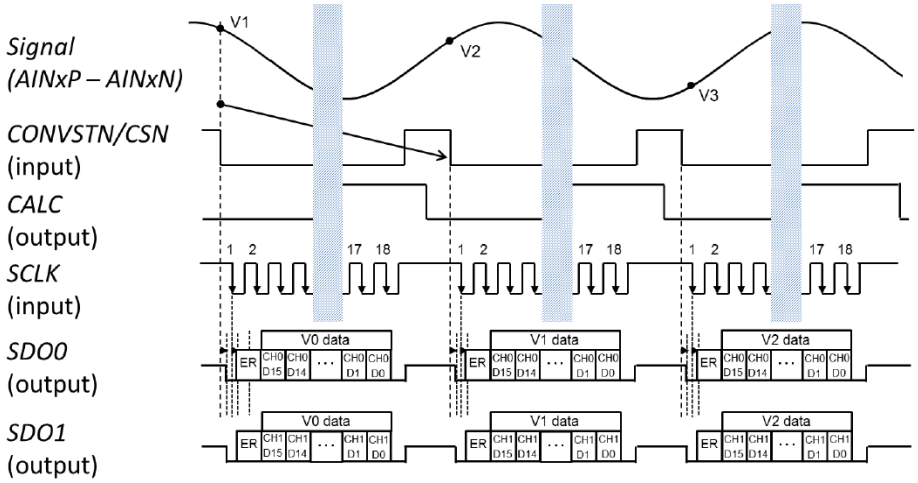
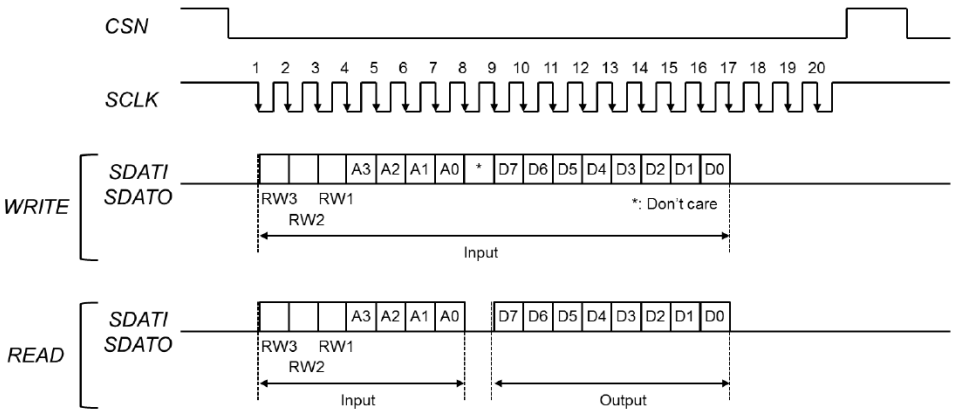


Figure 8. Data Output Timing (CONVSTN, CSN Common)

(2) Short of SDATO/SDATI Pins

Register writing and reading via 3-wire serial interface (CSN, SCLK and SDATI/SDATO pins) are enabled by shorting the SDATO pin and the SDATI pin.
In this case, the pin of a connected device to the AK924X should be I/O pin.
The SCLK pin must be set to “H” when setting the CSN pin to “L”.



RW3-RW1: Op code
“110” = WRITE
“101” = READ
A3-A0: Register Address
D7-D0: Control Data

Figure 9. Serial I/F Timing (SDATI, SDATO Common)

(3) Wiring Reduction of SDO0 or SDO1

By setting CONT bit = "1" (serial output mode) by register access, the A/D conversion result of the CH1 is output from the SDO0 pin after outputting the A/D conversion result of the CH0 (the A/D conversion result of the CH0 is output from the SDO1pin after outputting the A/D conversion result of the CH1). In this case, clock should be input continuously for 37 cycles to the SCLK pin while the CSN pin is "L". "L" signal is output from SDOX pins when the 38th or more clock cycles are input.
The SCLK pin must be set to "H" when setting the CSN pin to "L".
* The maximum conversion rate is 0.97MSPS in serial output mode.
Figure 10 shows an example of the AK9242.

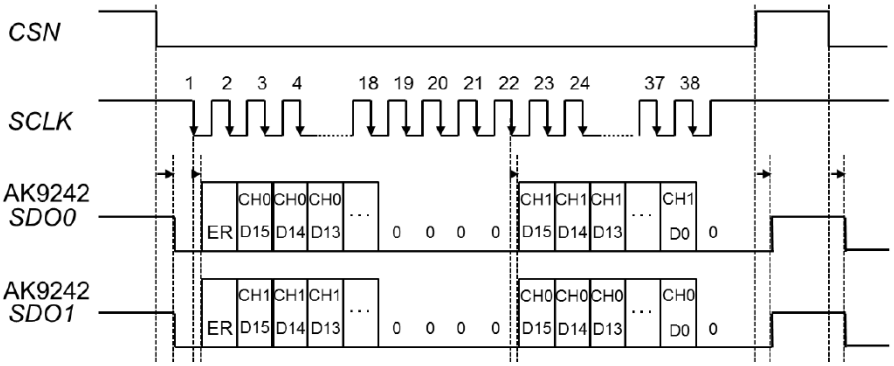


Figure 10. Data Output Timing in Serial Output Mode

(4) Wiring Reduction of the CALC Pin

Monitoring by the CALC pin is not necessary in following two cases.

1. In case of receiving data on a falling edge "↓" of CSN after tDD (max) from a falling edge "↓" of CONVSTN.

Parameter	Symbol	Min.	Max.	Unit
Throughput Rate	fCYC	0.05	1.1	MSPS
Conversion Time	tCYC	0.91	20	µs
Conversion Pulse Width	tCVS	68	-	ns
CONVSTN Low to CALC High Delay	tDCC	-	300	ns
CALC High Time	tCALC	-	550	ns
CONVSTN Low to Data Valid Delay	tDD	-	850	ns
CALC Low to CSN Low Set Up time	tDCCS	0	-	ns

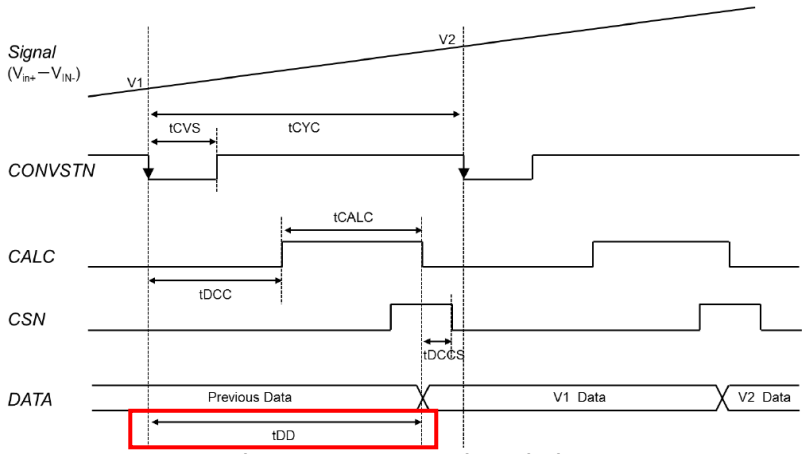


Figure 11. Conversion Timing

2. In case of "(1)", shorting the CONVSTN/CSN pins

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