National Semiconductor

T-46-09-05

# MM54HC194/MM74HC194
# 4-Bit Bidirectional Universal Shift Register

## General Description

This 4-bit high speed bidirectional shift register utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. This device operates at speeds similar to the equivalent low power Schottky part.

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction $Q_A$ toward $Q_D$); SHIFT LEFT; INHIBIT CLOCK (do nothing).

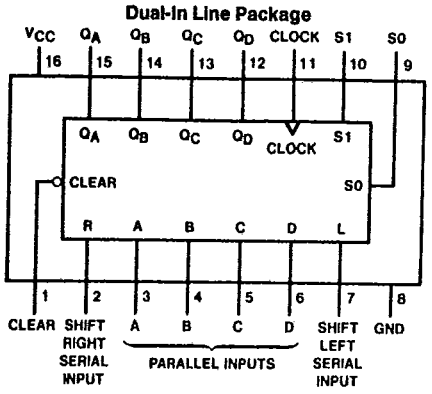
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into their respective flip flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 160 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

## Connection Diagram

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**Order Number MM54HC194* or MM74HC194***

*Please look into Section 8, Appendix D for availability of various package types.

## Function Table

| Inputs | | | | | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear | Mode S1 | Mode S2 | Clock | Serial Left | Serial Right | Parallel A | B | C D | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ |
| L | X | X | X | X | X | X | X | X X | L | L | L | L |
| H | X | X | L | X | X | X | X | X X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |
| H | H | H | ↑ | X | X | a | b | c d | a | b | c | d |
| H | L | H | ↑ | X | H | X | X | X X | H | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | L | H | ↑ | X | L | X | X | X X | L | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ |
| H | H | L | ↑ | H | X | X | X | X X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | H |
| H | H | L | ↑ | L | X | X | X | X X | $Q_{Bn}$ | $Q_{Cn}$ | $Q_{Dn}$ | L |
| H | L | L | X | X | X | X | X | X X | $Q_{A0}$ | $Q_{B0}$ | $Q_{C0}$ | $Q_{D0}$ |

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

$Q_{A0}$, $Q_{B0}$, $Q_{C0}$, $Q_{D0}$ = the level of $Q_A$, $Q_B$, $Q_C$, or $Q_D$, respectively, before the indicated steady-state input conditions were established.

$Q_{An}$, $Q_{Bn}$, $Q_{Cn}$, $Q_{Dn}$ = the level of $Q_A$, $Q_B$, $Q_C$, respectively, before the most-recent ↑ transition of the clock.

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$+1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$+0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temperature ($T_L$) (Soldering 10 seconds) | 260°C |

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | 0 | $V_{CC}$ | V |
| Operating Temp. Range ($T_A$) | | | |
| MM74HC | −40 | +85 | °C |
| MM54HC | −55 | +125 | °C |
| Input Rise or Fall Times ($t_r$, $t_f$) $V_{CC}$=2.0V | | 1000 | ns |
| $V_{CC}$=4.5V | | 500 | ns |
| $V_{CC}$=6.0V | | 400 | ns |

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$=25°C | 74HC $T_A$=−40 to 85°C | 54HC $T_A$=−55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum High Level Output Voltage | $V_{IN}=V_{IH}$ or $V_{IL}$ $\|I_{OUT}\|\leq 20\ \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V |
| | | $V_{IN}=V_{IH}$ or $V_{IL}$ $\|I_{OUT}\|\leq 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $\|I_{OUT}\|\leq 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| $V_{OL}$ | Maximum Low Level Output Voltage | $V_{IN}=V_{IH}$ or $V_{IL}$ $\|I_{OUT}\|\leq 20\ \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{IN}=V_{IH}$ or $V_{IL}$ $\|I_{OUT}\|\leq 4.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $\|I_{OUT}\|\leq 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}=V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$ | 6.0V | | 8.0 | 80 | 160 | μA |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V ± 10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$=5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**$V_{IL}$ limits are currently tested at 20% of $V_{CC}$. The above $V_{IL}$ specification (30% of $V_{CC}$) will be implemented no later than Q1, CY'89.

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## AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | | 50 | 35 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to Q | | 17 | 24 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Q | | 19 | 25 | ns |
| $t_{REM}$ | Minimum Removal Time, Reset Inactive to Clock | | | 5 | ns |
| $t_S$ | Minimum Setup Time (A, B, C, D to Clock) | | | 20 | ns |
| $t_S$ | Minimum Setup Time Mode Controls to Clock | | | 20 | ns |
| $t_W$ | Minimum Pulse Width Clock or Reset | | 9 | 16 | ns |
| $t_H$ | Minimum Hold Time any Input | | −3 | 0 | ns |

## AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A=25°C$ | 74HC $T_A=-40$ to 85°C | 54HC $T_A=-55$ to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $f_{MAX}$ | Maximum Operating Frequency | | 2.0V | 10 | 6 | 5 | 4 | MHz |
| | | | 4.5V | 45 | 30 | 24 | 20 | MHz |
| | | | 6.0V | 50 | 35 | 28 | 24 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to Q | | 2.0V | 70 | 145 | 183 | 216 | ns |
| | | | 4.5V | 15 | 29 | 37 | 45 | ns |
| | | | 6.0V | 12 | 25 | 31 | 37 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Q | | 2.0V | 80 | 150 | 189 | 216 | ns |
| | | | 4.5V | 15 | 30 | 37 | 45 | ns |
| | | | 6.0V | 12 | 26 | 31 | 37 | ns |
| $t_{THL}$, $t_{TLH}$ | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| $t_{REM}$ | Minimum Removal Time Reset Inactive to Clock | | 2.0V | | 5 | 5 | 5 | ns |
| | | | 4.5V | | 5 | 5 | 5 | ns |
| | | | 6.0V | | 5 | 5 | 5 | ns |
| $t_S$ | Minimum Set Up Time (A, B, C, or D to Clock) | | 2.0V | | 100 | 125 | 150 | ns |
| | | | 4.5V | | 20 | 25 | 30 | ns |
| | | | 6.0V | | 17 | 21 | 25 | ns |
| $t_S$ | Minimum Set Time Mode Controls to Clock | | 2.0V | | 100 | 125 | 150 | ns |
| | | | 4.5V | | 20 | 25 | 30 | ns |
| | | | 6.0V | | 17 | 21 | 25 | ns |
| $t_H$ | Minimum Hold Time any Input | | 2.0V | −10 | 0 | 0 | 0 | ns |
| | | | 4.5V | −3 | 0 | 0 | 0 | ns |
| | | | 6.0V | −3 | 0 | 0 | 0 | ns |
| $t_W$ | Minimum Pulse Width Clock or Reset | | 2.0V | 30 | 80 | 100 | 120 | ns |
| | | | 4.5V | 89 | 16 | 20 | 24 | ns |
| | | | 6.0V | 8 | 14 | 18 | 20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Time | | 2.0V | | 1000 | 1000 | 1000 | ns |
| | | | 4.5V | | 500 | 500 | 500 | ns |
| | | | 6.0V | | 400 | 400 | 400 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | | | 77 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

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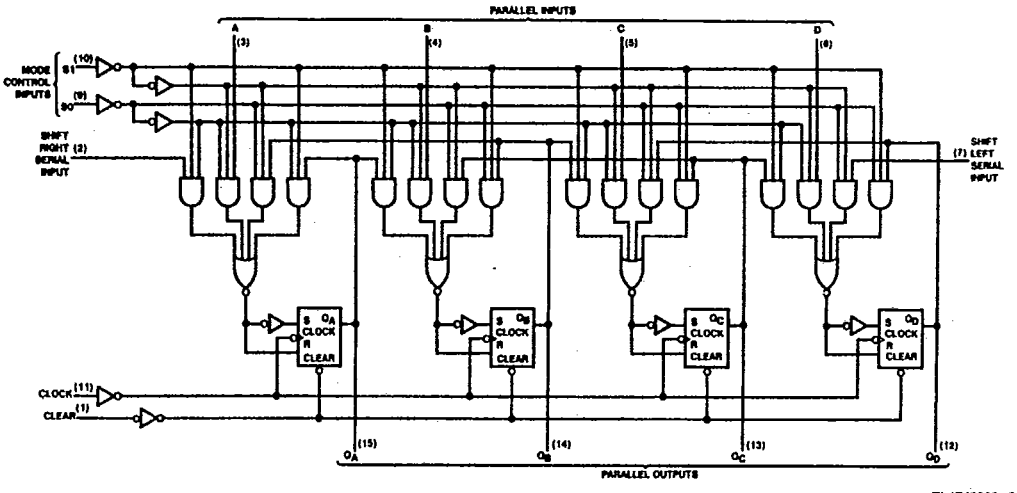
## Logic and Timing Diagrams

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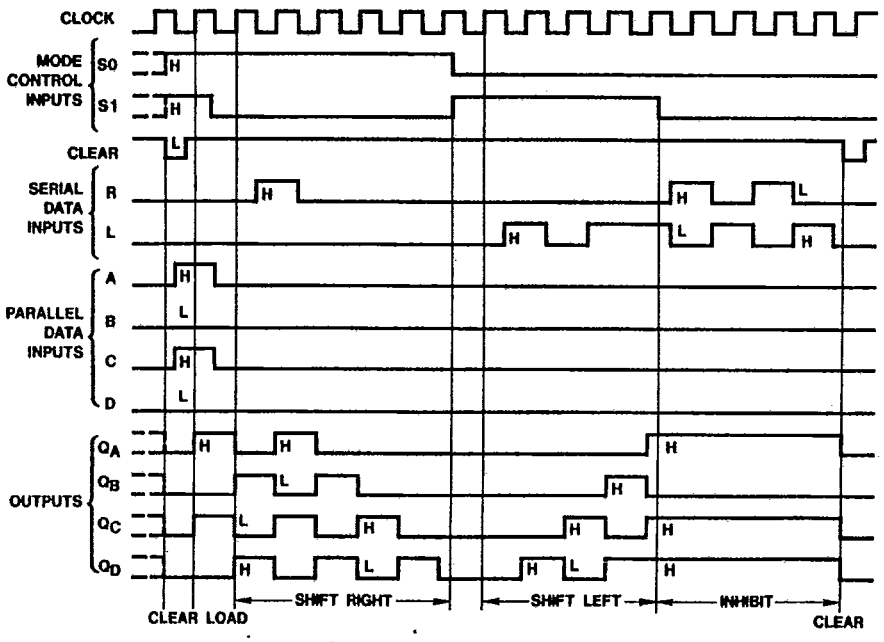


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