

# NSTB1002DXV5T1G, NSTB1002DXV5T5G

Preferred Devices

## Dual Common Base-Collector Bias Resistor Transistors NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSTB1002DXV5T1G series, two complementary devices are housed in the SOT-553 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- These are Pb-Free Devices

**MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for Q<sub>1</sub> and Q<sub>2</sub>, - minus sign for Q<sub>1</sub> (PNP) omitted)

Rating	Symbol	Value		Unit
		Q1	Q2	
Collector-Base Voltage	$V_{CBO}$	-40	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	-40	50	Vdc
Collector Current	$I_C$	-200	100	mAdc

### THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

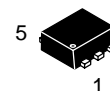
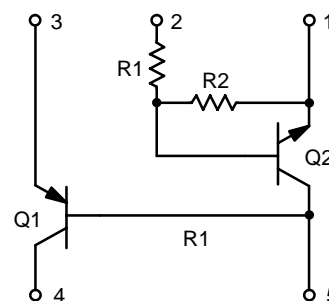
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. FR-4 @ Minimum Pad



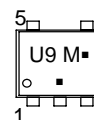
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SOT-553  
CASE 463B

### MARKING DIAGRAM



U9 = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping
NSTB1002DXV5T1G	SOT-553 (Pb-Free)	4 mm pitch 4000/Tape & Reel
NSTB1002DXV5T5G	SOT-553 (Pb-Free)	2 mm pitch 8000/Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

# NSTB1002DXV5T1G, NSTB1002DXV5T5G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### Q1 TRANSISTOR: PNP OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (Note 2)	V <sub>(BR)CEO</sub>	-40	-	-	Vdc
Collector-Base Breakdown Voltage	V <sub>(BR)CBO</sub>	-40	-	-	Vdc
Emitter-Base Breakdown Voltage	V <sub>(BR)EBO</sub>	-5.0	-	-	Vdc
Base Cutoff Current	I <sub>BL</sub>	-	-	-50	nAdc
Collector Cutoff Current	I <sub>CEX</sub>	-	-	-50	nAdc

### ON CHARACTERISTICS (Note 2)

DC Current Gain (I <sub>C</sub> = -0.1 mAdc, V <sub>CE</sub> = -1.0 Vdc) (I <sub>C</sub> = -1.0 mAdc, V <sub>CE</sub> = -1.0 Vdc) (I <sub>C</sub> = -10 mAdc, V <sub>CE</sub> = -1.0 Vdc) (I <sub>C</sub> = -50 mAdc, V <sub>CE</sub> = -1.0 Vdc) (I <sub>C</sub> = -100 mAdc, V <sub>CE</sub> = -1.0 Vdc)	h <sub>FE</sub>		60 80 100 60 30	- - 300 - -	-
Collector-Emitter Saturation Voltage (I <sub>C</sub> = -10 mAdc, I <sub>B</sub> = -1.0 mAdc) (I <sub>C</sub> = -50 mAdc, I <sub>B</sub> = -5.0 mAdc)	V <sub>CE(sat)</sub>		- -	-0.25 -0.4	Vdc
Base-Emitter Saturation Voltage (I <sub>C</sub> = -10 mAdc, I <sub>B</sub> = -1.0 mAdc) (I <sub>C</sub> = -50 mAdc, I <sub>B</sub> = -5.0 mAdc)	V <sub>BE(sat)</sub>		-0.65 -	-0.85 -0.95	Vdc

### SMALL-SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product	f <sub>T</sub>	250	-	-	MHz
Output Capacitance	C <sub>obo</sub>	-	4.5	-	pF
Input Capacitance	C <sub>ibo</sub>	-	10.0	-	pF
Input Impedance (V <sub>CE</sub> = -10 Vdc, I <sub>C</sub> = -1.0 mAdc, f = 1.0 kHz)	h <sub>ie</sub>	2.0	12	-	kΩ
Voltage Feedback Ratio (V <sub>CE</sub> = -10 Vdc, I <sub>C</sub> = -1.0 mAdc, f = 1.0 kHz)	h <sub>re</sub>	0.1	10	-	X 10 <sup>-4</sup>
Small-Signal Current Gain (V <sub>CE</sub> = -10 Vdc, I <sub>C</sub> = -1.0 mAdc, f = 1.0 kHz)	h <sub>fe</sub>	100	400	-	-
Output Admittance (V <sub>CE</sub> = -10 Vdc, I <sub>C</sub> = -1.0 mAdc, f = 1.0 kHz)	h <sub>oe</sub>	3.0	60	-	μmhos
Noise Figure (V <sub>CE</sub> = -5.0 Vdc, I <sub>C</sub> = -100 μAdc, R <sub>S</sub> = 1.0 kΩ, f = 1.0 kHz)	nF	-	4.0	-	dB

### SWITCHING CHARACTERISTICS

Delay Time	(V <sub>CC</sub> = -3.0 Vdc, V <sub>BE</sub> = 0.5 Vdc)	t <sub>d</sub>	-	35	ns
Rise Time	(I <sub>C</sub> = -10 mAdc, I <sub>B1</sub> = -1.0 mAdc)	t <sub>r</sub>	-	35	
Storage Time	(V <sub>CC</sub> = -3.0 Vdc, I <sub>C</sub> = -10 mAdc)	t <sub>s</sub>	-	225	ns
Fall Time	(I <sub>B1</sub> = I <sub>B2</sub> = -1.0 mAdc)	t <sub>f</sub>	-	75	

### Q2 TRANSISTOR: NPN

#### OFF CHARACTERISTICS

Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	-	-	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	-	-	500	nAdc
Emitter-Base Cutoff Current (V <sub>EB</sub> = 6.0, I <sub>C</sub> = 5.0 mA)	I <sub>EBO</sub>	-	-	0.1	mAdc

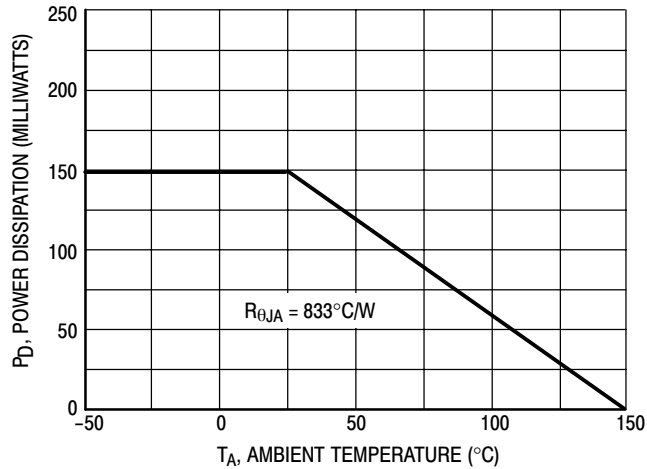
2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

# NSTB1002DXV5T1G, NSTB1002DXV5T5G

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b>					
Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage ( $I_C = 2.0\ \text{mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	Vdc
DC Current Gain ( $V_{CE} = 10\ \text{V}$ , $I_C = 5.0\ \text{mA}$ )	$h_{FE}$	80	140	–	
Collector-Emitter Saturation Voltage ( $I_C = 10\ \text{mA}$ , $I_B = 0.3\ \text{mA}$ )	$V_{CE(SAT)}$	–	–	0.25	Vdc
Output Voltage (on) ( $V_{CC} = 5.0\ \text{V}$ , $V_B = 2.5\ \text{V}$ , $R_L = 1.0\ \text{k}\Omega$ )	$V_{OL}$	–	–	0.2	Vdc
Output Voltage (off) ( $V_{CC} = 5.0\ \text{V}$ , $V_B = 0.5\ \text{V}$ , $R_L = 1.0\ \text{k}\Omega$ )	$V_{OH}$	4.9	–	–	Vdc
Input Resistor	R1	33	47	61	$\text{k}\Omega$
Resistor Ratio	R1/R2	0.8	1.0	1.2	

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2.0\%$ .



**Figure 1. Derating Curve**

# NSTB1002DXV5T1G, NSTB1002DXV5T5G

## TYPICAL ELECTRICAL CHARACTERISTICS — PNP TRANSISTOR

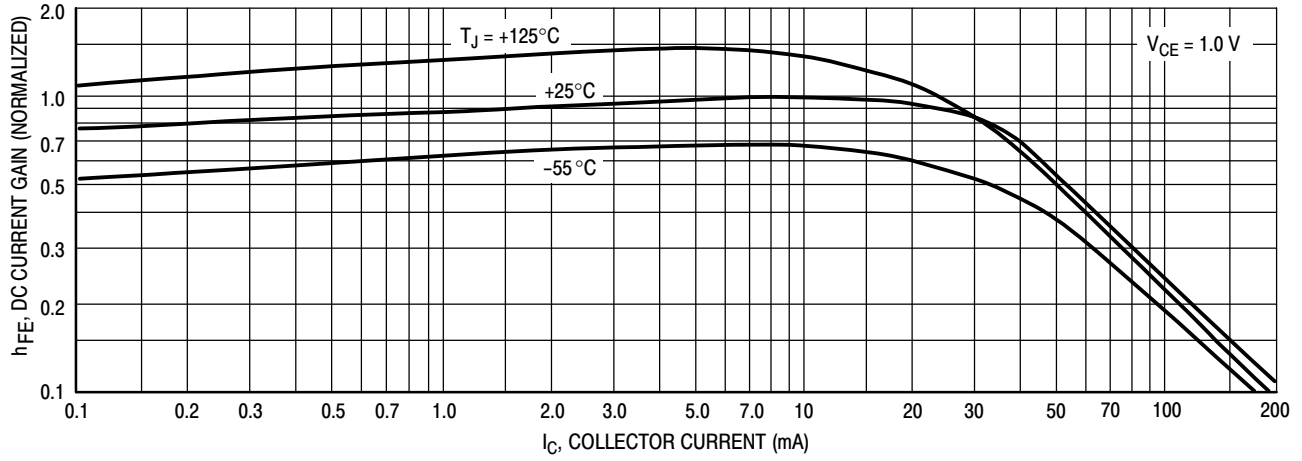


Figure 2. DC Current Gain

# NSTB1002DXV5T1G, NSTB1002DXV5T5G

## TYPICAL ELECTRICAL CHARACTERISTICS — NPN TRANSISTOR

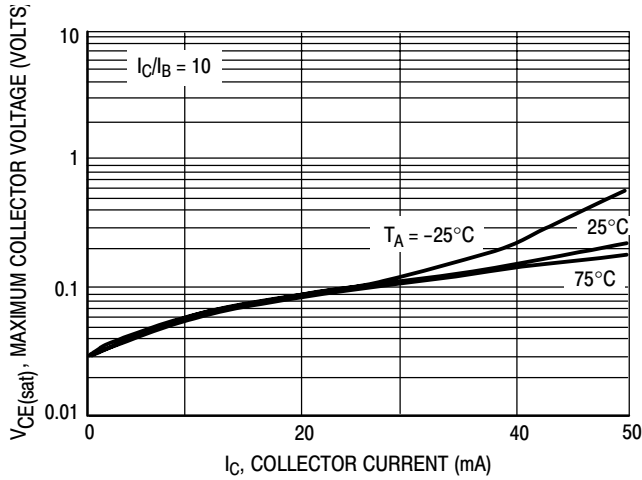


Figure 3.  $V_{CE(sat)}$  versus  $I_C$

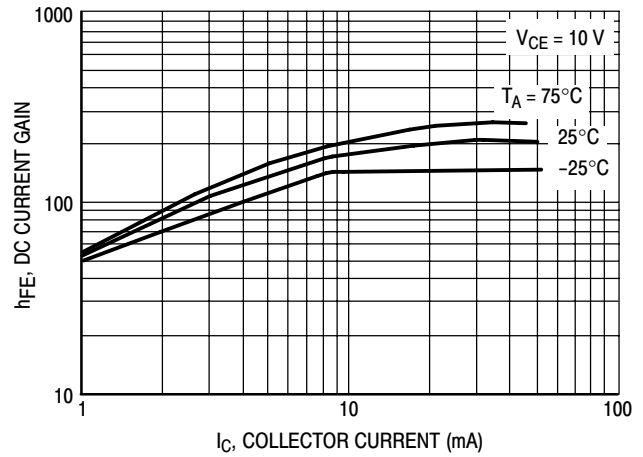


Figure 4. DC Current Gain

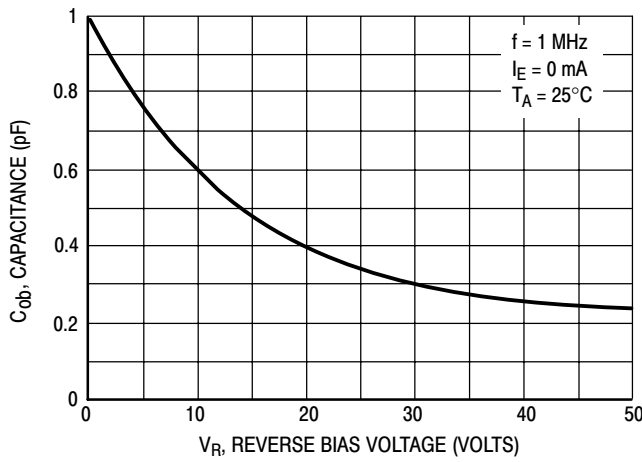


Figure 5. Output Capacitance

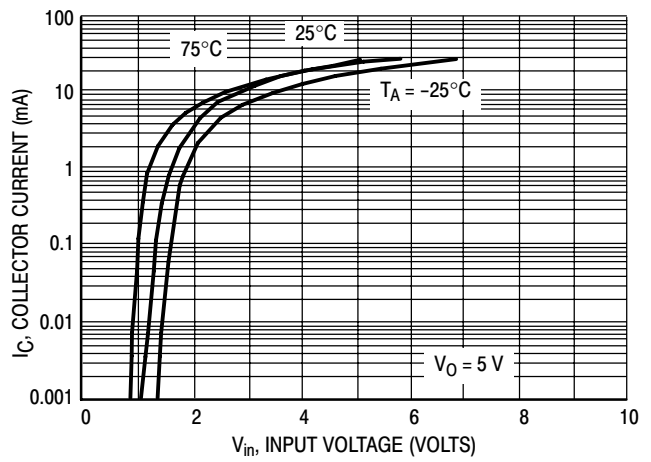


Figure 6. Output Current versus Input Voltage

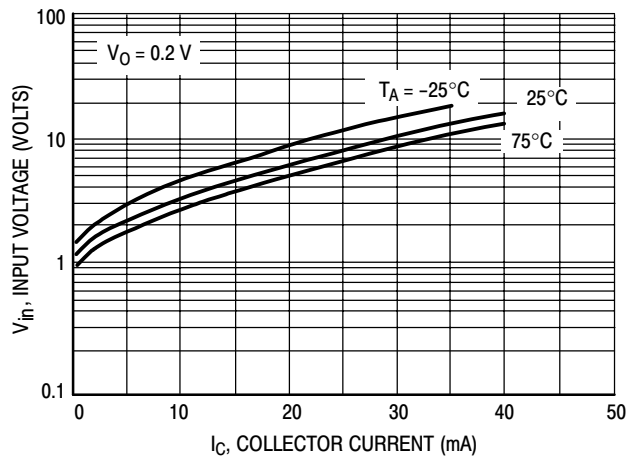


Figure 7. Input Voltage versus Output Current

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

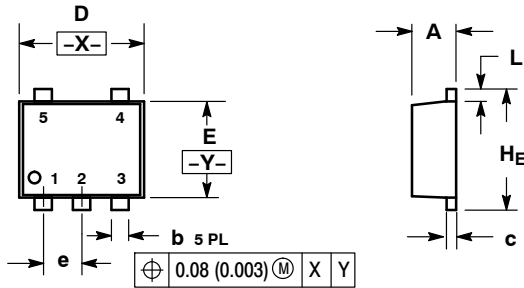
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SCALE 4:1

### SOT-553, 5 LEAD CASE 463B ISSUE C

DATE 20 MAR 2013

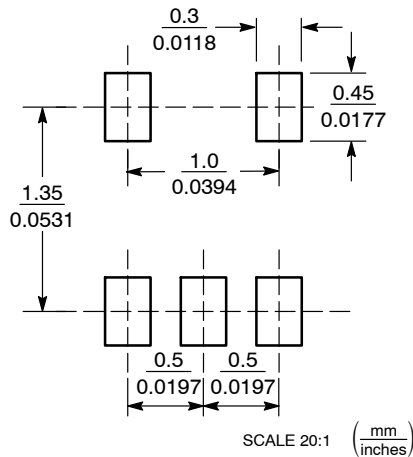


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.55	1.60	1.65	0.061	0.063	0.065
E	1.15	1.20	1.25	0.045	0.047	0.049
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.55	1.60	1.65	0.061	0.063	0.065

### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLE 1:**

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

**STYLE 2:**

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

**STYLE 3:**

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

**STYLE 4:**

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

**STYLE 5:**

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

**STYLE 6:**

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR 1
- 5. COLLECTOR 2/BASE 1

**STYLE 7:**

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

**STYLE 8:**

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER


**STYLE 9:**

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

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<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>SOT-553, 5 LEAD</b>	<b>PAGE 1 OF 2</b>



ISSUE	REVISION	DATE
A	ADDED STYLES 3-9. REQ. BY D. BARLOW	11 NOV 2003
B	ADDED NOMINAL VALUES AND UPDATED GENERIC MARKING DIAGRAM. REQ. BY HONG XIAO	27 MAY 2005
C	UPDATED DIMENSIONS D, E, AND HE. REQ. BY J. LETTERMAN.	20 MAR 2013

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