

# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

- Internal Look-Ahead Circuitry for Fast Counting
- Carry Output for N-Bit Cascading
- Fully Synchronous Operation for Counting

## description

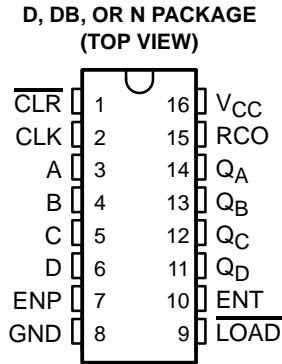
This synchronous, presettable, 4-bit binary counter has internal carry look-ahead circuitry for use in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that normally are associated with asynchronous (ripple-clock) counters. However, counting spikes can occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of CLK.

This counter is fully programmable. That is, it can be preset to any number between 0 and 15. Because presetting is synchronous, a low logic level at the load ( $\overline{LOAD}$ ) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of ENP and ENT.

The clear function is synchronous, and a low logic level at the clear ( $\overline{CLR}$ ) input sets all four of the flip-flop outputs to low after the next low-to-high transition of the clock, regardless of the levels of ENP and ENT. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications, without additional gating. This function is implemented by the ENP and ENT inputs and an RCO output. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. RCO, thus enabled, produces a high-logic-level pulse while the count is 15 (HHHH). The high-logic-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The SN74F163A features a fully independent clock circuit. Changes at ENP, ENT, or  $\overline{LOAD}$  that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the setup and hold times.



## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F163AN	SN74F163AN
		Tube	SN74F163AD	F163A
	SOIC – D	Tape and reel	SN74F163ADR	
		SSOP – DB	Tape and reel	SN74F163ADBR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

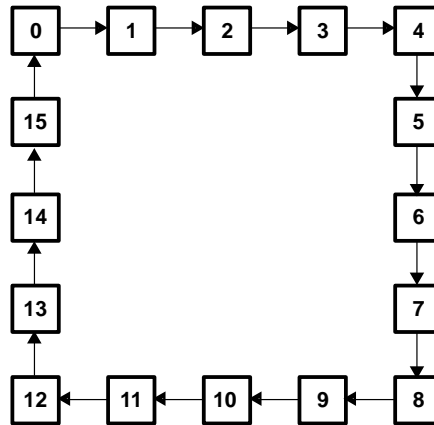
Copyright © 2001, Texas Instruments Incorporated

# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

---

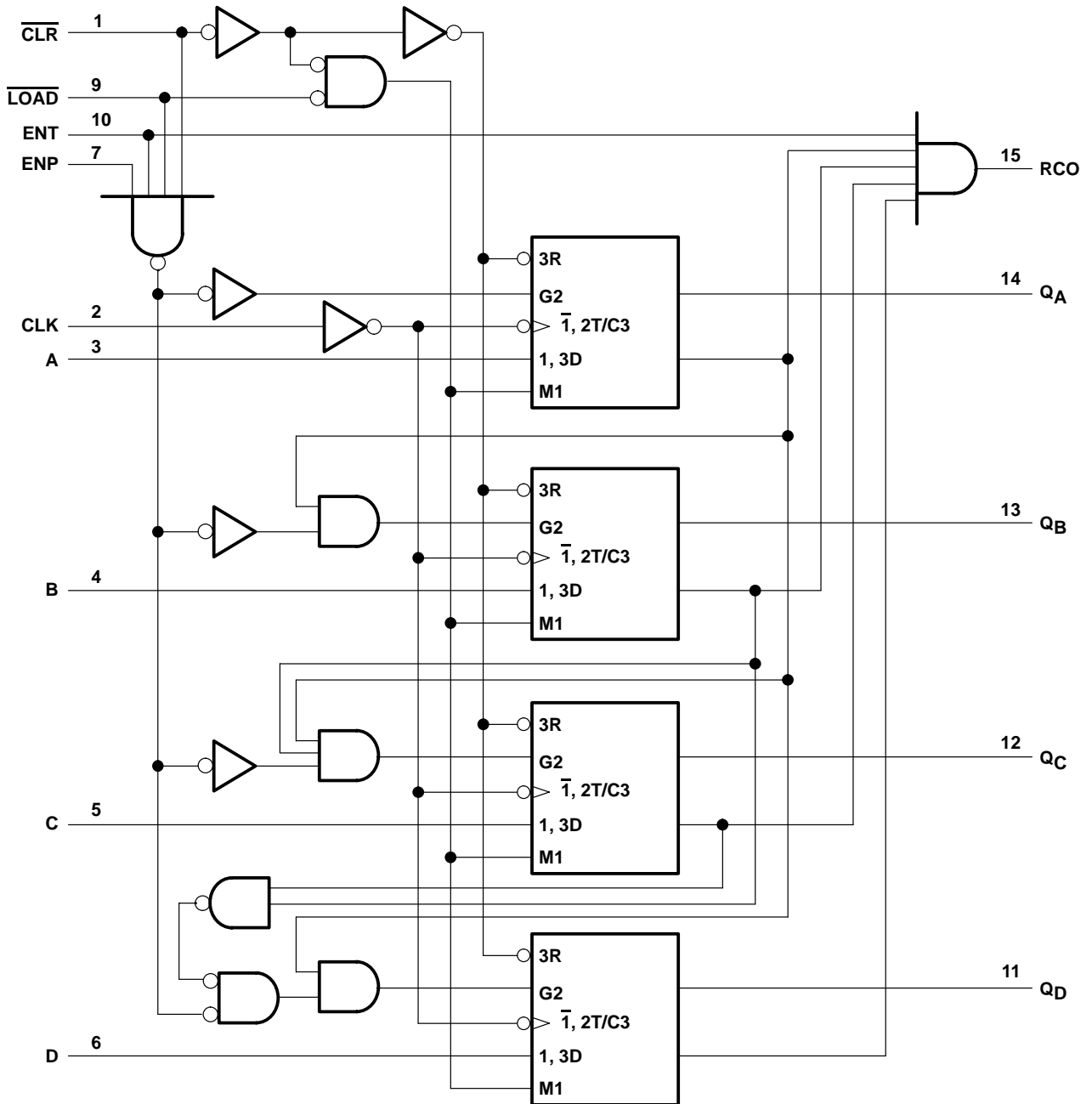
## state diagram



# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

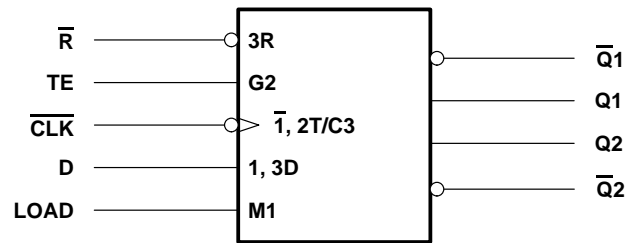
logic diagram (positive logic)



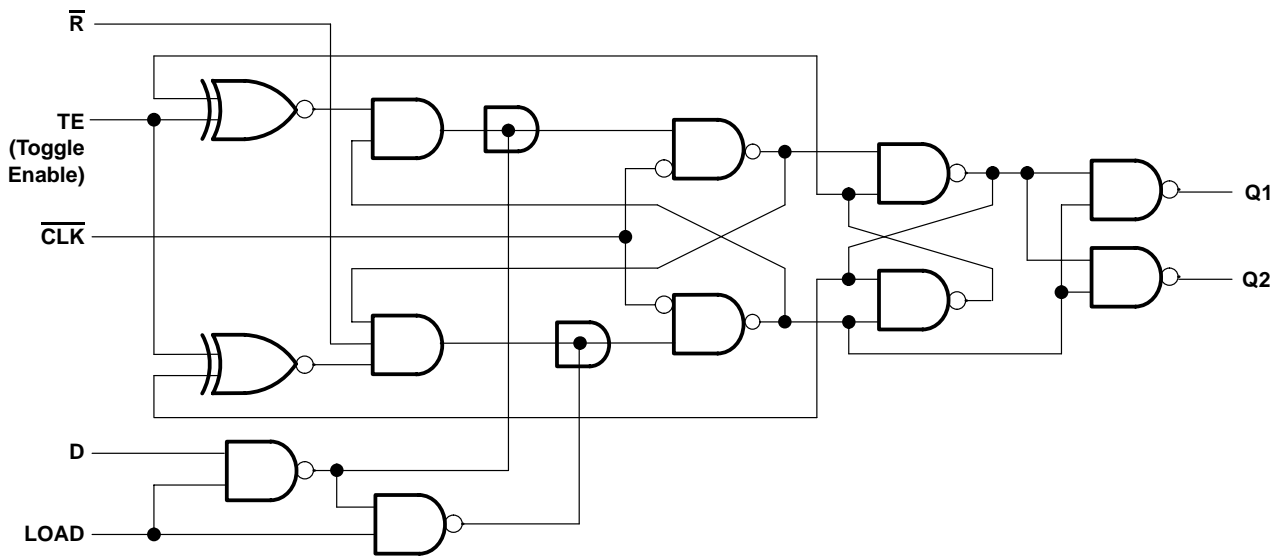
# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

## logic symbol, each flip-flop



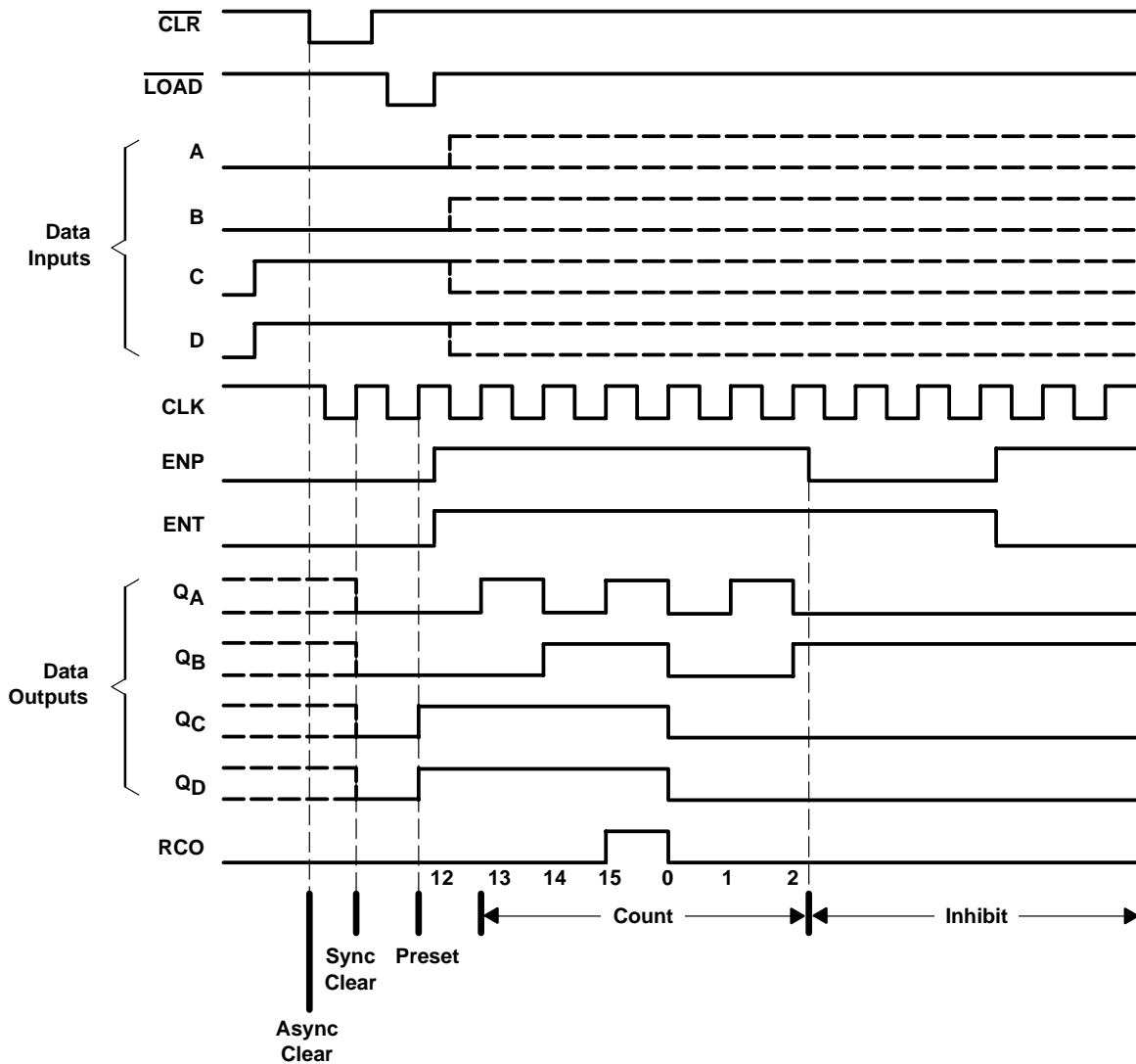
## logic diagram, each flip-flop (positive logic)



**typical clear, preset, count, and inhibit sequences**

The following timing sequence is illustrated below:

1. Clear outputs to zero
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit



# SN74F163A

## SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to $V_{CC}$
Current into any output in the low state	40 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{IK}$ Input clamp current			–18	mA
$I_{OH}$ High-level output current			–1	mA
$I_{OL}$ Low-level output current			20	mA
$T_A$ Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$V_{OH}$	$V_{CC} = 4.5$ V, $I_{OH} = -1$ mA	2.5	3.4		V
	$V_{CC} = 4.75$ V, $I_{OH} = -1$ mA	2.7			
$V_{OL}$	$V_{CC} = 4.5$ V, $I_{OL} = 20$ mA		0.3	0.5	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1	mA
$I_{IH}$	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20	µA
$I_{IL}$	$V_{CC} = 5.5$ V, $V_I = 0.5$ V	ENP, CLK, A, B, C, D		–0.6	mA
		ENT, LOAD		–1.2	
		CLR		–1.2	
$I_{OS}§$	$V_{CC} = 5.5$ V, $V_O = 0$	–60		–150	mA
$I_{CC}$	$V_{CC} = 5.5$ V		37	55	mA

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Clock frequency		0	100	0	90	MHz
t <sub>w</sub>	Pulse duration	CLK high or low (loading)	5		5		ns
		CLK (counting)	High	4	4		
			Low	6	7		
t <sub>su</sub>	Setup time	Data before CLK↑	High or low	5	5		ns
		LOAD and CLR before CLK↑	High	11	11.5		
			Low	8.5	9.5		
		ENP and ENT before CLK↑	High	11	11.5		
			Low	5	5		
t <sub>h</sub>	Hold time	Data after CLK↑	High or low	2	2		ns
		LOAD and CLR after CLK↑	High	2	2		
			Low	0	0		
		ENP and ENT after CLK↑	High or low	0	0		

### switching characteristics (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 PF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V TO 5.5 V, C <sub>L</sub> = 50 PF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN TO MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>			100	120		90		MHz
t <sub>PLH</sub>	CLK (LOAD high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
t <sub>PHL</sub>			2.7	7.1	10	2.7	11	
t <sub>PLH</sub>	CLK (LOAD low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
t <sub>PHL</sub>			3.2	5.6	8.5	3.2	9.5	
t <sub>PLH</sub>	CLK	RCO	4.2	9.6	14	4.2	15	ns
t <sub>PHL</sub>			4.2	9.6	14	4.2	15	
t <sub>PLH</sub>	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
t <sub>PHL</sub>			1.7	4.1	7.5	1.7	8.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

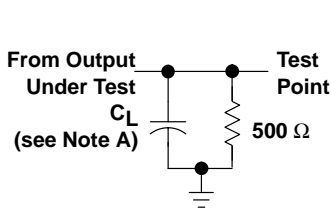
NOTE 4: Load circuits and waveforms are shown in Figure 1.



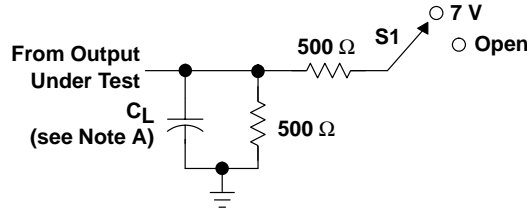
# SN74F163A SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS088A – MARCH 1987 – REVISED AUGUST 2001

## PARAMETER MEASUREMENT INFORMATION

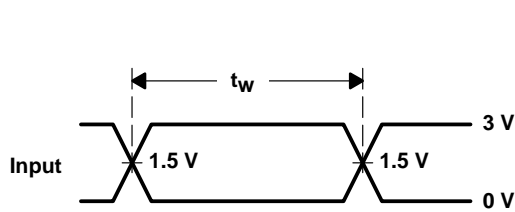


LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS

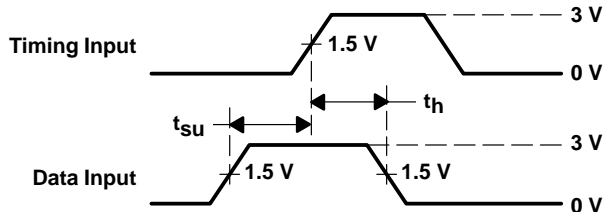


LOAD CIRCUIT FOR  
3-STATE AND OPEN-DRAIN OUTPUTS

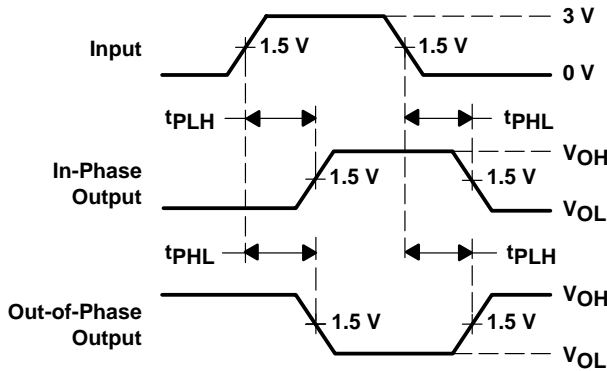
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open
Open Collector	7 V



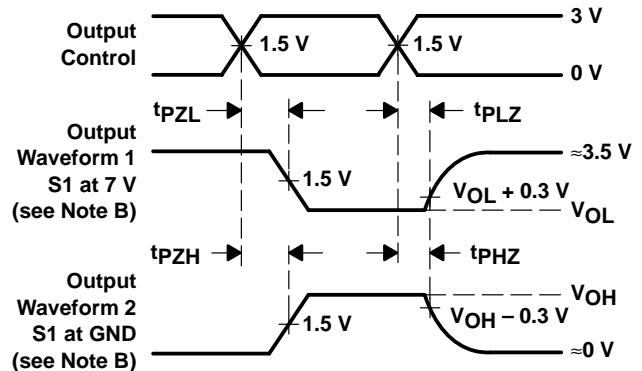
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.
  - The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F163AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F163A	<a href="#">Samples</a>
SN74F163ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F163A	<a href="#">Samples</a>
SN74F163AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F163AN	<a href="#">Samples</a>
SN74F163ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F163AN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F163ADR	SOIC	D	16	2500	340.5	336.1	32.0

**TUBE**




\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74F163AD	D	SOIC	16	40	507	8	3940	4.32
SN74F163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74F163ANE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated