CS5346

103-dB, 192-kHz, Stereo Audio ADC with 6:1 Input Mux

ADC Features

- Multi-bit Delta–Sigma Modulator
- 103 dB Dynamic Range
- -95 dB THD+N
- Stereo 6:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - ± 12 dB Gain, 0.5-dB Step Size
  - Zero-crossing, Click-free Transitions
- Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-noise Bias Supply
- Up to 192 kHz Sampling Rates
- Selectable 24-bit, Left-justified or I²S Serial Audio Interface Formats

System Features

- Power-down Mode
- +5 V Analog Power Supply, Nominal
- +3.3 V Digital Power Supply, Nominal
- Direct Interface with 3.3 V to 5 V Logic Levels
- Pin Compatible with CS5345 (*See Section 2 for details.)

General Description

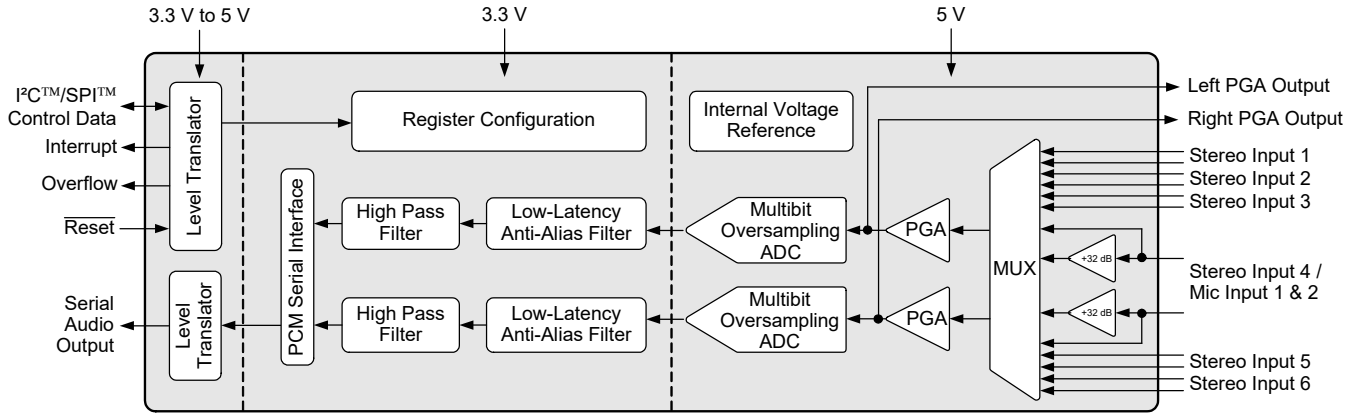
The CS5346 integrates an analog multiplexer, programmable gain amplifier, and stereo audio analog-to-digital converter. The CS5346 performs stereo analog-to-digital (A/D) conversion of 24-bit serial values at sample rates up to 192 kHz.

A 6:1 stereo input multiplexer is included for selecting between line-level and microphone-level inputs. The microphone input path includes a +32 dB gain stage and a low-noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain/attenuation of ±12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta-sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 8 kHz to 192 kHz in either Slave or Master Mode.

Integrated level translators allow easy interfacing between the CS5346 and other devices operating over a wide range of logic levels.

The CS5346 is available in a 48-pin LQFP package in Commercial (-40° to +85° C) grade. The CDB5346 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to “Ordering Information” on page 38 for complete details.



Preliminary Product Information | This document contains information for a product under development. Cirrus Logic reserves the right to modify this product without notice.

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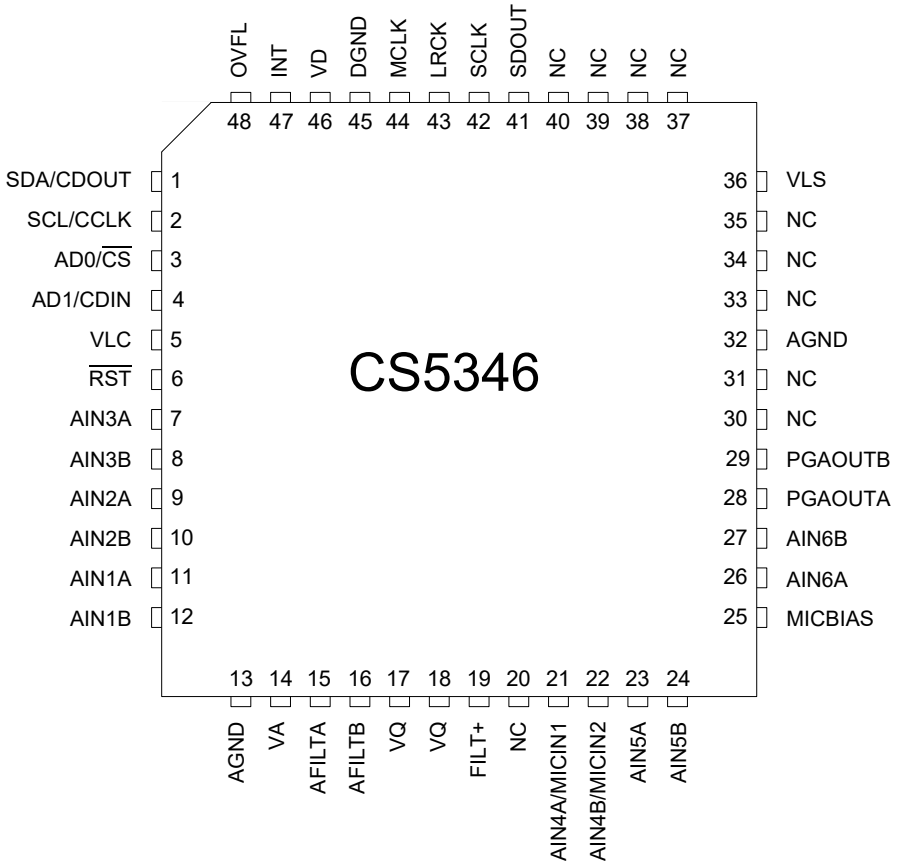
1. PIN DESCRIPTIONS - CS5346

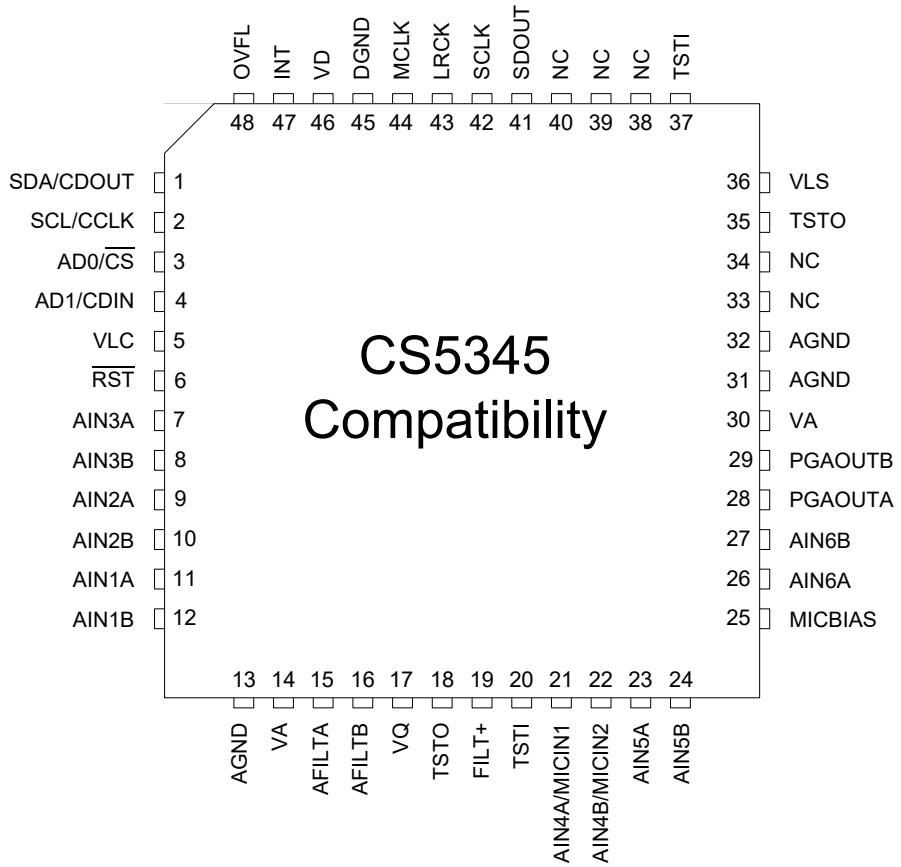


Pin Name	#	Pin Description
SDA/CDOUT	1	**Serial Control Data** (*Input*/*Output*) - SDA is a data I/O in I²C® Mode. CDOUT is the output data line for the control port interface in SPI™ Mode.
SCL/CCLK	2	**Serial Control Port Clock** (*Input*) - Serial clock for the serial control port.
AD0/$\overline{CS}$	3	**Address Bit 0 (I²C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I²C Mode; $\overline{CS}$ is the chip-select signal for SPI format.
AD1/CDIN	4	**Address Bit 1 (I²C) / Serial Control Data Input (SPI)** *(Input)* - AD1 is a chip address pin in I²C Mode; CDIN is the input data line for the control port interface in SPI Mode.
VLC	5	**Control Port Power** (*Input*) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{RST}$	6	**Reset** (*Input*) - The device enters a low-power mode when this pin is driven low.
AIN3A AIN3B	7 8	**Stereo Analog Input 3** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.
AIN2A AIN2B	9 10	**Stereo Analog Input 2** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.

AIN1A AIN1B	11 12	**Stereo Analog Input 1** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.
AGND	13	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VA	14	**Analog Power** *(Input)* - Positive power for the internal analog section.
AFILTA	15	**Anti-alias Filter Connection** (*Output*) - Antialias filter connection for the channel A ADC input.
AFILTB	16	**Anti-alias Filter Connection** (*Output*) - Antialias filter connection for the channel B ADC input.
VQ	17 18	**Quiescent Voltage** (*Output*) - Filter connection for the internal quiescent reference voltage.
FILT+	19	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
NC	20	**No Connect** - This pin is not connected internally and should be tied to ground to minimize any potential coupling effects.
AIN4A/MICIN1 AIN4B/MICIN2	21 22	**Stereo Analog Input 4 / Microphone Input 1 & 2** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.
AIN5A AIN5B	23 24	**Stereo Analog Input 5** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.
MICBIAS	25	**Microphone Bias Supply** (*Output*) - Low-noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics specification table.
AIN6A AIN6B	26 27	**Stereo Analog Input 6** (*Input*) - The full-scale level is specified in the Analog Characteristics specification table.
PGAOUTA PGAOUTB	28 29	**PGA Analog Audio Output** (*Output*) - Either an analog output from the PGA block or high impedance. See "PGAOut Source Select (Bit 6)" on page 30.
NC	30 31	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
AGND	32	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
NC	33 34 35	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
VLS	36	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
NC	37 38 39 40	**No Connect** - These pins are not connected internally and should be tied to ground to minimize any potential coupling effects.
SDOUT	41	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK	42	**Serial Clock** *(Input/Output)* - Serial clock for the serial audio interface.
LRCK	43	**Left Right Clock** *(Input/Output)* - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	44	**Master Clock** (*Input*) - Clock source for the ADC's delta-sigma modulators.
DGND	45	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	46	**Digital Power** (*Input*) - Positive power for the internal digital section.
INT	47	**Interrupt** (*Output*) - Indicates an interrupt condition has occurred.
OVFL	48	**Overflow** (*Output*) - Indicates an ADC overflow condition is present.

2. PIN COMPATIBILITY - CS5345/CS5346 DIFFERENCES

The CS5346 is pin compatible with the CS5345 and is a drop in replacement for CS5345 applications where VA = 5 V, VD = 3.3 V, VLS ≥ 3.3 V, and VLC ≥ 3.3 V. The pinout diagram and table below show the requirements for the remaining pins when replacing the CS5345 in these designs with a CS5346.



#	CS5345 Pin Name	CS5346 Pin Name	CS5346 Connection for Compatibility
5	VLC	VLC	**Control Port Power** (*Input*) -Limited to nominal 5 or 3.3 V.
14	VA	VA	**Analog Power** *(Input)* - Limited to nominal 5 V.
18	TSTO	VQ	This pin must be left unconnected.
20	TSTI	NC	This pin should be tied to ground.
30	VA	NC	This pin may be connected to the analog supply voltage. The decoupling capacitor for the CS5345 is not required.
31	AGND	NC	This pin should be connected to ground.
35	TSTO	NC	This pin may be left unconnected.
36	VLS	VLS	**Serial Audio Interface Power** (*Input*) - Limited to nominal 5 or 3.3 V.
37	TSTI	NC	This pin should be tied to ground.
46	VD	VD	**Digital Power** (*Input*) - Limited to nominal 3.3 V

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

AGND = DGND = 0 V; All voltages with respect to ground.

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	4.75	5.0	5.25	V
	Digital	VD	3.13	3.3	3.47	V
	Logic - Serial Port	VLS	3.13	3.3	5.25	V
	Logic - Control Port	VLC	3.13	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	Commercial	T_A	-40	-	+85	°C

ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V All voltages with respect to ground. (Note 1)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Analog	VA	-0.3	+6.0	V
	Digital	VD	-0.3	+3.63	V
	Logic - Serial Port	VLS	-0.3	+6.0	V
	Logic - Control Port	VLC	-0.3	+6.0	V
Input Current	(Note 2)	I_{in}	-	±10	mA
Analog Input Voltage		V_{INA}	AGND-0.3	VA+0.3	V
Digital Input Voltage	Logic - Serial Port	V_{IND-S}	-0.3	VLS+0.3	V
	Logic - Control Port	V_{IND-C}	-0.3	VLC+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-50	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): VA = 5 V; VD = VLS = VLC = 3.3 V; AGND = DGND = 0 V; T_A = +25° C; Input test signal: 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz; Fs = 48/96/192 kHz; PGA gain = 0 dB; All connections as shown in Figure 7 on page 18.

Parameter			Symbol	Min	Typ	Max	Unit
Analog-to-Digital Converter Characteristics							
Dynamic Range (Line Level Inputs)							
		A-weighted		97	103	-	dB
		unweighted		94	100	-	dB
(Note 3)	40 kHz bandwidth	unweighted		-	98	-	dB
Total Harmonic Distortion + Noise (Line Level Inputs)		(Note 4)					
		-1 dB		-	-95	-89	dB
		-20 dB	THD+N	-	-80	-	dB
		-60 dB		-	-40	-	dB
(Note 3)	40 kHz bandwidth	-1 dB		-	-92	-	dB
Dynamic Range (Mic Level Inputs)							
		A-weighted		77	83	-	dB
(Note 3)		unweighted		74	80	-	dB
Total Harmonic Distortion + Noise (Mic Level Inputs)		(Note 4)					
		-1 dB	THD+N	-	-80	-74	dB
		-20 dB		-	-60	-	dB
(Note 3)		-60 dB		-	-20	-	dB
Interchannel Isolation		(Line Level Inputs)		-	90	-	dB
		(Mic Level Inputs)		-	80	-	dB
A/D Full-scale Input Voltage				0.51*VA	0.57*VA	0.63*VA	V_{pp}
Gain Error				-	-	±10	%
Interchannel Gain Mismatch				-	0.1	-	dB
Microphone - Level Input Characteristics							
Preamplifier Gain				31	32	33	dB
				35.5	40	44.7	V/V
Interchannel Gain Mismatch				-	0.1	-	dB
Input Impedance		(Note 5)		-	60	-	kΩ

3. Valid for Double- and Quad-Speed Modes only.
4. Referred to the typical A/D full-scale input voltage
5. Valid when the microphone-level inputs are selected.

ANALOG CHARACTERISTICS CONT.

Parameter	Symbol	Min	Typ	Max	Unit
Line-Level Input and Programmable Gain Amplifier					
Gain Range		- 12 -4	- -	+ 12 +4	dB V/V
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB
Maximum Input Level		-	-	0.85*VA	V_{pp}
Input Impedance Selected inputs Un-selected inputs		 28.8 -	 36 -	 43.2 38	 kΩ kΩ
Selected Interchannel Input Impedance Mismatch		-	5	-	%
Analog Outputs					
Dynamic Range (Line Level Inputs) A-weighted unweighted		 98 95	 104 101	 - -	 dB dB
Total Harmonic Distortion + Noise (Line Level Inputs) (Note 6) -1 dB -20 dB -60 dB	THD+N	 - - -	 -80 -81 -41	 -74 - -	 dB dB dB
Dynamic Range (Mic Level Inputs) A-weighted unweighted		 77 74	 83 80	 - -	 dB dB
Total Harmonic Distortion + Noise (Mic Level Inputs) (Note 6) -1 dB -20 dB -60 dB	THD+N	 - - -	 -74 -60 -20	 -68 - -	 dB dB dB
Frequency Response 10 Hz to 20 kHz		-0.1dB	-	+0.1dB	dB
Analog In to Analog Out Phase Shift		-	180	-	deg
DC Current draw from a PGAOUT pin	I_{OUT}	-	-	1	µA
AC-Load Resistance	R_L	100	-	-	kΩ
Load Capacitance	C_L	-	-	20	pF

6. Referred to the typical A/D Full-Scale Input Voltage.

DIGITAL FILTER CHARACTERISTICS

Parameter (Note 7)			Symbol	Min	Typ	Max	Unit
Single-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.035	dB
Stopband				0.5688	-	-	Fs
Stopband Attenuation				70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	12/Fs	-	s
Double-Speed Mode							
Passband	(-0.1 dB)			0	-	0.4896	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5604	-	-	Fs
Stopband Attenuation				69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	9/Fs	-	s
Quad-Speed Mode							
Passband	(-0.1 dB)			0	-	0.2604	Fs
Passband Ripple				-	-	0.025	dB
Stopband				0.5000	-	-	Fs
Stopband Attenuation				60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)			t_{gd}	-	5/Fs	-	s
High-Pass Filter Characteristics							
Frequency Response	-3.0 dB			-	1	-	Hz
	-0.13 dB	(Note 8)			20	-	Hz
Phase Deviation	@ 20 Hz	(Note 8)		-	10	-	Deg
Passband Ripple				-	-	0	dB
Filter Settling Time					10^5/Fs		s

7. Response is clock-dependent and will scale with Fs. Note that the response plots (Figures 17 to 28) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
8. Response shown is for Fs = 48 kHz.

DC ELECTRICAL CHARACTERISTICS

AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz; Master Mode.

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	41	50	mA
(Normal Operation)	VD, VLS, VLC = 3.3 V	I_D	-	23	28	mA
Power Supply Current	VA = 5 V	I_A	-	0.50	-	mA
(Power-Down Mode) (Note 9)	VLS, VLC, VD = 3.3 V	I_D	-	0.54	-	mA
Power Consumption						
(Normal Operation)	VA = 5 V	-	-	205	250	mW
	VD, VLS, VLC = 3.3 V	-	-	76	93	mW
(Power-Down Mode)	VA = 5V; VD, VLS, VLC = 3.3 V	-	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 10)	PSRR	-	55	-	dB
VQ Characteristics						
Quiescent Voltage		VQ	-	0.5 x VA	-	VDC
Maximum DC Current from VQ		I_Q	-	1	-	µA
VQ Output Impedance		Z_Q	-	23	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		I_{MB}	-	-	2	mA

9. Power-Down Mode is defines as $\overline{RST}$ = Low with all clock and data lines held static and no analog input.
10. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): AGND = DGND = 0 V; VLS = VLC = 3.3 V.

Parameters (Note 11)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage						
	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.3xVLS	V
	Control Port	V_{IL}	-	-	0.3xVLC	V
High-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
Low-Level Output Voltage at I_o = 2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	1	-	pF
Minimum OVFL Active Time			$\frac{10^6}{LRCK}$	-	-	µs

11. Serial Port signals include: MCLK, SCLK, LRCK, SDOUT.
Control Port signals include: SCL/CCLK, SDA/CDOUT, AD0/$\overline{CS}$, AD1/CDIN, $\overline{RST}$, INT, OVFL.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

Logic '0' = DGND = AGND = 0 V; Logic '1' = VLS, C_L = 20 pF. (Note 12)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single-Speed Mode	Fs	8	-	50	kHz
	Double-Speed Mode	Fs	50	-	100	kHz
	Quad-Speed Mode	Fs	100	-	200	kHz
MCLK Specifications						
MCLK Frequency		fmclk	2.048	-	51.200	MHz
MCLK Input Pulse Width High/Low		tclkhl	8	-	-	ns
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	36	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period						
	Single-Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
	Double-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
	Quad-Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK Pulse Width High		t_{sclkh}	30	-	-	ns
SCLK Pulse Width Low		t_{sclkl}	48	-	-	ns
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	0	-	36	ns

12. See Figure 1 and Figure 2 on page 15.

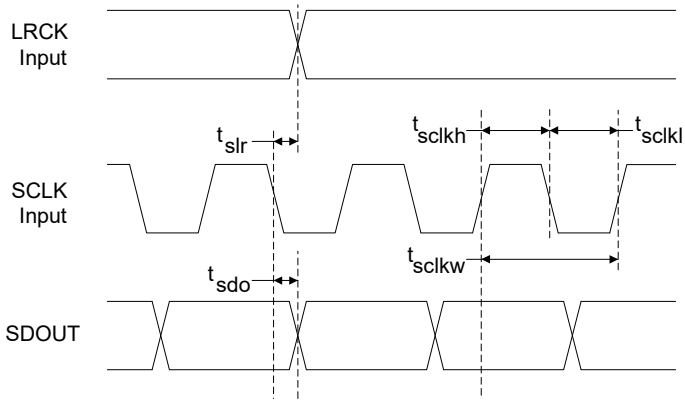


Figure 1. Master Mode Serial Audio Port Timing

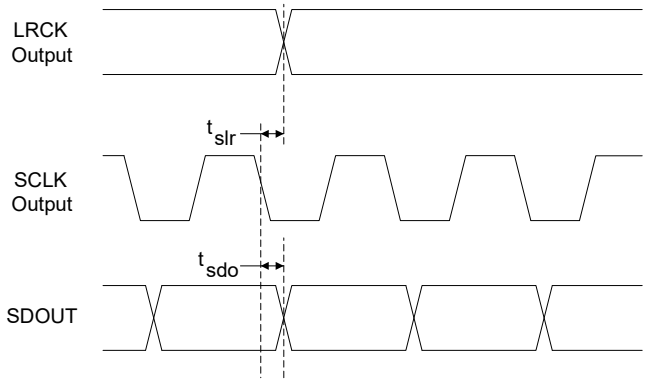


Figure 2. Slave Mode Serial Audio Port Timing

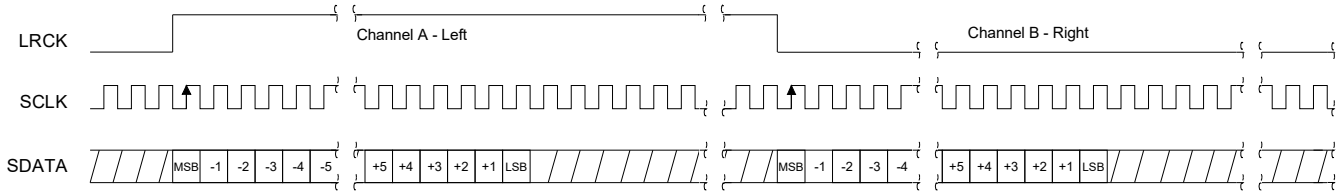


Figure 3. Format 0, 24-Bit Data Left-Justified

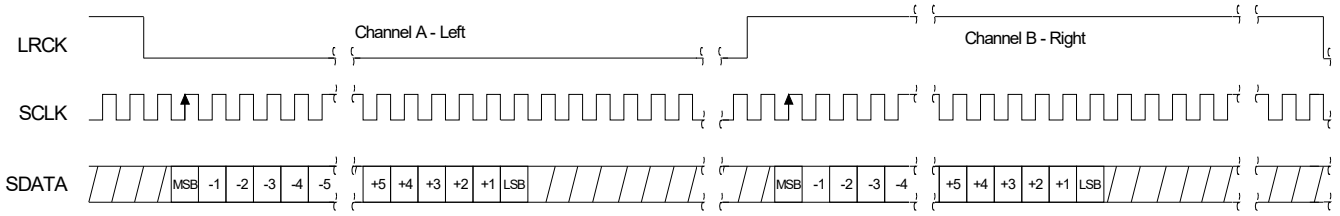


Figure 4. Format 1, 24-Bit Data I²S

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, C_L = 30 pF.

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{\text{RST}}$ Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 13)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL and SDA	t_{rc}, t_{rd}	-	1	µs
Fall Time SCL and SDA	t_{fc}, t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

13. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

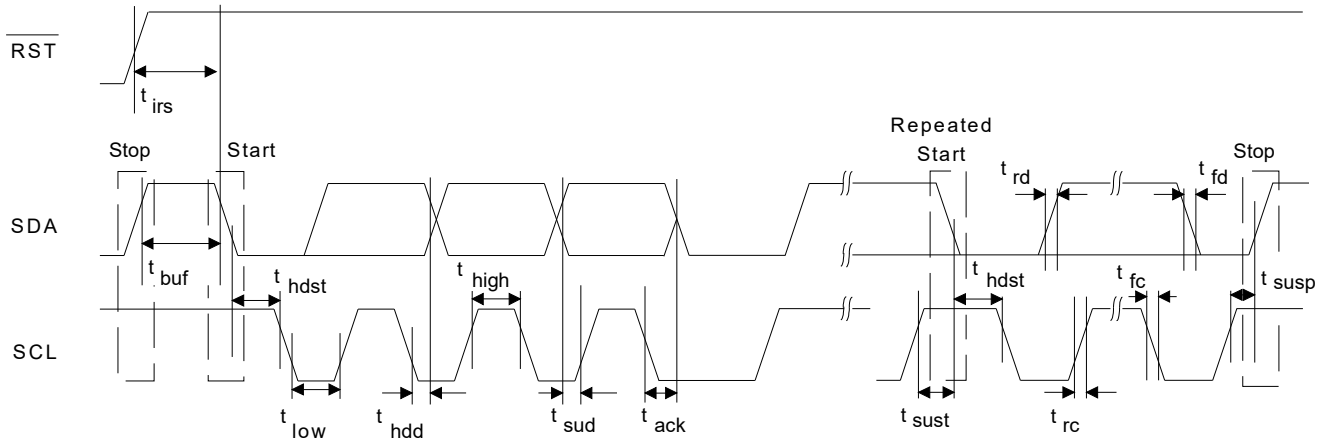


Figure 5. Control Port Timing - I²C Format

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI FORMAT

Inputs: Logic 0 = DGND = AGND = 0 V, Logic 1 = VLC, C_L = 30 pF.

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	-	6.0	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 14)	t_{dh}	15	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	50	ns
Rise Time of CDOUT		t_{r1}	-	25	ns
Fall Time of CDOUT		t_{f1}	-	25	ns
Rise Time of CCLK and CDIN	(Note 15)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 15)	t_{f2}	-	100	ns

14. Data must be held for sufficient time to bridge the transition time of CCLK.
15. For f_{sck} <1 MHz.

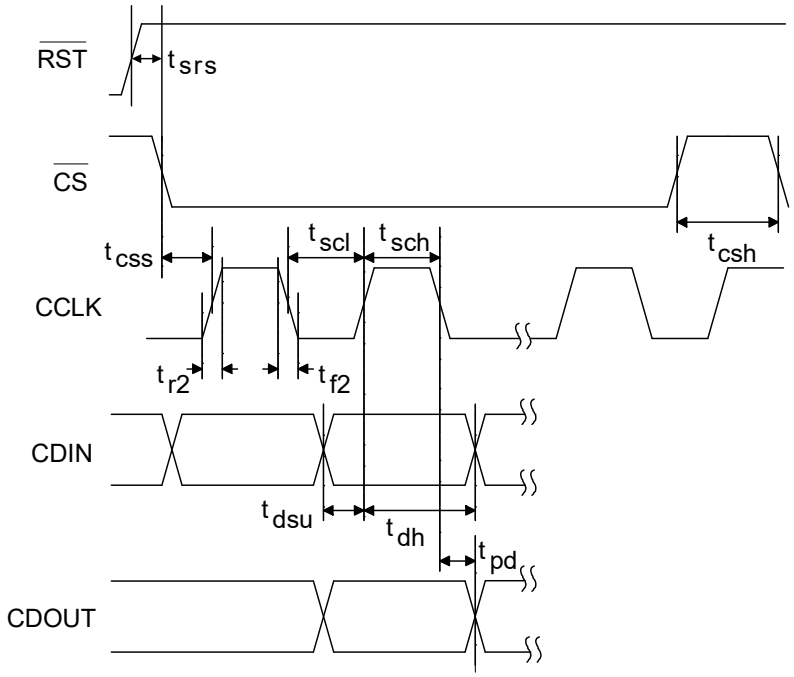


Figure 6. Control Port Timing - SPI Format

4. TYPICAL CONNECTION DIAGRAM

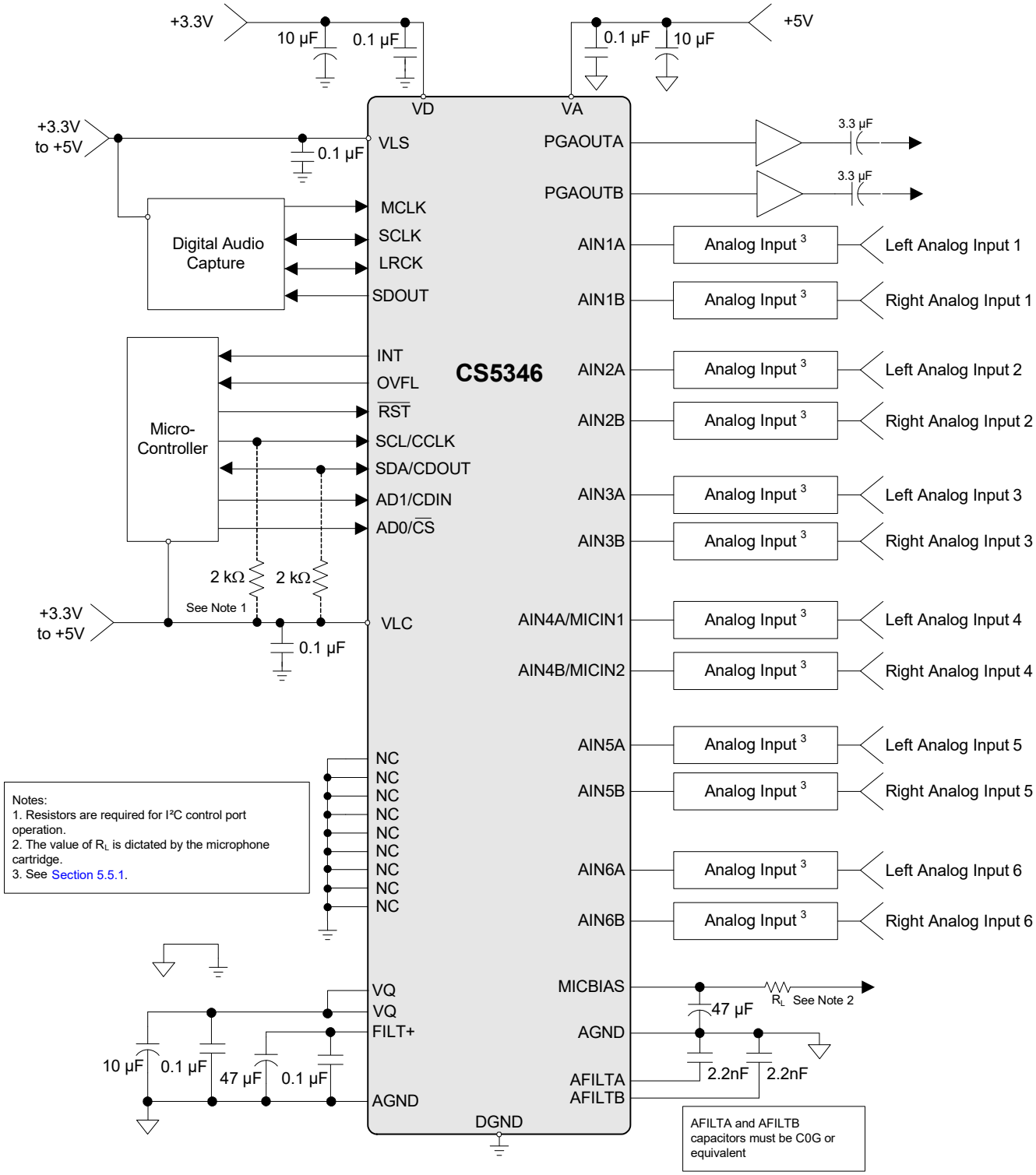


Figure 7. Typical Connection Diagram

5. APPLICATIONS

5.1 Recommended Power-Up Sequence

1. Hold $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3. The desired register settings can be loaded while the PDN bit remains set.
4. Clear the PDN bit to initiate the power-up sequence.

5.2 System Clocking

The CS5346 will operate at sampling frequencies from 8 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1.

Mode	Sampling Frequency
Single-Speed	8-50 kHz
Double-Speed	50-100 kHz
Quad-Speed	100-200 kHz

Table 1. Speed Modes

5.2.1 Master Clock

MCLK/LRCK must maintain an integer ratio as shown in Table 2. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked out of the device. The FM bits (See "Functional Mode (Bits 7:6)" on page 29.) and the MCLK Freq bits (See "MCLK Frequency - Address 05h" on page 30.) configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	* 64x	* 96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	**QSM**					**DSM**		**SSM**	
*** Only available in master mode.**									

Table 2. Common Clock Frequencies

5.2.2 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to Fs and SCLK equal to 64 x Fs as shown in Figure 8.

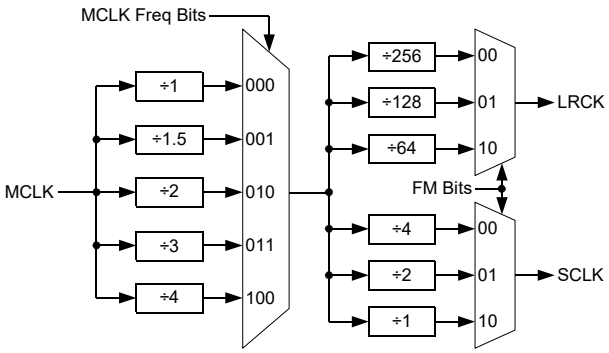


Figure 8. Master Mode Clocking

5.2.3 Slave Mode

In Slave Mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 128x, 64x or 48x Fs, depending on the desired speed mode. Refer to Table 3 for required clock ratios.

	Single-Speed	Double-Speed	Quad-Speed
SCLK/LRCK Ratio	48x, 64x, 128x	48x, 64x	48x, 64x

Table 3. Slave Mode Serial Bit Clock Ratios

5.3 High-Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS5346, a small DC offset may be driven into the A/D converter. The CS5346 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit (See "High-Pass Filter Freeze (Bit 1)" on page 29.) is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS5346 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics section for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5346.

5.4 Analog Input Multiplexer, PGA, and Mic Gain

The CS5346 contains a stereo 6-to-1 analog input multiplexer followed by a programmable gain amplifier (PGA). The input multiplexer can select one of six possible stereo analog input sources and route it to the PGA. Analog inputs 4A and 4B are able to insert a +32 dB (+40x) gain stage before the input multiplexer, allowing them to be used for microphone-level signals without the need for any external gain. The PGA stage provides ±12 dB (±4x) adjustment in 0.5 dB steps. Figure 9 shows the architecture of the input multiplexer, PGA, and microphone gain stages.

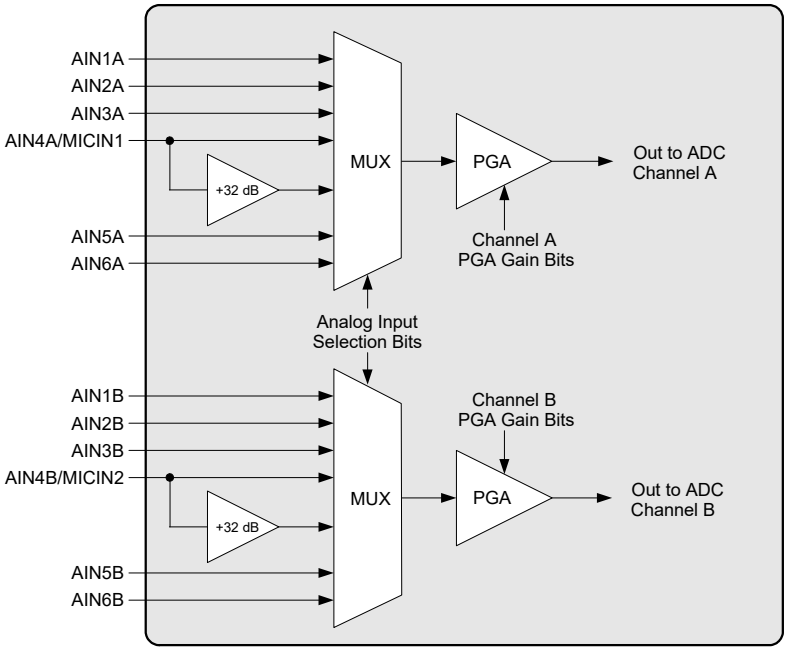


Figure 9. Analog Input Architecture

The ""Analog Input Selection (Bits 2:0)" on page 32" outlines the bit settings necessary to control the input multiplexer and mic gain. "Channel B PGA Control - Address 07h" on page 30 and "Channel A PGA Control - Address 08h" on page 31 outline the register settings necessary to control the PGA. By default, line-level input 1 is selected, and the PGA is set to 0 dB.

5.5 Input Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are (n × 6.144 MHz) the digital passband frequency, where n=0,1,2,... Refer to the Typical Connection Diagram for the recommended analog input circuit that will attenuate noise energy at 6.144 MHz. The use of capacitors which have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity. Any unused analog input pairs should be left unconnected.

5.5.1 Analog Input Configuration for 1 V_{RMS} Input Levels

The CS5346 PGA, excluding the input multiplexer, is shown in Figure 10 with nominal component values. Interfacing to this circuit is a relatively simple matter and several options are available. The simplest option is shown in Figure 11. However, it may be advantageous in some applications to provide a low-pass filter prior to the PGA to prevent radio frequency interference within the amplifier. The circuit shown in Figure 12

demonstrates a simple solution. The 1800 pF capacitors in the low-pass filter should be C0G or equivalent to avoid distortion issues

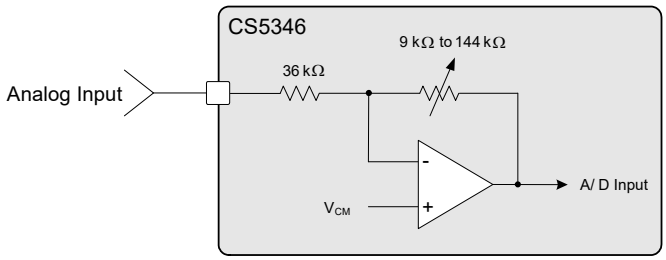


Figure 10. CS5346 PGA

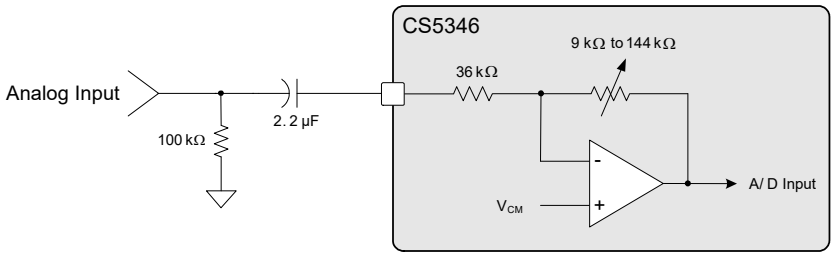


Figure 11. 1 V_{RMS} Input Circuit

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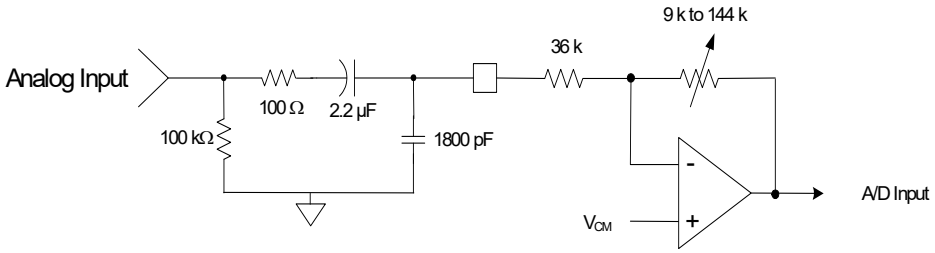


Figure 12. 1 V_{RMS} Input Circuit with RF Filtering

5.5.2 Analog Input Configuration for 2 V_{RMS} Input Levels

The CS5346 can also be easily configured to support an external 2 V_{RMS} input signal, as shown in Figure 13. In this configuration, the 2 V_{RMS} input signal is attenuated to 1.5 V_{RMS} at the analog input with the external 12 kΩ resistor and the input impedance to the network is increased to 48 kΩ. The PGA gain must also be configured to attenuate the 1.5 V_{RMS} at the input pin to the 1.0 V_{RMS} maximum A/D input level to prevent clipping in the ADC.

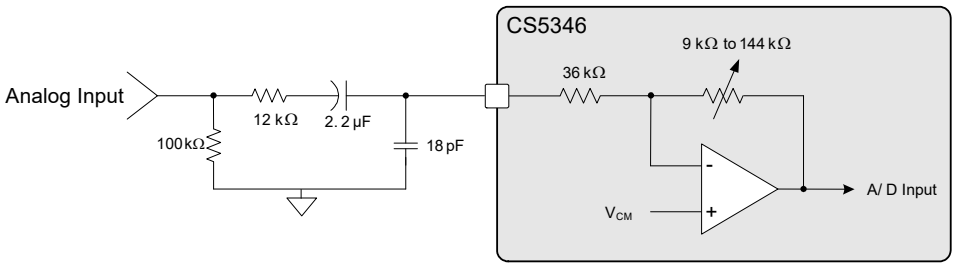


Figure 13. 2 V_{RMS} Input Circuit

5.6 PGA Auxiliary Analog Output

The CS5346 includes an auxiliary analog output through the PGAOUT pins. These pins can be configured to output the analog input to the ADC as selected by the input MUX and gained or attenuated with the PGA, or alternatively, they may be set to high impedance. See the "PGAOut Source Select (Bit 6)" on page 30 for information on configuring the PGA auxiliary analog output.

The PGA auxiliary analog output can source very little current. As current from the PGAOUT pins increases, distortion will increase. For this reason, a high-input impedance buffer must be used on the PGAOUT pins to achieve full performance. An example buffer for PGAOUT is provided on the CDB5346 for reference. Refer to the table in "DC Electrical Characteristics" on page 12 for acceptable loading conditions.

5.7 Control Port Description and Timing

The control port is used to access the registers, allowing the CS5346 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has two modes: SPI and I²C, with the CS5346 acting as a slave device. SPI Mode is selected if there is a high-to-low transition on the AD0/$\overline{CS}$ pin, after the $\overline{RST}$ pin has been brought high. I²C Mode is selected by connecting the AD0/$\overline{CS}$ pin through a resistor to VLC or DGND, thereby permanently selecting the desired AD0 bit address state.

5.7.1 SPI Mode

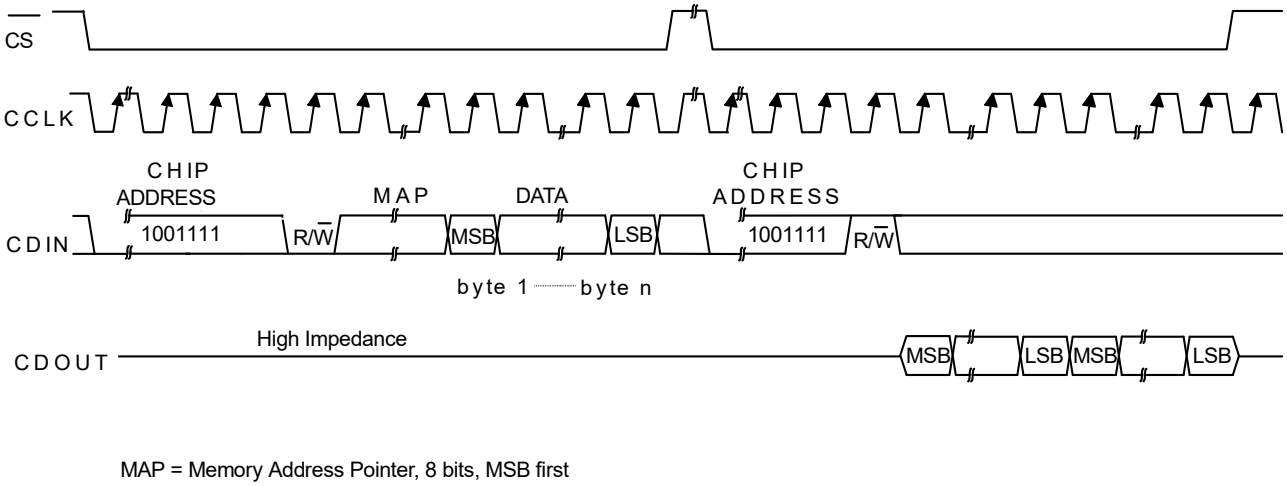
In SPI Mode, $\overline{CS}$ is the chip-select signal; CCLK is the control port bit clock (input into the CS5346 from the microcontroller); CDIN is the input data line from the microcontroller; CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

Figure 14 shows the operation of the control port in SPI Mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001111. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data that will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. To begin a read, bring $\overline{CS}$ low, send out the chip ad-

dress and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high-impedance state).

For both read and write cycles, the memory address pointer will automatically increment following each data byte in order to facilitate block reads and writes of successive registers.



MAP = Memory Address Pointer, 8 bits, MSB first

Figure 14. Control Port Timing in SPI Mode

5.7.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the two least-significant bits of the chip address and should be connected through a resistor to VLC or DGND as desired. The state of the pins is sensed while the CS5346 is being reset.

The signal timings for a read and write cycle are shown in Figure 15 and Figure 16. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS5346 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 5 bits of the 7-bit address field are fixed at 10011. To communicate with a CS5346, the chip address field, which is the first byte sent to the CS5346, should match 10011 followed by the settings of the AD1 and AD0. The 8th bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Following each data byte, the memory address pointer will automatically increment to facilitate block reads and writes of successive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS5346 after each input byte is read, and is input to the CS5346 from the microcontroller after each transmitted byte.

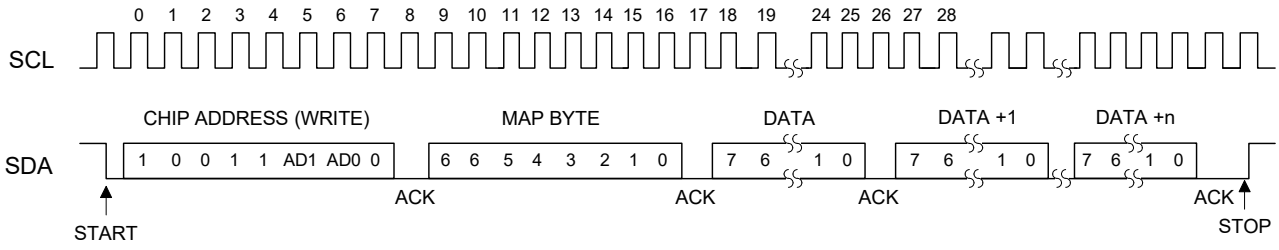


Figure 15. Control Port Timing, I²C Write

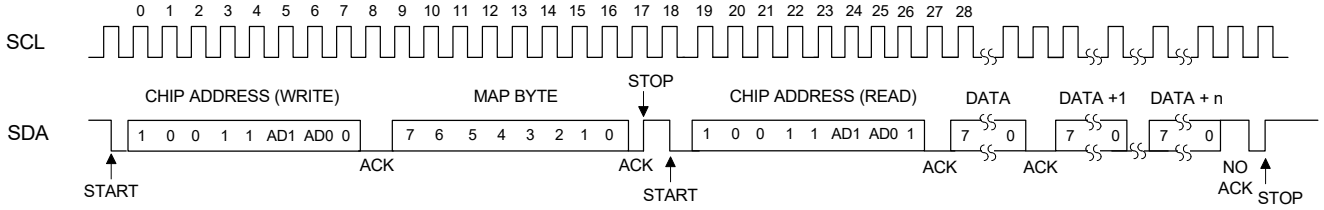


Figure 16. Control Port Timing, I²C Read

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 16, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

- Send start condition.
- Send 10011xx0 (chip address & write operation).
- Receive acknowledge bit.
- Send MAP byte.
- Receive acknowledge bit.
- Send stop condition, aborting write.
- Send start condition.
- Send 10011xx1(chip address & read operation).
- Receive acknowledge bit.
- Receive byte, contents of selected register.
- Send acknowledge bit.
- Send stop condition.

5.8 Interrupts and Overflow

The CS5346 has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may function as either an active high CMOS driver or an active-low, open-drain driver (see “Active High/Low (Bit 0)” on page 35). When configured as active low open-drain, the INT pin has no active pull-up transistor, allowing it to be used for wired-OR hook-ups with multiple peripherals connected to the microcontroller interrupt input pin. In this configuration, an external pull-up resistor must be placed on the INT pin for proper operation.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions (see “Interrupt Status - Address 0Dh” on page 35). Each source may be masked off through mask register bits. In addition, Each source may be set to rising edge, falling edge, or level-sensitive. Combined with the option of level-sensitive or edge-sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

The CS5346 also has a dedicated overflow output. The OVFL pin functions as active low open drain and has no active pull-up transistor, thereby requiring an external pull-up resistor. The OVFL pin outputs an OR of the ADCOverflow and ADCUnderflow conditions available in the Interrupt Status register; however, these conditions do not need to be unmasked for proper operation of the OVFL pin.

5.9 Reset

When $\overline{\text{RST}}$ is low, the CS5346 enters a low-power mode and all internal states are reset, including the control port and registers, the outputs are muted. When $\overline{\text{RST}}$ is high, the control port becomes operational, and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control register will then cause the part to leave the low-power state and begin operation.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RST}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT+ pin. During this voltage reference ramp delay, SDOUT will be automatically muted.

It is recommended that $\overline{\text{RST}}$ be activated if the analog or digital supplies drop below the recommended operating condition to prevent power-glitch-related issues.

5.10 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the master clocks and left/right clocks must be the same for all of the CS5346s in the system. If only one master clock source is needed, one solution is to place one CS5346 in Master Mode, and slave all of the other CS5346s to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS5346 reset with the inactive edge of master clock. This will ensure that all converters begin sampling on the same clock edge.

5.11 Grounding and Power Supply Decoupling

As with any high-resolution converter, the CS5346 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 7 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supplies (VLS or VLC). Power supply decoupling capacitors should be as near to the CS5346 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CS5346 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS5346 digital outputs only to CMOS inputs.

6. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
pg. 28		1	1	0	0	x	x	x	x
02h	Power Control	Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	Reserved	PDN
pg. 28		0	0	0	0	0	0	0	1
03h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	1	0	0	0
04h	ADC Control	FM1	FM0	Reserved	DIF	Reserved	Mute	HPFFreeze	M/$\overline{S}$
pg. 29		0	0	0	0	0	0	0	0
05h	MCLK Frequency	Reserved	MCLK Freq2	MCLK Freq1	MCLK Freq0	Reserved	Reserved	Reserved	Reserved
pg. 30		0	0	0	0	0	0	0	0
06h	PGAOut Control	Reserved	PGAOut	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
pg. 30		0	1	0	0	0	0	0	0
07h	PGA Ch B Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
pg. 30		0	0	0	0	0	0	0	0
08h	PGA Ch A Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
pg. 31		0	0	0	0	0	0	0	0
09h	Analog Input Control	Reserved	Reserved	Reserved	PGASoft	PGAZero	Sel2	Sel1	Sel0
pg. 31		0	0	0	1	1	0	0	1
0Ah - 0Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
0Ch	Active Level Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Active_H/$\overline{L}$
pg. 32		1	1	0	0	0	0	0	0
0Dh	Interrupt Status	Reserved	Reserved	Reserved	Reserved	ClkErr	Reserved	Ovfl	Undrfl
pg. 32		0	0	0	0	0	0	0	0
0Eh	Interrupt Mask	Reserved	Reserved	Reserved	Reserved	ClkErrM	Reserved	OvflM	UndrflM
pg. 33		0	0	0	0	0	0	0	0
0Fh	Interrupt Mode MSB	Reserved	Reserved	Reserved	Reserved	ClkErr1	Reserved	Ovfl1	Undrfl1
pg. 33		0	0	0	0	0	0	0	0
10h	Interrupt Mode LSB	Reserved	Reserved	Reserved	Reserved	ClkErr0	Reserved	Ovfl0	Undrfl0
pg. 33		0	0	0	0	0	0	0	0

7. REGISTER DESCRIPTION

7.1 Chip ID - Register 01h

7	6	5	4	3	2	1	0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID, which is 1100b, and the remaining bits (3 through 0) indicate the device revision as shown in Table 4 below.

REV[3:0]	Revision
0000	A1

Table 4. Device Revision

7.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	Reserved	PDN

7.2.1 Freeze (Bit 7)

Function:

This function allows modifications to be made to certain control port bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed in Table 5.

Name	Register	Bit(s)
Mute	04h	2
Gain[5:0]	07h	5:0
Gain[5:0]	08h	5:0

Table 5. Freeze-able Bits

7.2.2 Power-Down MIC (Bit 3)

Function:

The microphone preamplifier block will enter a low-power state whenever this bit is set.

7.2.3 Power-Down ADC (Bit 2)

Function:

The ADC pair will remain in a reset state whenever this bit is set.

7.2.4 Power-Down Device (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The power-down bit is set by default and must be cleared before normal operation can occur. The contents of the control registers are retained when the device is in power-down.

7.3 ADC Control - Address 04h

7	6	5	4	3	2	1	0
FM1	FM0	Reserved	DIF	Reserved	Mute	HPFFreeze	M/$\overline{S}$

7.3.1 Functional Mode (Bits 7:6)

Function:

Selects the required range of sample rates.

FM1	FM0	Mode
0	0	Single-Speed Mode: 8 to 50 kHz sample rates
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Reserved

Table 6. Functional Mode Selection

7.3.2 Digital Interface Format (Bit 4)

Function:

The required relationship between LRCK, SCLK and SDOUT is defined by the Digital Interface Format bit. The options are detailed in Table 7 and may be seen in Figure 3 and Figure 4.

DIF	Description	Format	Figure
0	Left-Justified (default)	0	3
1	I²S	1	4

Table 7. Digital Interface Formats

7.3.3 Mute (Bit 2)

Function:

When this bit is set, the serial audio output of the both channels is muted.

7.3.4 High-Pass Filter Freeze (Bit 1)

Function:

When this bit is set, the internal high-pass filter is disabled. The current DC offset value will be frozen and continue to be subtracted from the conversion result. See “High-Pass Filter and DC Offset Calibration” on page 20.

7.3.5 Master / Slave Mode (Bit 0)

Function:

This bit selects either master or slave operation for the serial audio port. Setting this bit selects Master Mode, while clearing this bit selects Slave Mode.

7.4 MCLK Frequency - Address 05h

7	6	5	4	3	2	1	0
Reserved	MCLK Freq2	MCLK Freq1	MCLK Freq0	Reserved	Reserved	Reserved	Reserved

7.4.1 Master Clock Dividers (Bits 6:4)

Function:

Sets the frequency of the supplied MCLK signal. See Table 8 for the appropriate settings.

MCLK Divider	MCLK Freq2	MCLK Freq1	MCLK Freq0
÷ 1	0	0	0
÷ 1.5	0	0	1
÷ 2	0	1	0
÷ 3	0	1	1
÷ 4	1	0	0
Reserved	1	0	1
Reserved	1	1	x

Table 8. MCLK Frequency

7.5 PGAOut Control - Address 06h

7	6	5	4	3	2	1	0
Reserved	PGAOut	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7.5.1 PGAOut Source Select (Bit 6)

Function:

This bit is used to configure the PGAOut pins to be either high impedance or PGA outputs. Refer to Table 9.

PGAOut	PGAOutA & PGAOutB
0	High Impedance
1	PGA Output

Table 9. PGAOut Source Selection

7.6 Channel B PGA Control - Address 07h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

7.6.1 Channel B PGA Gain (Bits 5:0)

Function:

See “Channel A PGA Gain (Bits 5:0)” on page 31.

7.7 Channel A PGA Control - Address 08h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

7.7.1 Channel A PGA Gain (Bits 5:0)

Function:

Sets the gain or attenuation for the ADC input PGA stage. The gain may be adjusted from -12 dB to +12 dB in 0.5 dB steps. The gain bits are in two's complement with the Gain0 bit set for a 0.5 dB step. Register settings outside of the ±12 dB range are reserved and must not be used. See Table 10 for example settings.

Gain[5:0]	Setting
101000	-12 dB
000000	0 dB
011000	+12 dB

Table 10. Example Gain and Attenuation Settings

7.8 ADC Input Control - Address 09h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PGASoft	PGAZero	Sel2	Sel1	Sel0

7.8.1 PGA Soft Ramp or Zero Cross Enable (Bits 4:3)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 11.

Zero Cross Enable

Zero Cross Enable dictates that signal-level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 11.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal-level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 11.

PGASoft	PGAZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

Table 11. PGA Soft Cross or Zero Cross Mode Selection

7.8.2 Analog Input Selection (Bits 2:0)

Function:

These bits are used to select the input source for the PGA and ADC. Please see Table 12.

Sel2	Sel1	Sel0	PGA/ADC Input
0	0	0	Microphone-Level Inputs (+32 dB Gain Enabled)
0	0	1	Line-Level Input Pair 1
0	1	0	Line-Level Input Pair 2
0	1	1	Line-Level Input Pair 3
1	0	0	Line-Level Input Pair 4
1	0	1	Line-Level Input Pair 5
1	1	0	Line-Level Input Pair 6
1	1	1	Reserved

Table 12. Analog Input Multiplexer Selection

7.9 Active Level Control - Address 0Ch

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Active_H/$\overline{L}$

7.9.1 Active High/ $\overline{Low}$ (Bit 0)

Function:

When this bit is set, the INT pin functions as an active high CMOS driver.

When this bit is cleared, the INT pin functions as an active low open drain driver and will require an external pull-up resistor for proper operation.

7.10 Status - Address 0Dh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ClkErr	Reserved	Ovfl	Undrfl

For all bits in this register, a ‘1’ means the associated condition has occurred at least once since the register was last read. A ‘0’ means the associated condition has NOT occurred since the last reading of the register. Status bits that are masked off in the associated mask register will always be ‘0’ in this register. This register defaults to 00h.

7.10.1 Clock Error (Bit 3)

Function:

Indicates the occurrence of a clock error condition.

7.10.2 Overflow (Bit 1)

Function:

Indicates the occurrence of an ADC overflow condition.

7.10.3 Underflow (Bit 0)

Function:

Indicates the occurrence of an ADC underflow condition.

7.11 Status Mask - Address 0Eh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ClkErrM	Reserved	OvflM	UndrflM

Function:

The bits of this register serve as a mask for the Status sources found in the register “Status - Address 0Dh” on page 32. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the status register. The bit positions align with the corresponding bits in the Status register.

7.12 Status Mode MSB - Address 0Fh

7.13 Status Mode LSB - Address 10h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ClkErr1	Reserved	Ovfl1	Undrfl1
Reserved	Reserved	Reserved	Reserved	ClkErr0	Reserved	Ovfl0	Undrfl0

Function:

The two Status Mode registers form a 2-bit code for each Status register function. There are three ways to update the Status register in accordance with the status condition. In the Rising-Edge Active Mode, the status bit becomes active on the arrival of the condition. In the Falling-Edge Active Mode, the status bit becomes active on the removal of the condition. In Level-Active Mode, the status bit is active during the condition.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

9. FILTER PLOTS

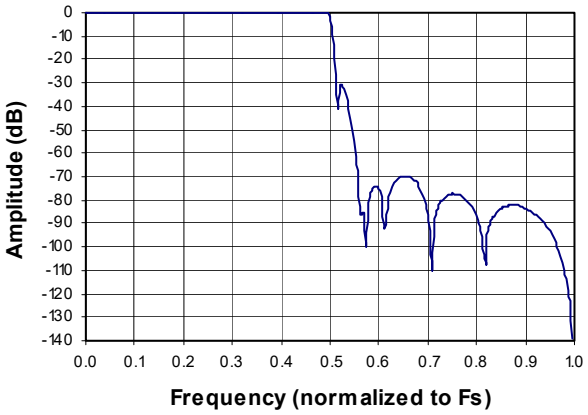


Figure 17. Single-Speed Stopband Rejection

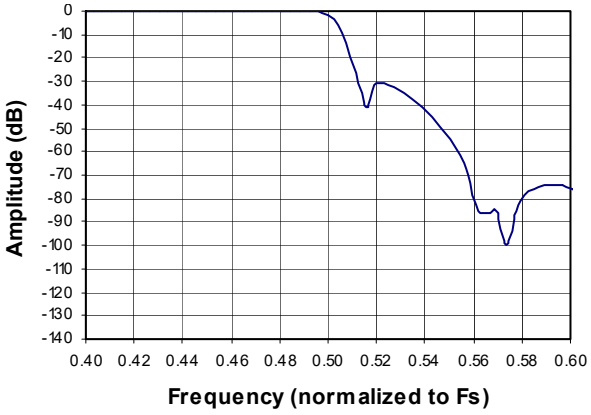


Figure 18. Single-Speed Stopband Rejection

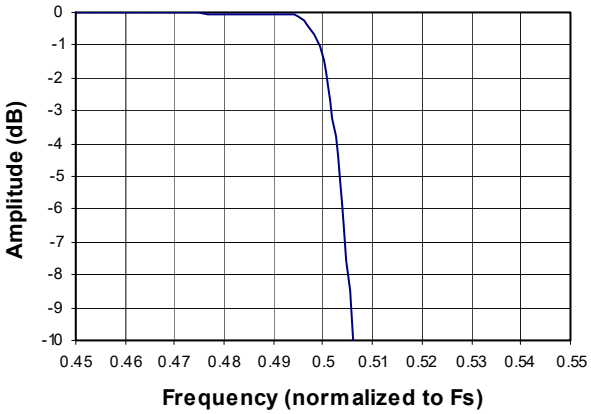


Figure 19. Single-Speed Transition Band (Detail)

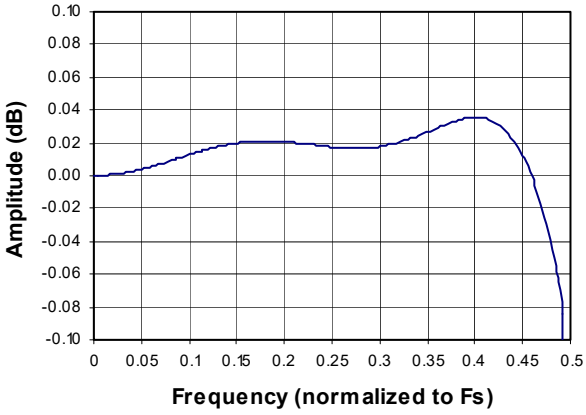


Figure 20. Single-Speed Passband Ripple

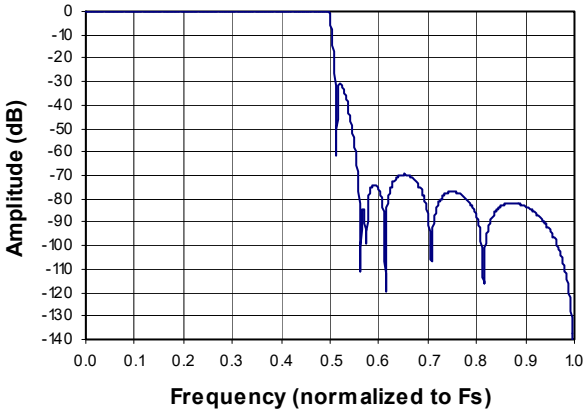


Figure 21. Double-Speed Stopband Rejection

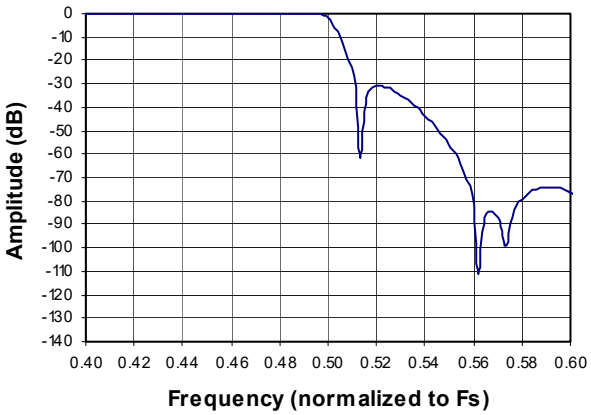


Figure 22. Double-Speed Stopband Rejection

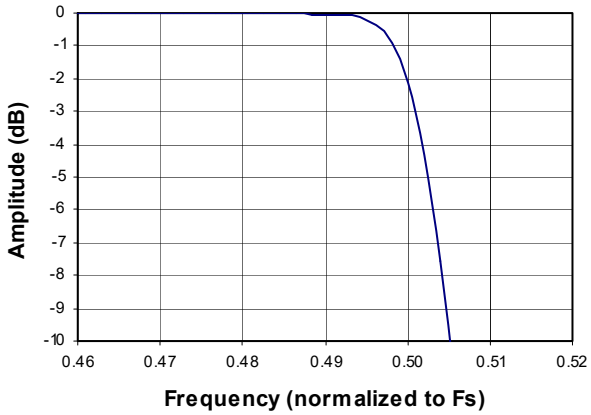


Figure 23. Double-Speed Transition Band (Detail)

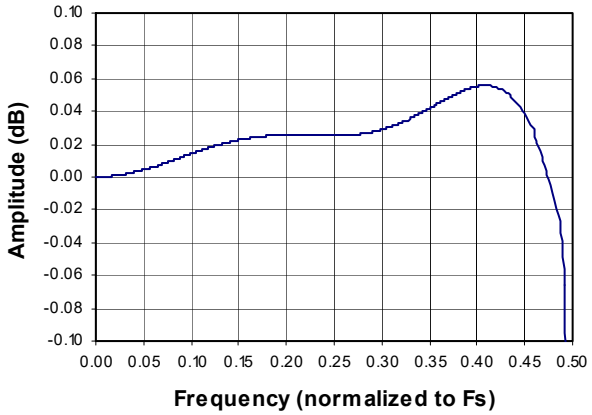


Figure 24. Double-Speed Passband Ripple

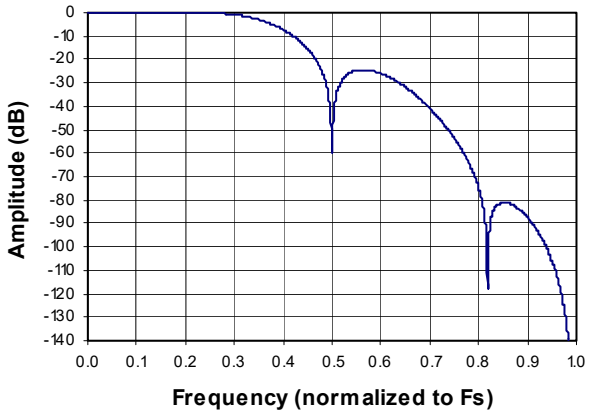


Figure 25. Quad-Speed Stopband Rejection

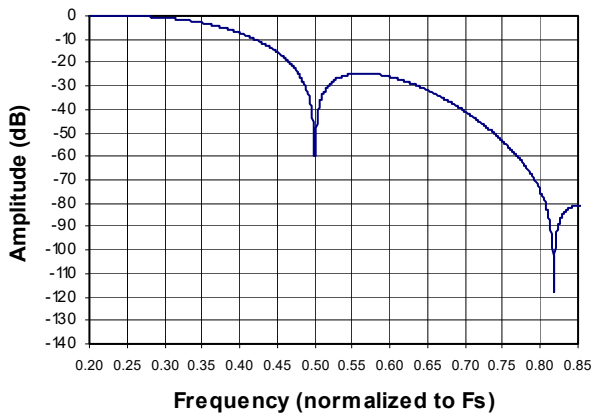


Figure 26. Quad-Speed Stopband Rejection

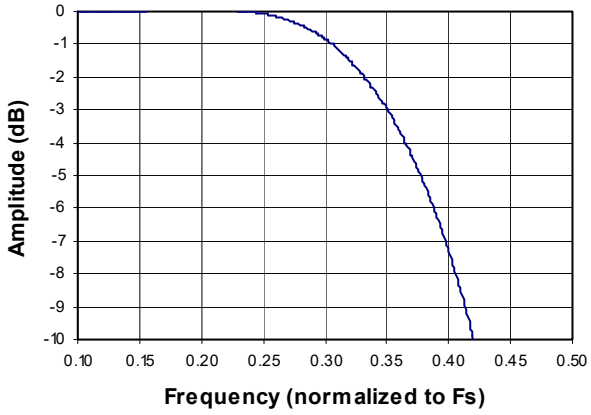


Figure 27. Quad-Speed Transition Band (Detail)

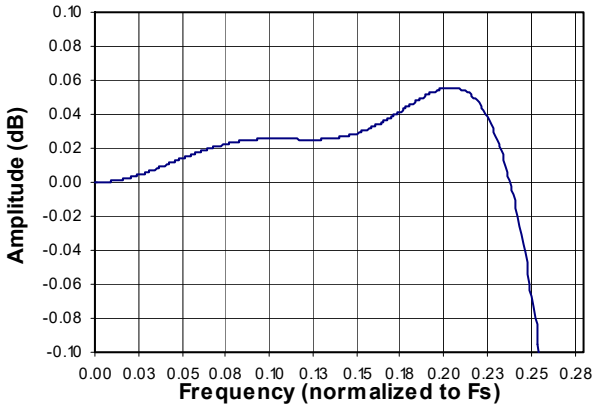
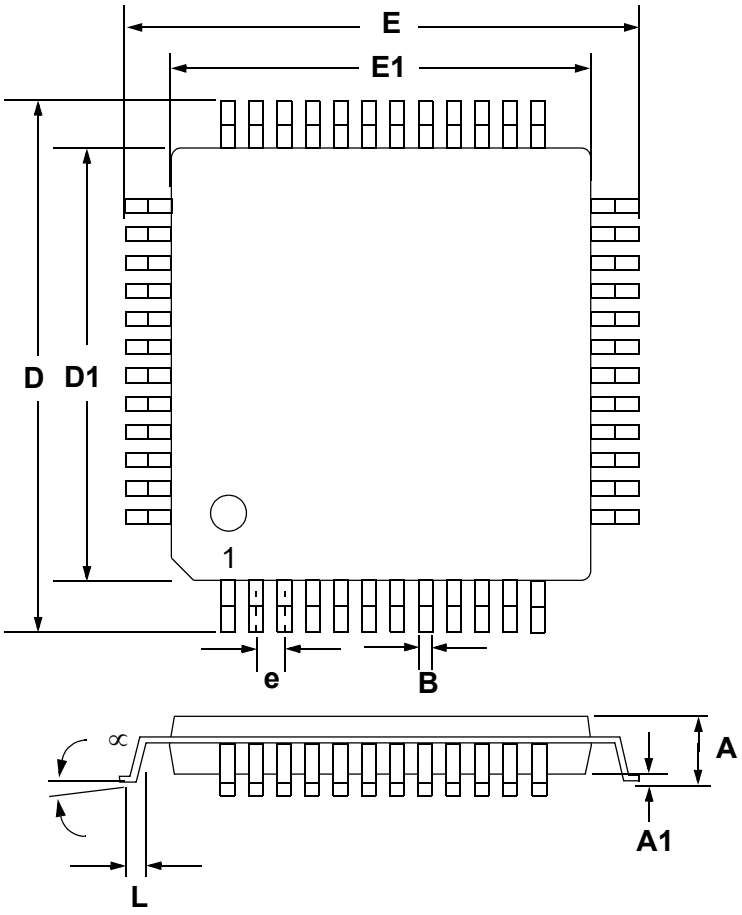


Figure 28. Quad-Speed Passband Ripple

10.PACKAGE DIMENSIONS

48L LQFP PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	---	0.055	0.063	---	1.40	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
B	0.007	0.009	0.011	0.17	0.22	0.27
D	0.343	0.354	0.366	8.70	9.0 BSC	9.30
D1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
E	0.343	0.354	0.366	8.70	9.0 BSC	9.30
E1	0.272	0.28	0.280	6.90	7.0 BSC	7.10
e*	0.016	0.020	0.024	0.40	0.50 BSC	0.60
L	0.018	0.24	0.030	0.45	0.60	0.75
∝	0.000°	4°	7.000°	0.00°	4°	7.00°

* Nominal pin pitch is 0.50 mm *Controlling dimension is mm. *JEDEC Designation: MS022

11.THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 1)	48-LQFP	θ_{JA} θ_{JC}	- -	48 15	- -	°C/Watt °C/Watt
Allowable Junction Temperature			-	-	125	°C

1. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

12.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS5346	24-bit, 192 kHz Stereo Audio ADC	48-LQFP	Yes	Commercial	-40° to +85° C	Tray	CS5346K-CQZ
						Tape & Reel	CS5346K-CQZR
CDB5346	CS5346 Evaluation Board		No	-	-	-	CDB5346

13.REVISION HISTORY

Release	Changes
PP1	-Updated Title -Added text to Section 2. on page 7 -Added V/V representations for PGA and MIC gain specifications -Updated Automotive THD+N and DNR limits -Added reference to CDB5346 in Section 5.6 on page 23
PP2	-Added note 3 and note for AFILTA/AFILTB capacitors in Figure 7.
PP3	-Removed references to automotive grade parts.
F1	-Updated Ordering Information as per PCN-2020-141.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.