MC74HCT541A

Octal 3-State Non-Inverting Buffer/Line Driver/ Line Receiver With LSTTL-Compatible Inputs

High−Performance Silicon−Gate CMOS

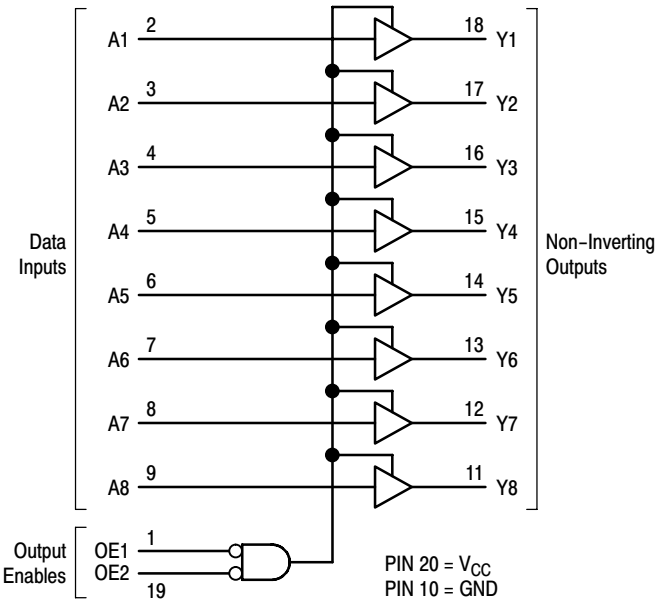
The MC74HCT541A is identical in pinout to the LS541. This device may be used as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HCT541A is an octal non−inverting buffer/line driver/line receiver designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active−low output enables.

Features

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS−Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- Pb−Free Packages are Available*

LOGIC DIAGRAM



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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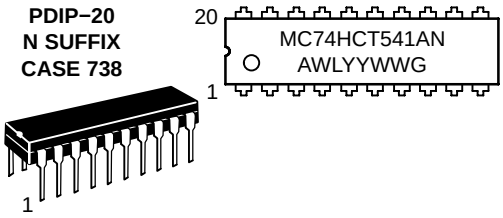
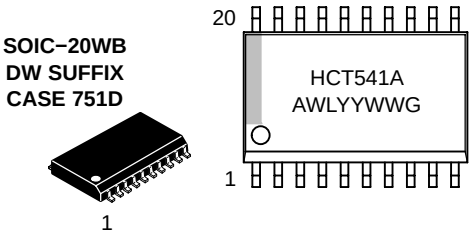
MARKING DIAGRAMS

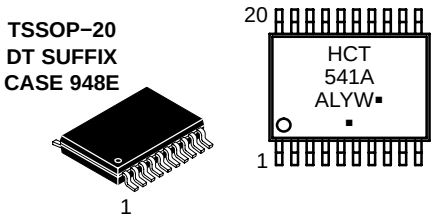
PDIP−20
N SUFFIX
CASE 738



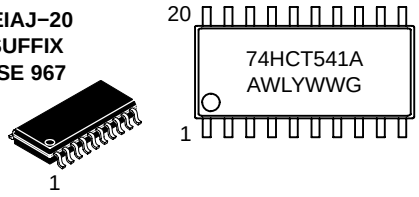
SOIC−20WB
DW SUFFIX
CASE 751D



TSSOP−20
DT SUFFIX
CASE 948E



SOEIAJ−20
F SUFFIX
CASE 967



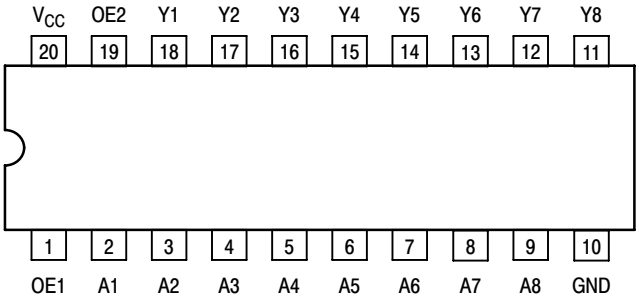
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

PINOUT: 20−LEAD PACKAGES



(Top View)

FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance
X = Don't Care

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature Range	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP or SOIC Package	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature Range, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise/Fall Time (Figure 1)	0	500	ns

DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1V or V_{CC} − 0.1V $\|I_{out}\| \le 20\mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$mA	4.5	3.98	3.84	3.70	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$mA	4.5	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	Output in High Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0μA	5.5	4	40	160	μA

				≥ −55°C	25 to 125°C	
ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0μA	5.5	2.9	2.4	mA

1. Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).
2. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC CHARACTERISTICS (V_{CC} = 5.0V, C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		−55 to 25°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	23	28	32	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 4)	30	34	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum 3−State Output Capacitance (Output in High Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	55	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

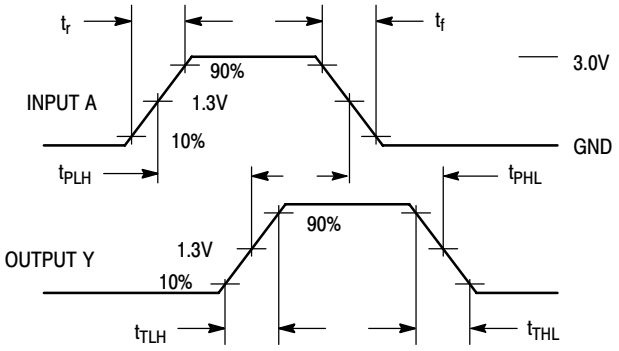


Figure 1.

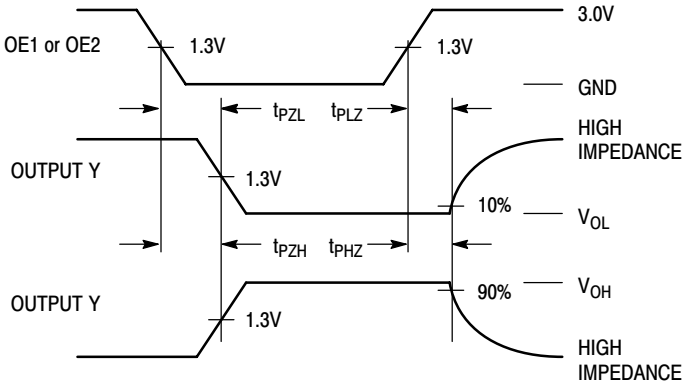
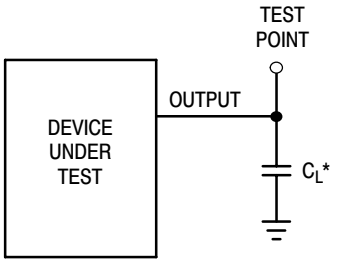


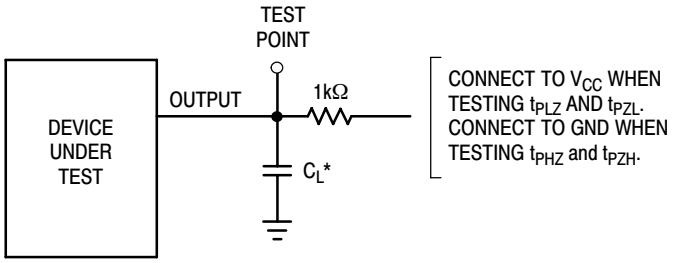
Figure 2.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 3.



*Includes all probe and jig capacitance

Figure 4.

PIN DESCRIPTIONS

INPUTS

A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9) — Data input pins. Data on these pins appear in non−inverted form on the corresponding Y outputs, when the outputs are enabled.

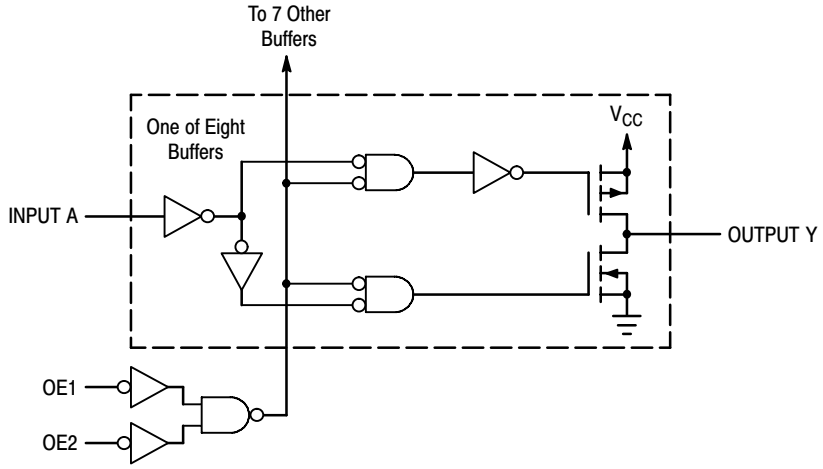
CONTROLS

OE1, OE2 (PINS 1, 19) — Output enables (active−low). When a low voltage is applied to both of these pins, the outputs are enabled and the device functions as a non−inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

OUTPUTS

Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11) — Device outputs. Depending upon the state of the output enable pins, these outputs are either non−inverting outputs or high−impedance outputs.

LOGIC DETAIL



ORDERING INFORMATION

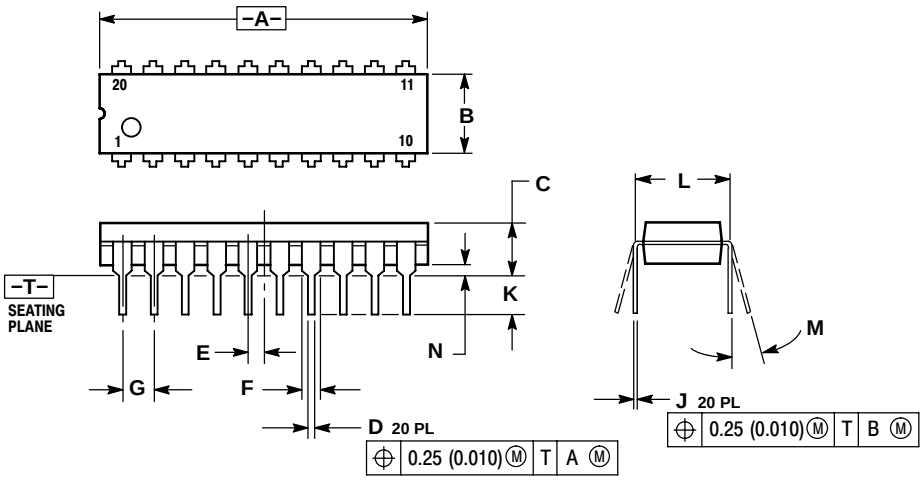
Device	Package	Shipping†
MC74HCT541AN	PDIP−20	18 Units / Rail
MC74HCT541ANG	PDIP−20 (Pb−Free)	
MC74HCT541ADW	SOIC−20	38 Units / Rail
MC74HCT541ADWG	SOIC−20 (Pb−Free)	
MC74HCT541ADWR2	SOIC−20	1000 / Tape & Reel
MC74HCT541ADWR2G	SOIC−20 (Pb−Free)	
MC74HCT541ADTR2	TSSOP−20*	2500 / Tape & Reel
MC74HCT541ADTR2G	TSSOP−20*	
MC74HCT541AFG	SOEIAJ−20 (Pb−Free)	40 Units / Rail
MC74HCT541AFEL	SOEIAJ−20	2000 / Tape & Reel
MC74HCT541AFELG	SOEIAJ−20 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*These packages are inherently Pb−Free.

PACKAGE DIMENSIONS

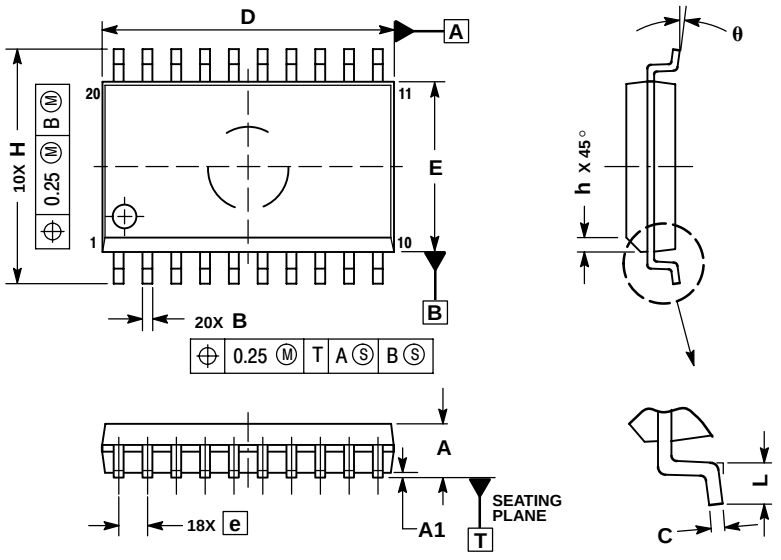
PDIP−20
N SUFFIX
CASE 738−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO−20 WB
DW SUFFIX
CASE 751D−05
ISSUE G

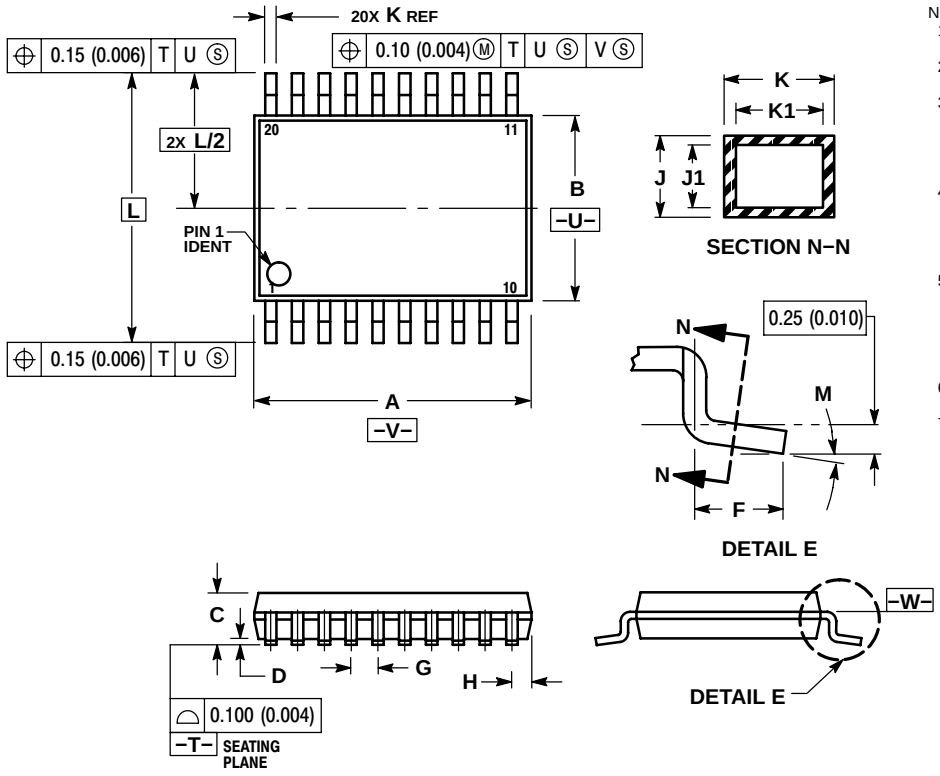


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP−20
DT SUFFIX
CASE 948E−02
ISSUE B

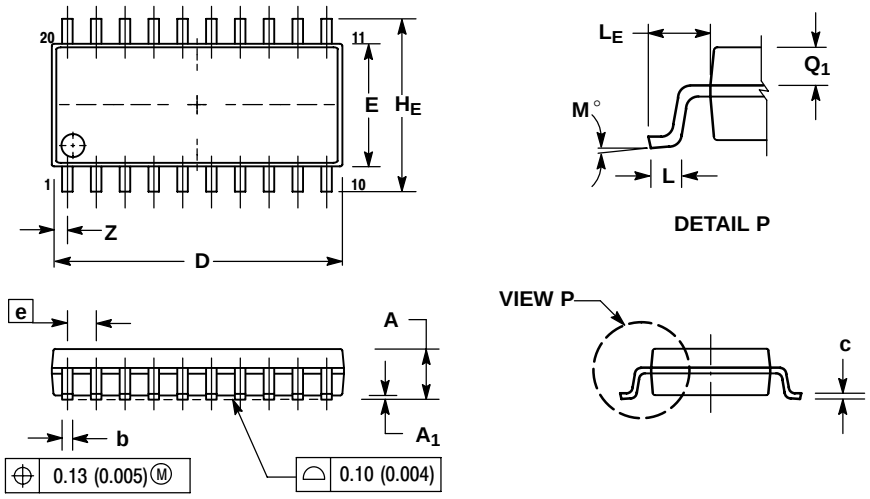


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOEIAJ−20
F SUFFIX
CASE 967−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

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MC74HCT541A/D