NST489AMT1G, NSVT489AMT1G

High Current Surface Mount NPN Silicon Low $V_{CE(sat)}$ Switching Transistor for Load Management in Portable Applications

ON Semiconductor®

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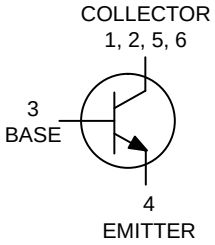
30 VOLTS, 3.0 AMPS NPN TRANSISTOR

TSOP−6
CASE 318G
STYLE 6



Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	50	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current − Continuous	I_C	2.0	A
Collector Current − Peak	I_{CM}	3.0	A

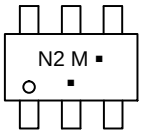
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	 535 4.3	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	 234	 °C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	 1.180 9.4	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	 106	 °C/W
Thermal Resistance, Junction−to−Lead #1	$R_{\theta JL}$ (Note 1) $R_{\theta JL}$ (Note 2)	110 50	°C/W °C/W
Total Device Dissipation (Single Pulse < 10 s)	$P_{Dsingle}$ (Notes 2 and 3)	 1.75	 W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−4 with 1 oz and 3.9 mm^2 of copper area.
2. FR−4 with 1 oz and 645 mm^2 of copper area.
3. Refer to Figure 8.

DEVICE MARKING



N2 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NST489AMT1G	TSOP−6 (Pb−Free)	3,000 / Tape & Reel
NSVT489AMT1G	TSOP−6 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Breakdown Voltage (I_C = 10 mA, I_B = 0)		$V_{(BR)CEO}$	30	−	−	V
Collector−Base Breakdown Voltage (I_C = 0.1 mA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	V
Emitter−Base Breakdown Voltage (I_E = 0.1 mA, I_C = 0)		$V_{(BR)EBO}$	5.0	−	−	V
Collector Cutoff Current (V_{CB} = 30 V, I_E = 0)		I_{CBO}	−	−	0.1	μA
Collector−Emitter Cutoff Current (V_{CES} = 30 V)		I_{CES}	−	−	0.1	μA
Emitter Cutoff Current (V_{EB} = 4.0 V)		I_{EBO}	−	−	0.1	μA
ON CHARACTERISTICS						
DC Current Gain (Note 4)	(I_C = 1.0 mA, V_{CE} = 5.0 V) (I_C = 0.5 A, V_{CE} = 5.0 V) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	300 300 200	− 500 −	− 900 −	
Collector−Emitter Saturation Voltage (Note 4)	(I_C = 1.0 A, I_B = 100 mA) (I_C = 0.5 A, I_B = 50 mA) (I_C = 0.1 A, I_B = 1.0 mA)	$V_{CE(sat)}$	− − −	0.10 0.06 0.05	0.200 0.125 0.075	V
Base−Emitter Saturation Voltage (Note 4) (I_C = 1.0 A, I_B = 0.1 A)		$V_{BE(sat)}$	−	−	1.1	V
Base−Emitter Turn−on Voltage (Note 4) (I_C = 1.0 A, V_{CE} = 2.0 V)		$V_{BE(on)}$	−	−	1.1	V
Cutoff Frequency (I_C = 100 mA, V_{CE} = 5.0 V, f = 100 MHz		f_T	200	300	−	MHz
Output Capacitance (f = 1.0 MHz)		C_{obo}	−	−	15	pF

4. Pulsed Condition: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

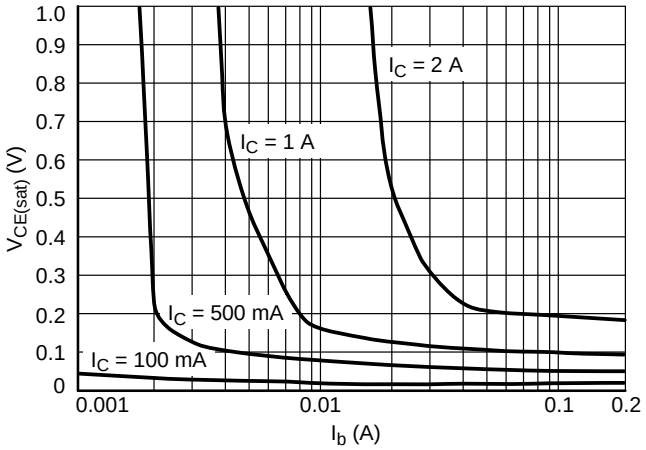


Figure 1. $V_{CE\ (sat)}$ versus I_b

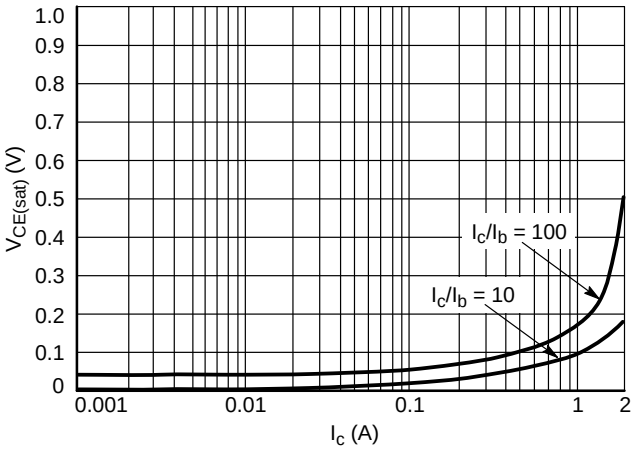


Figure 2. $V_{CE\ (sat)}$ versus I_c

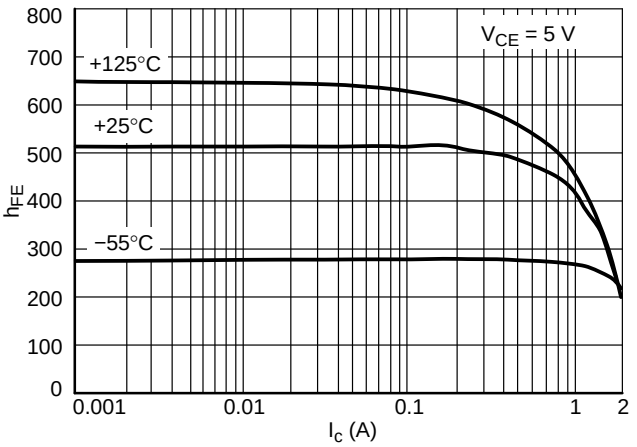


Figure 3. h_{FE} versus I_c

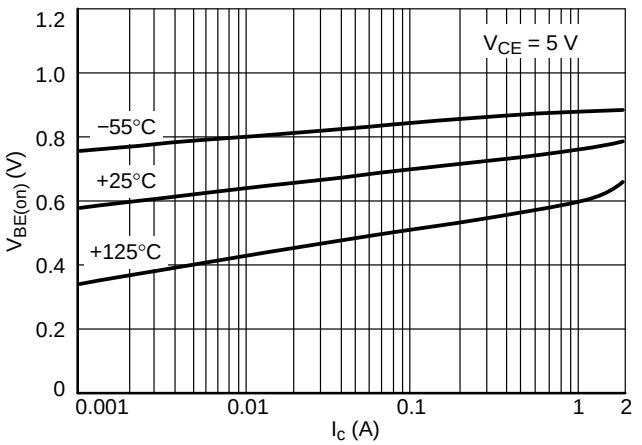


Figure 4. $V_{BE(on)}$ versus I_c

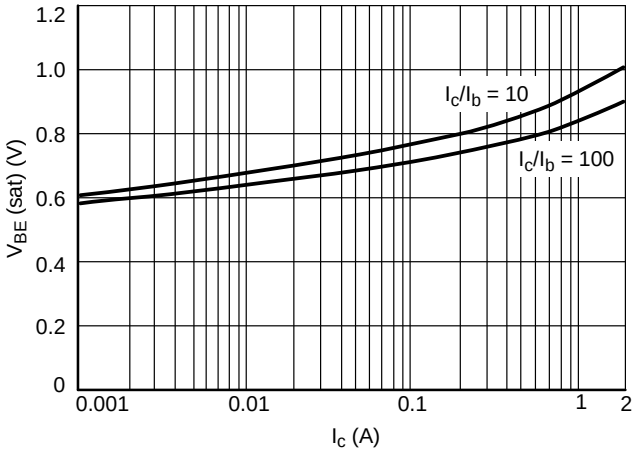


Figure 5. $V_{BE(sat)}$ versus I_c

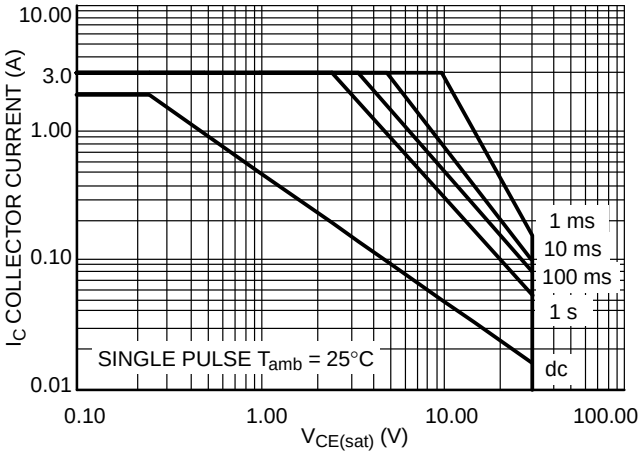


Figure 6. Safe Operating Area

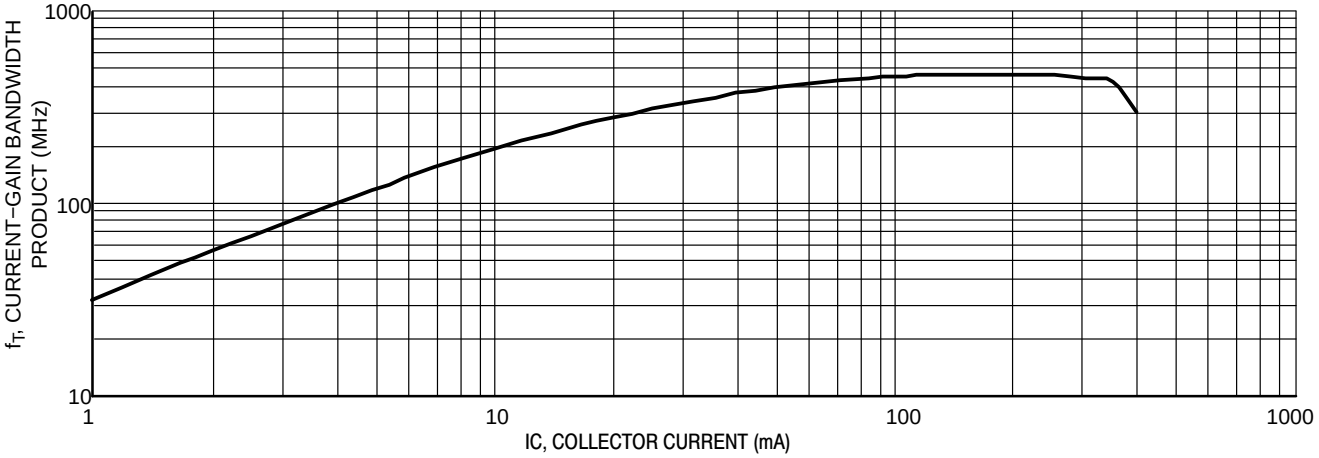


Figure 7. f_T (MHZ) versus I_C (mA) V_{CE} = 5.0 V

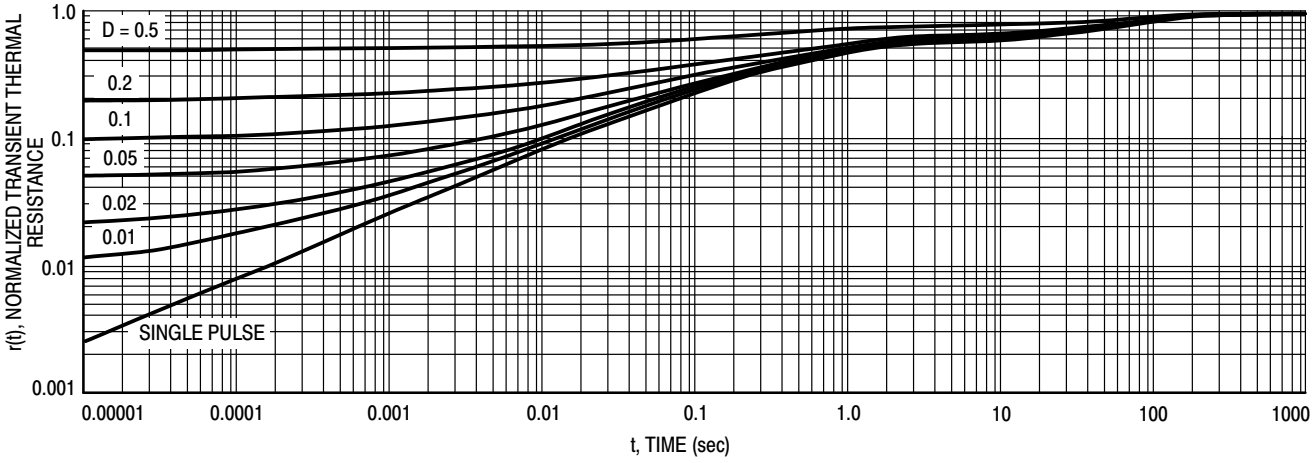


Figure 8. Normalized Thermal Response

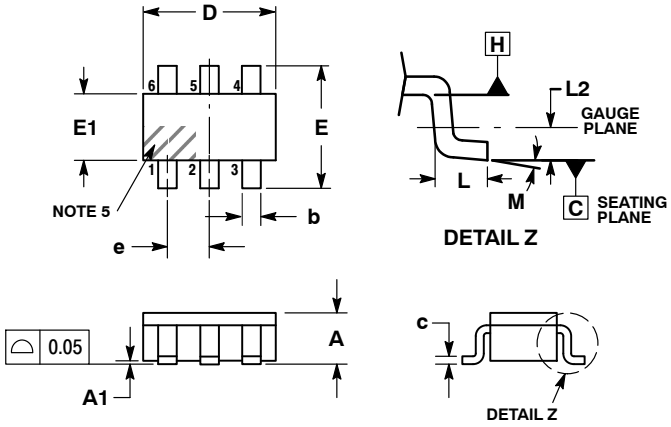
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

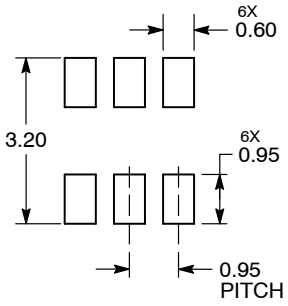
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

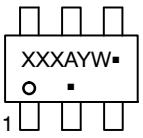
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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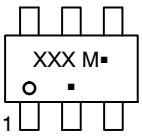

STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

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For additional information, please contact your local Sales Representative

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