

NST489AMT1G, NSVT489AMT1G

High Current Surface Mount NPN Silicon Low $V_{CE(sat)}$ Switching Transistor for Load Management in Portable Applications

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	30	V
Collector-Base Voltage	V_{CBO}	50	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current – Continuous	I_C	2.0	A
Collector Current – Peak	I_{CM}	3.0	A

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 1)	535 4.3	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	234	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 2)	1.180 9.4	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	106	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$ (Note 1) $R_{\theta JL}$ (Note 2)	110 50	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 s)	$P_{D\text{single}}$ (Notes 2 and 3)	1.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-4 with 1 oz and 3.9 mm^2 of copper area.
2. FR-4 with 1 oz and 645 mm^2 of copper area.
3. Refer to Figure 8.



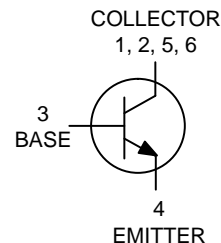
ON Semiconductor®

www.onsemi.com

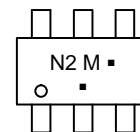
30 VOLTS, 3.0 AMPS
NPN TRANSISTOR



TSOP-6
CASE 318G
STYLE 6



DEVICE MARKING



N2 = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NST489AMT1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel
NSVT489AMT1G	TSOP-6 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NST489AMT1G, NSVT489AMT1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	30	–	–	V	
Collector–Base Breakdown Voltage ($I_C = 0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	50	–	–	V	
Emitter–Base Breakdown Voltage ($I_E = 0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	–	V	
Collector Cutoff Current ($V_{CB} = 30\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	0.1	μA	
Collector–Emitter Cutoff Current ($V_{CES} = 30\text{ V}$)	I_{CES}	–	–	0.1	μA	
Emitter Cutoff Current ($V_{EB} = 4.0\text{ V}$)	I_{EBO}	–	–	0.1	μA	
ON CHARACTERISTICS						
DC Current Gain (Note 4)	h_{FE}	$(I_C = 1.0\text{ mA}, V_{CE} = 5.0\text{ V})$ $(I_C = 0.5\text{ A}, V_{CE} = 5.0\text{ V})$ $(I_C = 1.0\text{ A}, V_{CE} = 5.0\text{ V})$	300 300 200	– 500 –	– 900 –	
Collector–Emitter Saturation Voltage (Note 4)	$V_{CE(sat)}$	$(I_C = 1.0\text{ A}, I_B = 100\text{ mA})$ $(I_C = 0.5\text{ A}, I_B = 50\text{ mA})$ $(I_C = 0.1\text{ A}, I_B = 1.0\text{ mA})$	– – –	0.10 0.06 0.05	0.200 0.125 0.075	V
Base–Emitter Saturation Voltage (Note 4) ($I_C = 1.0\text{ A}$, $I_B = 0.1\text{ A}$)	$V_{BE(sat)}$		–	–	1.1	V
Base–Emitter Turn–on Voltage (Note 4) ($I_C = 1.0\text{ A}$, $V_{CE} = 2.0\text{ V}$)	$V_{BE(on)}$		–	–	1.1	V
Cutoff Frequency ($I_C = 100\text{ mA}$, $V_{CE} = 5.0\text{ V}$, $f = 100\text{ MHz}$)	f_T		200	300	–	MHz
Output Capacitance ($f = 1.0\text{ MHz}$)	C_{obo}		–	–	15	pF

4. Pulsed Condition: Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

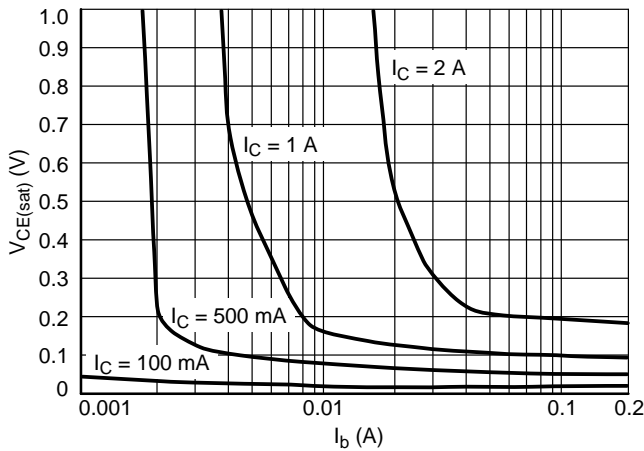


Figure 1. $V_{CE(sat)}$ versus I_b

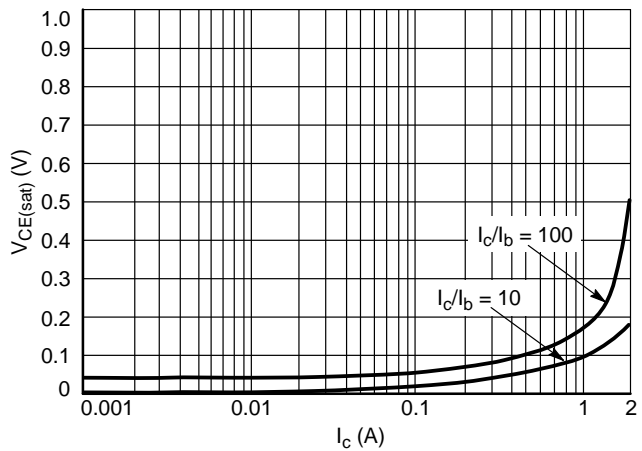


Figure 2. $V_{CE(sat)}$ versus I_C

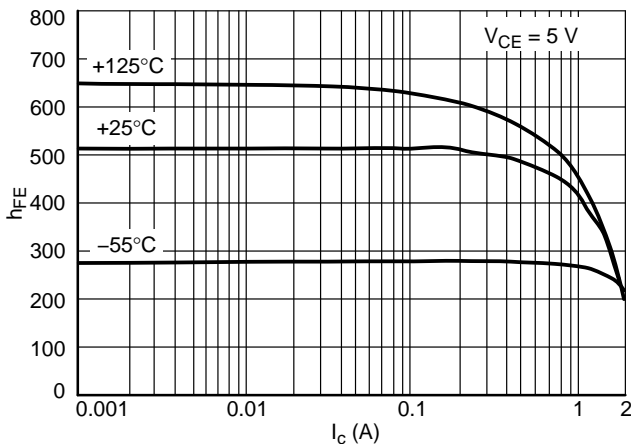


Figure 3. h_{FE} versus I_C

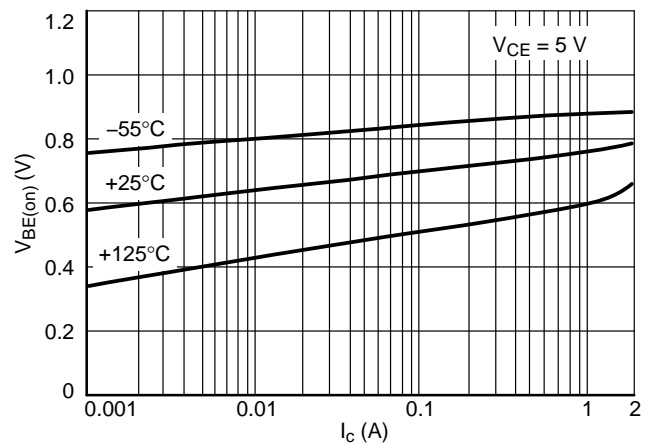


Figure 4. $V_{BE(on)}$ versus I_C

NST489AMT1G, NSVT489AMT1G

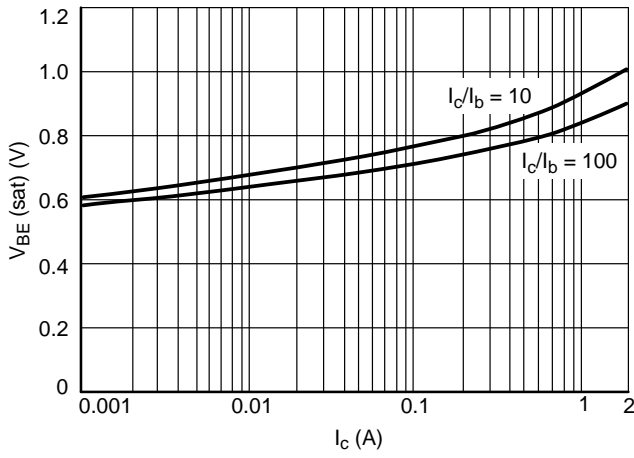


Figure 5. $V_{BE(sat)}$ versus I_C

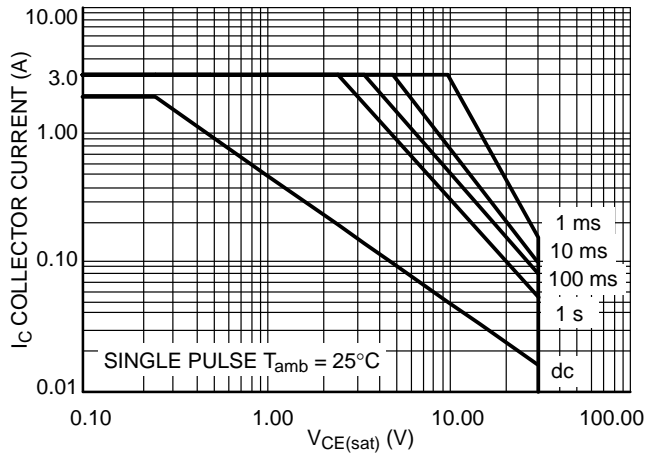


Figure 6. Safe Operating Area

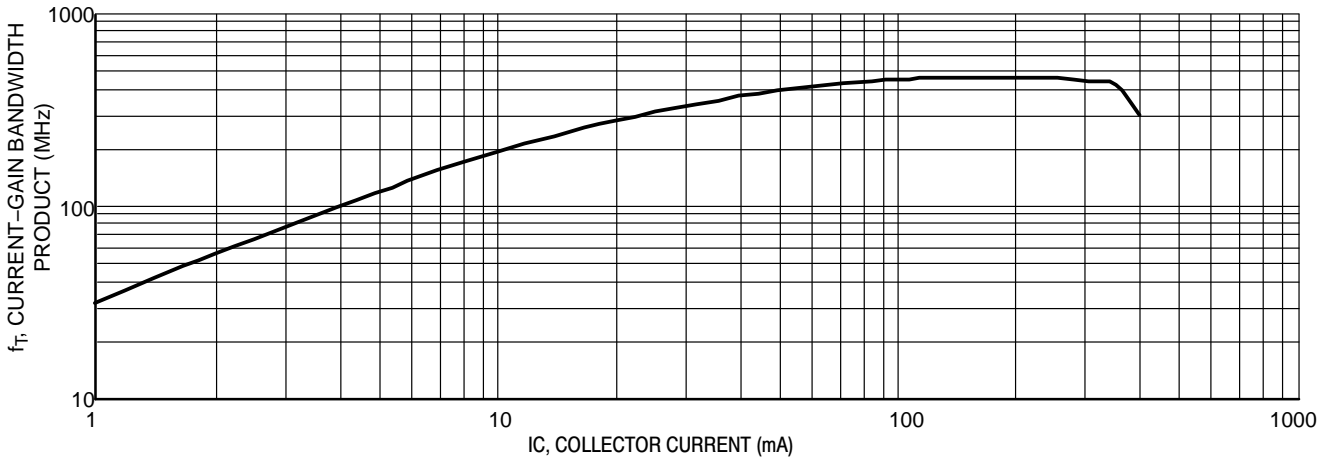


Figure 7. f_T (MHz) versus I_C (mA) $V_{CE} = 5.0$ V

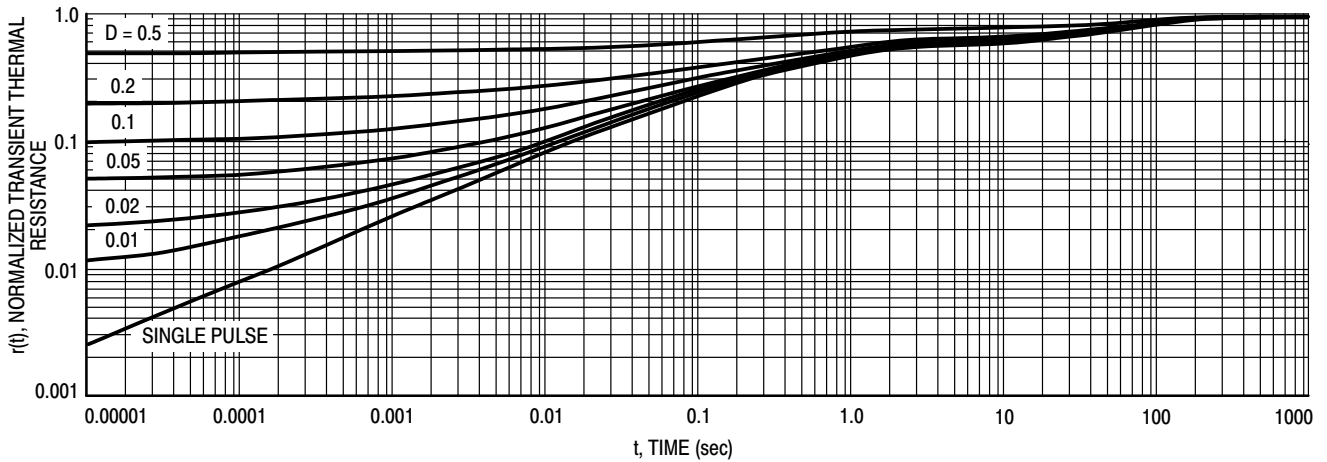


Figure 8. Normalized Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

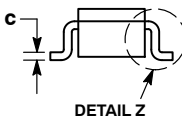
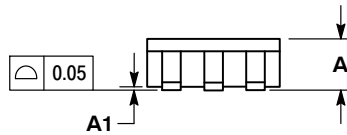
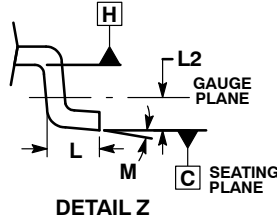
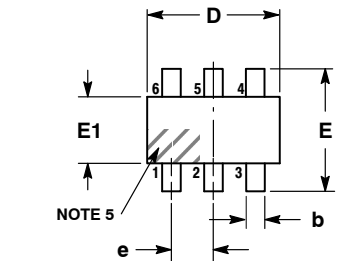
ON Semiconductor®



SCALE 2:1

TSOP-6 CASE 318G-02 ISSUE V

DATE 12 JUN 2012



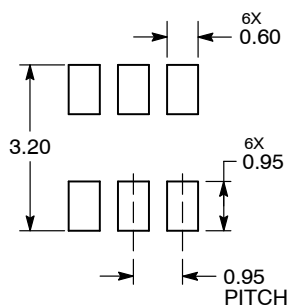
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	-	10°

- | | | | | | |
|--|--|---|---|---|--|
| <p>STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN</p> | <p>STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2</p> | <p>STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out</p> | <p>STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD</p> | <p>STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2</p> | <p>STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR</p> |
| <p>STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER</p> | <p>STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND</p> | <p>STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE</p> | <p>STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+</p> | <p>STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2</p> | <p>STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O</p> |
| <p>STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1</p> | <p>STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN</p> | <p>STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE</p> | <p>STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE</p> | <p>STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR</p> | |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- | | |
|--|---|
| <p>XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package</p> | <p>XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package</p> |
|--|---|

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

DOCUMENT NUMBER:	98ASB14888C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-6	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative