

Dual 4-input multiplexer (3-State)

54F253

FEATURES

- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable Inputs

DESCRIPTION

The 54F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable (E_{0a}, E_{0b}) inputs of the 4-input multiplexers are High, the outputs are forced to a High impedance (Hi-Z) state.

The 54F253 is the logic implementation of a 2-pole, 4-position

switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

All but one device must be in the High impedance state to avoid high currents exceeding the maximum ratings. If the outputs of the 3-State devices are tied together Design of the Output Enable signals must ensure that there is no overlap.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F253/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F253/BFA	GDFF2-F16
20-Pin Ceramic LLCC	54F253/B2A	CQCC2-N20

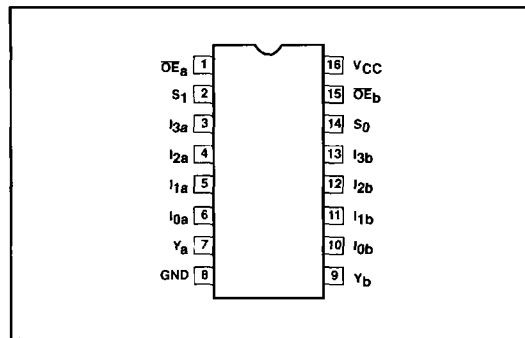
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

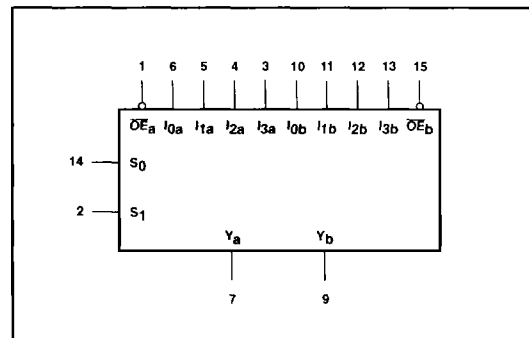
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$I_{0a} - I_{3a}$	Port A data inputs	1.0/1.0	20 μ A/0.6mA
$I_{0b} - I_{3b}$	Port B data inputs	1.0/1.0	20 μ A/0.6mA
$S_0 - S_1$	Common select inputs	1.0/1.0	20 μ A/0.6mA
\overline{OE}_a	Port A output enable input (active Low)	1.0/1.0	20 μ A/0.6mA
\overline{OE}_b	Port B output enable input (active Low)	1.0/1.0	20 μ A/0.6mA
Y_a, Y_b	3-State outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

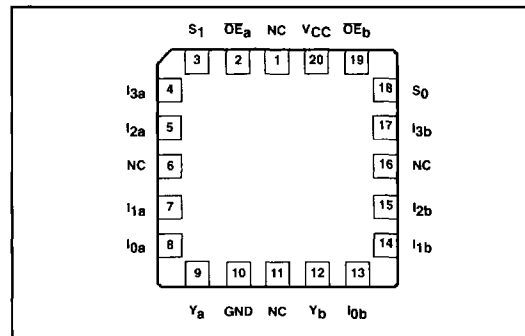
PIN CONFIGURATION



LOGIC SYMBOL



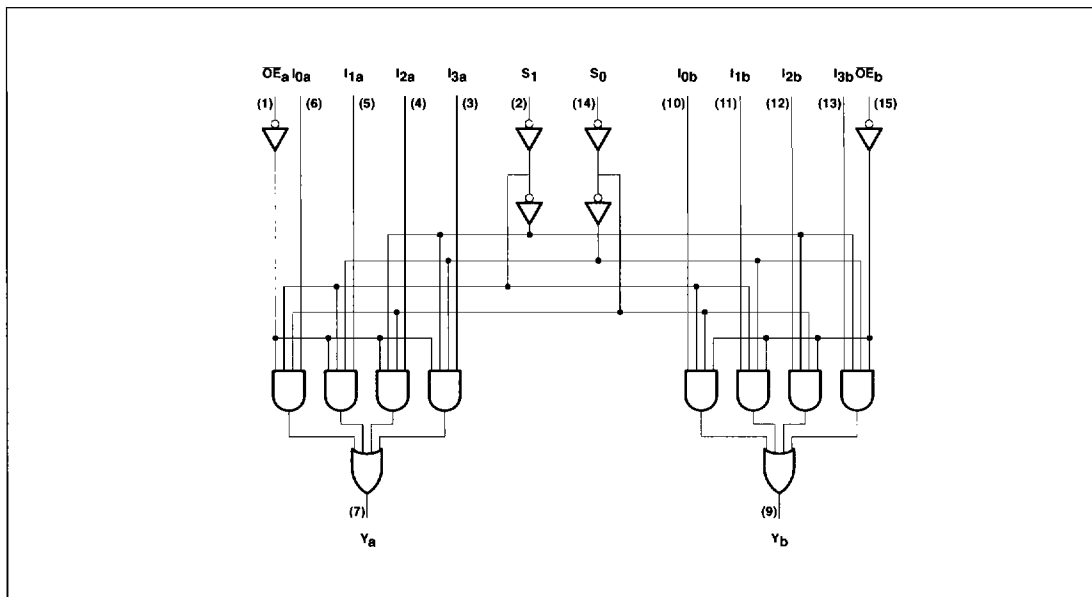
LLCC LEAD CONFIGURATION



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUT	
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	OE	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
 L = Low voltage level
 X = Don't care
 (Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5.0	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3	mA
I_{OH1}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ⁴	LIMITS			UNIT		
			Min	Typ ⁵	Max			
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, I_{OH2} = -3\text{mA}$	2.4			V		
		$V_{IH} = \text{Min}, I_{OH1} = -1\text{mA}$	2.5			V		
V_{OL}	Low-level output voltage	$V_{CC} = \text{Min}, V_{IL} = \text{Max}, V_{IH} = \text{Min}, I_{OL} = \text{Max}$		0.35	0.50	V		
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = I_{IK}$		-0.73	-1.2	V		
I_{IH2}	Input current at maximum input voltage	$V_{CC} = \text{Max}, V_I = 7.0\text{V}$			100	μA		
I_{IH1}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$		1	20	μA		
I_{IL}	Low-level input current	$V_{CC} = \text{Max}, V_I = 0.5\text{V}$		-0.4	-0.6	mA		
I_{OZH}	Off-state output current High-level voltage applied	$V_{CC} = \text{Max}, V_{IH} = \text{Min}, V_O = 2.7\text{V}$		2	50	μA		
I_{OZL}	Off-state output current Low-level voltage applied	$V_{CC} = \text{Max}, V_{IH} = \text{Min}, V_O = 0.5\text{V}$		-2	-50	μA		
I_{OS}	Short-circuit output current ⁶	$V_{CC} = \text{Max}$	-60	-80	-150	mA		
I_{CC}	Supply current ⁷ (total)	I_{CCH}	$V_{CC} = \text{Max}$	$\overline{OE}_n = \text{GND}; S_n = I_n \geq 4.0\text{V}$		10	16	mA
		I_{CCL}		$\overline{OE}_n = S_n = I_n = \text{GND}$		12	23	mA
		I_{CCZ}		$\overline{OE}_n \geq 4.0\text{V}; I_n = S_n = \text{GND}$		14	23	mA

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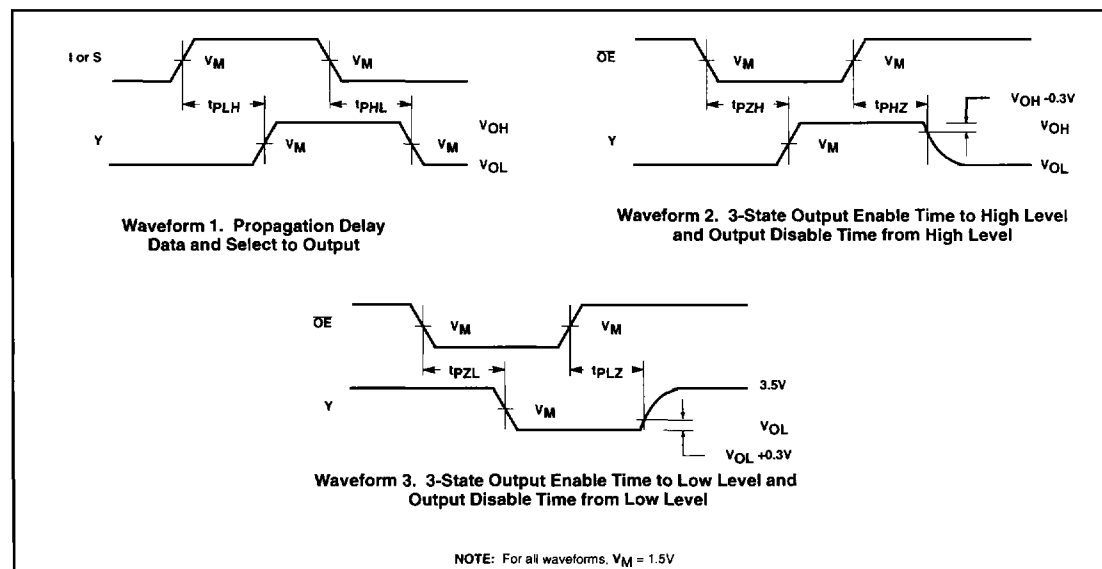
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _A = -55°C to +125°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	2.5 2.5	9.0 9.5	ns ns
t _{PLH} t _{PHL}	Propagation delay Select to output	Waveform 1	5.5 4.5	7.5 8.5	12.5 11.0	3.5 2.5	15.0 14.0	ns ns
t _{PZH}	Output enable time to High level	Waveform 2	3.0	6.5	9.0	2.5	10.5	ns
t _{PZL}	Output enable time to Low level	Waveform 3	3.0	6.5	9.5	2.5	11.0	ns
t _{PHZ}	Output disable time from High level	Waveform 2 Waveform 3	2.0	3.5	5.0	2.0	6.5	ns
t _{PLZ}	Output disable time from Low level	Waveform 3 Waveform 4	2.0	3.0	6.0	2.0	9.0	ns

NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at V_{CC} = 5.0V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- I_{CC} is measured with outputs opened.

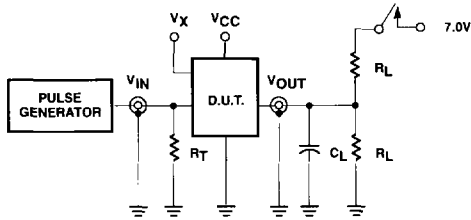
AC WAVEFORMS



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TEST CIRCUIT AND WAVEFORM



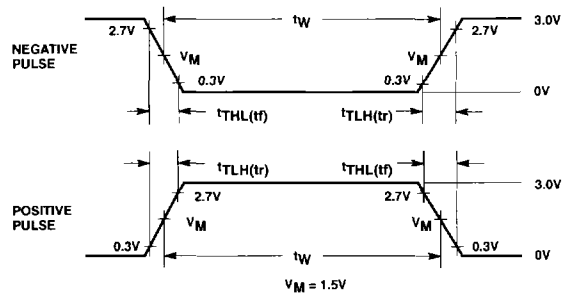
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

- R_L = Load Resistor; see AC Characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
- V_X = Unlocked pins must be held at: $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS

Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$