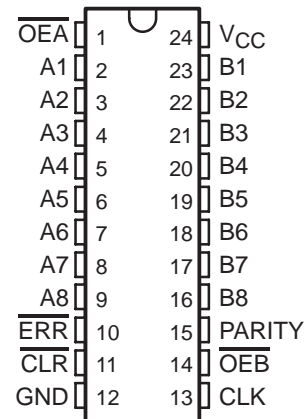


# SN74BCT29834 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

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- BiCMOS Process With TTL Inputs and Outputs
- BiCMOS Design Reduces Standby Current
- Flow-Through Pinout (All Inputs on Opposite Side From Outputs)
- Functionally Equivalent to SN74ALS29834 and AMD Am29834
- High-Speed Bus Transceiver With Parity Generator/Checker
- Parity-Error Flag With Open-Collector Output
- Available Register For Storage of the Parity-Error Flag
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)

DW OR NT PACKAGE  
(TOP VIEW)



## description

The SN74BCT29834 is an 8-bit to 9-bit parity transceiver designed for asynchronous communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the parity-error ( $\overline{ERR}$ ) output will indicate whether or not an error in the B data has occurred. The output-enable ( $\overline{OEA}$ ,  $\overline{OEB}$ ) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector parity-error flag ( $\overline{ERR}$ ).  $\overline{ERR}$  is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the clear ( $\overline{CLR}$ ) input. When both  $\overline{OEA}$  and  $\overline{OEB}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition which gives the designer more system diagnostic capability. The SN74BCT29834 provides inverting logic.

The SN74BCT29834 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of L's	A	B	PARITY	$\overline{ERR}‡$	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ data to B bus and generate parity
H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Clear error-flag register
H	H	H	No↑	X	X	Z	Z	Z	NC	Isolation§
		L	No↑	X					H	
		H	↑	Odd Even					L H	
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume the  $\overline{ERR}$  output was previously high.

§ In this mode, the  $\overline{ERR}$  output, when enabled, shows inverted parity of the A bus.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



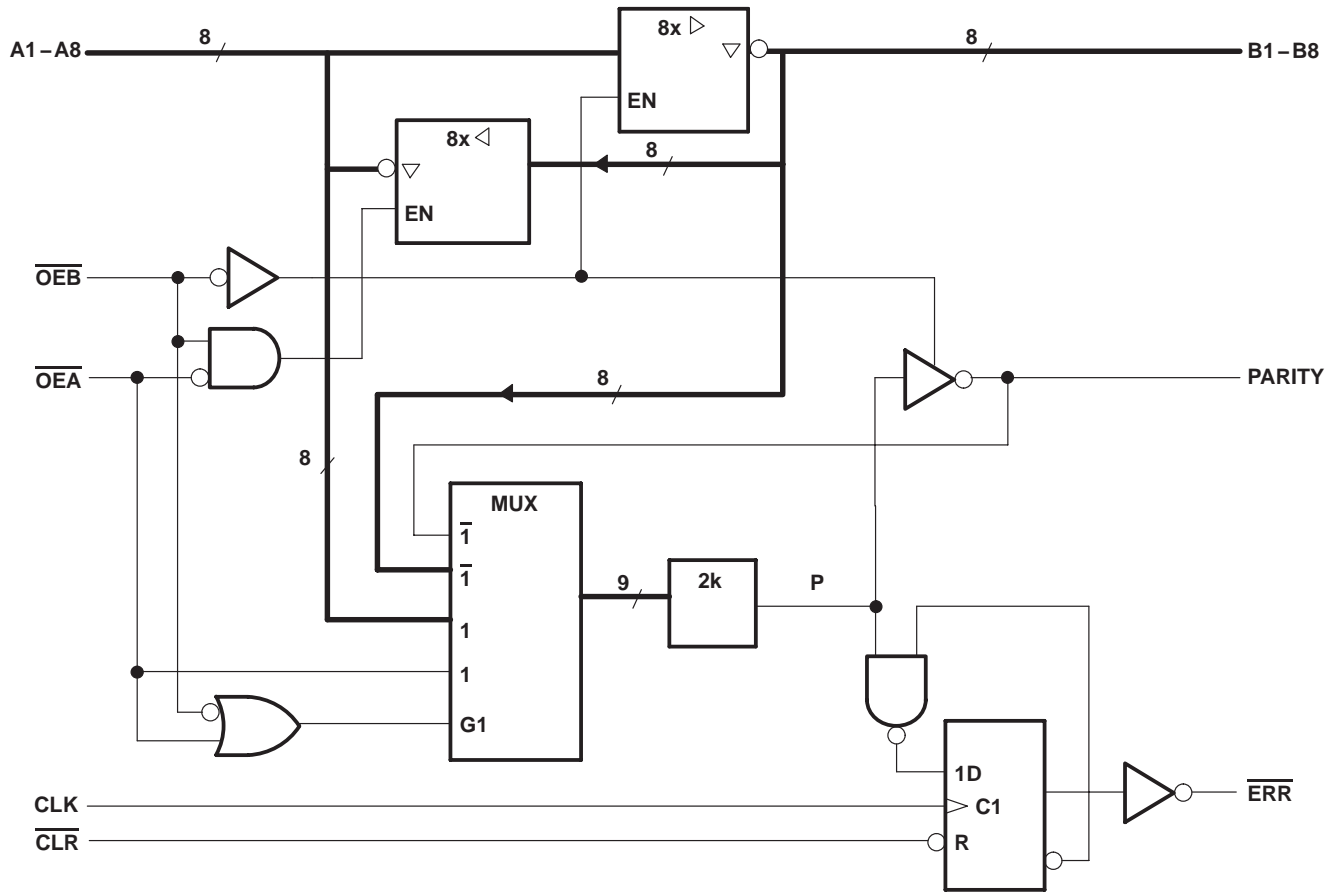
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# SN74BCT29834

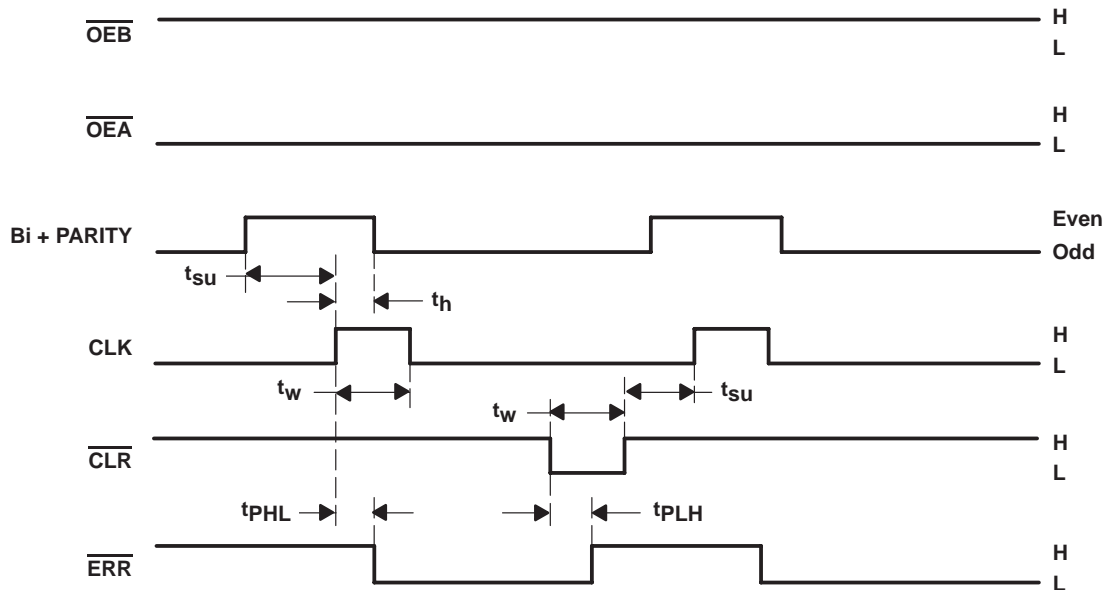
## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

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functional logic diagram (positive logic)



**error-flag waveforms**



**ERROR-FLAG FUNCTION TABLE**

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT P	$\overline{ERR}_{n-1}^\dagger$	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

$^\dagger \overline{ERR}_{n-1}$  represents the state of the  $\overline{ERR}$  output before any changes at  $\overline{CLR}$ , CLK, or point P.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

- Supply voltage,  $V_{CC}$  ..... 7 V
- Input voltage,  $V_I$  ..... 7 V
- Voltage applied to a disabled I/O port ..... 5.5 V
- Operating free-air temperature range ..... 0°C to 70°C
- Storage temperature range ..... -65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



# SN74BCT29834

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage, $\overline{ERR}$			2.4	V
$I_{OH}$	High-level output current			-24	mA
$I_{OL}$	Low-level output current			48	mA
$T_A$	Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	All inputs/outputs except $\overline{ERR}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4			V
			$I_{OH} = -24\text{ mA}$	2			
$I_{OH}$	$\overline{ERR}$	$V_{CC} = 4.5\text{ V}$ ,	$V_{OH} = 2.4\text{ V}$			20	μA
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 48\text{ mA}$		0.35	0.5	V
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			0.1	mA
$I_{IH}‡$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	μA
$I_{IL}‡$	Data	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.2	mA
	Control					-0.75	
$I_{OS}§$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-75		-250	mA
$I_{CCL}$		$V_{CC} = 5.5\text{ V}$ ,	Outputs open		55	80	mA
$I_{CCZ}$		$V_{CC} = 5.5\text{ V}$ ,	Outputs open		30	45	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ These parameters include off-state output current for I/O ports only.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

### timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
$t_w$	Pulse duration	CLK high	10	ns
		CLK low	10	
		$\overline{CLR}$ low	10	
$t_{su}$	Setup time before CLK↑	Bi and PARITY	12	ns
		$\overline{CLR}$ inactive	12	
$t_h$	Hold time after CLK↑	0		ns



# SN74BCT29834

## 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $C_L = 50$ pF, $R_1 = 500$ $\Omega$ , $R_2 = 500$ $\Omega$ , $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_1 = 500$ $\Omega$ , $R_2 = 500$ $\Omega$ , $T_A = \text{MIN to MAX}^\dagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$	A or $\bar{B}$	$\bar{B}$ or A	1	5	7	1	8	ns
$t_{PHL}$			1.5	4	6	1.5	7	
$t_{PLH}$	A	PARITY	1.5	10	13	1.5	15	ns
$t_{PHL}$			1.5	8	10	1.5	15	
$t_{PZH}$	$\overline{OEA}$ or $\overline{OEB}$	A or $\bar{B}$	2	11	15	2	19	ns
$t_{PZL}$			2	15	19	2	21	
$t_{PHZ}$	$\overline{OEA}$ or $\overline{OEB}$	A or $\bar{B}$	2	8	11	2	15	ns
$t_{PLZ}$			2	13	17	2	21	
$t_{PLH}$	CLK	$\overline{ERR}$	1.5	7	10	1.5	12	ns
	$\overline{CLR}$		1.5	13	17	1.5	18	
$t_{PLH}$	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
$t_{PHL}$			1.5	10	13	1.5	15	

$^\dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74BCT29834DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74BCT29834DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	Samples Not Available
SN74BCT29834NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.



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