User's Guide
SLVU339–February 2010

TPS65721EVM

This user's guide provides an overview of the TPS65721EVM evaluation module, a description of the connector and test points, and setup instructions. Also included are the EVM schematic, board art, and bill of materials.

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1 Introduction

The TPS65721EVM-516 evaluation module (EVM) is a fully assembled and tested circuit for evaluating the TPS65721 2-Channel Power Management integrated circuit (IC).

1.1 Requirements

In order to operate this EVM, the following components must be connected and properly configured. All components and connectors are supplied in the EVM except for the host computer and the DC power supply. Software must be downloaded from the TI Web site at www.ti.com.

1.1.1 Software

To download the software that is necessary to operate the TPS65721EVM, check the TPS65721 product folder on the TI Web site (www.ti.com) .

1.1.2 Host Computer

A computer with a USB port is required to operate this EVM. The TPS65721 software runs on a personal computer (PC) and communicates with the EVM via the PC's USB port and the USB-to-GPIO interface.

PC Requirements :

- Windows™ 2000 or XP operating system
- USB port
- Minimum of 30 MB of free hard disk space (100 MB recommended)
- Minimum of 256 MB of RAM

1.1.3 Power Supply Requirements

A DC power supply capable of delivering 5 V at 1 A is required to operate this EVM.

1.2 Applications

- Bluetooth headsets
- Handheld applications

1.3 Features

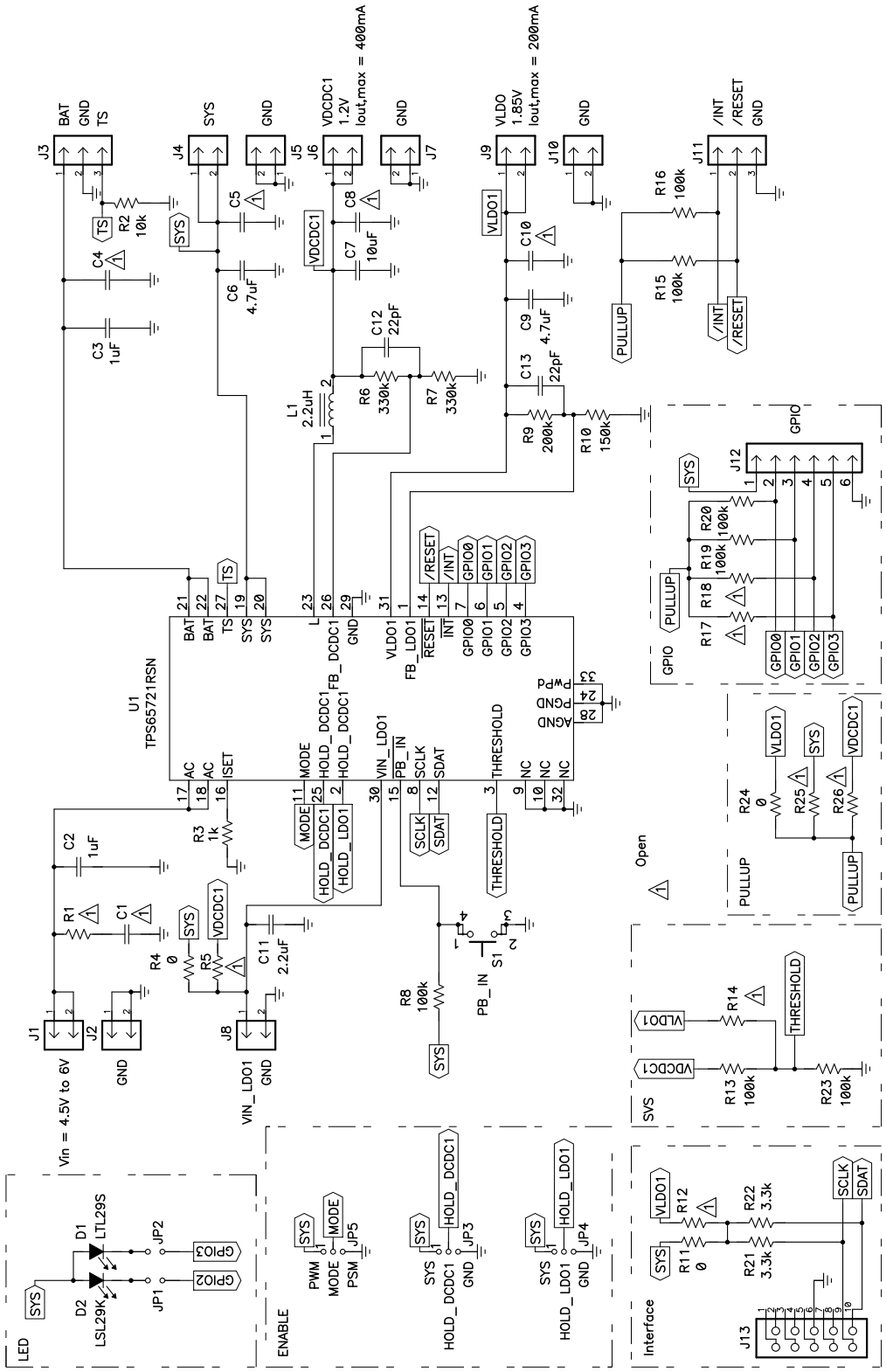
- Input voltage rating
- Output voltage adjustable via I^2C™ Interface
- Battery charger with power path management
- 300-mA charge current
- 400-mA step-down converter for TPS65721
- 2.25-MHz switching frequency
- 1 General-purpose 200-mA LDO

2 TPS65721EVM Electrical Performance Specifications

Table 1. TPS65721EVM Electrical and Performance Specifications

Symbol	Parameter	Notes and Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{AC}	Input Voltage AC		4.35		28	V
V_{IN_DCDC1}	Input Voltage DCDC1		2.1		5.6	V
V_{IN_LDO1}	Input Voltage LDO1		1.8		6.6	V
$I_{AC,max}$	Input Current	Bit <AC input current1, AC input current0> = 00	90	95	100	mA
		Bit <AC input current1, AC input current0> = 01 or 10	450	475	500	
V_{UVLO}	UVLO	V_{AC} rising	3.2	3.3	3.45	V
$V_{HYS\ -UVLO}$	UVLO Hysteresis	V_{AC} falling	200		300	mV
Output Characteristics						
VSYS	Voltage range at SYS		2.2		5.6	V
V_{DCDC1}	Output Voltage DCDC1	V_{IN} = Nom, I_{OUT} = Nom		1.2		V
	Output Voltage Accuracy DCDC1	V_{IN} = 2.3V to 5.6V , PFM operation , 0mA to IOUT,max		1%	2%	
			–2%	2%		
	Load Regulation	PWM operation		0.5%		
$I_{OUT,DCDC1}$	Output Current DCDC1	VIN = MIN to MAX			400	mA
I_{LIMF}	Forward Current Limit high- and low-side MOSFET	VIN = 2.3 V to 5.6 V	625	850	1150	mA
	Dropout Voltage LDO1	$V_{IN,LDO}$ = 2.05 V, I_{OUT} = 200 mA		120		mV
VLDO1	Output Voltage LDO1	V_{IN} = Nom, I_{OUT} = Nom, (including 1% resistor tolerance), as configured on the EVM	1.73	1.8	1.88	V
	Output Voltage Accuracy LDO1		–1.5 %		2.5%	
	Output Current of LDO1				200	mA
	Line Regulation LDO1		–1%		1%	
	Load Regulation LDO1		–1%		2%	
Systems Characteristics						
F_{SW}	Switching Frequency		2030	2250	2480	kHz
ηpk	Peak Efficiency	V_{IN} = Nom			95%	
η	Full Load Efficiency	V_{IN} =3.6, V_{OUT} =1.8, I_{OUT} = 400mV, MIPSA25202R2		85%		

3 TPS65721EVM Schematic



For Reference Only, See Table 2 for Specific Values

Figure 1. TPS65721EVM Schematic

4 Connector and Test Point Descriptions

4.1 Enable Jumpers/Switches

4.1.1 J1 – VIN

This header is the positive connection to the input power supply. The power supply must be connected between J1 and J2 (GND). The leads to the input supply must be twisted and kept as short as possible. The input voltage has to be between 4.35 V and 6 V.

4.1.2 J2 – GND

This header is the return connection to the input power supply. Connect the power supply between J2 and J1 (VIN). The leads to the input supply must be twisted and kept as short as possible. The input voltage has to be between 4.35 V and 6 V.

4.1.3 J3 – BAT/GND/TS

Connect your battery's positive connection to pin 1 of J3 and negative connection to pin 2 of J3. The battery thermistor can be connected to pin 3 of J3. if an external thermistor is used, R2 must be removed.

4.1.4 J4 – SYS

This header is the positive output of the power path.

4.1.5 J5 – GND

This header is the negative output of the power path.

4.1.6 J6 – VDCDC1

This header is the positive output of the VDCDC1 step-down converter. The output voltage of DCDC1 can be adjusted to any voltage between 0.6 V and VINDCDC1 with the external voltage divider R7 and R8.

The default setting is 1.2 V. VDCDC1 is capable of sourcing up to 200 mA. A load can be connected between J7 and J8 (GND).

4.1.7 J7 – GND

J8 is the return connection of VDCDC1 output rail. A load can be connected between J8 and J7 (VDCDC1).

4.1.8 J8 – VINLDO/GND

This header is the input supply for the LDO1 on the EVM. VINLDO1 is directly connected to SYS with R4. It also can be connected to VDCDC1 with R5.

An external power supply can be connected between J8 pin 1 (VINLDO) and pin 2 (GND). Note that the resistors R4 and R5 must be removed when supplying the LDO1 from an external power supply.

4.1.9 J9 – VLDO

This header is the positive output of the LDO1 linear regulator. The default output voltage of LDO1 is 1.85 V. VLDO1 can be adjusted via I2C interface in the range between.

LDO1 is capable of sourcing up to 300 mA. A load can be connected between J9 and J10 (GND).

4.1.10 J10 – GND

J10 is the return connection of LDO1 output rail. A load can be connected between J10 and J9 (VDCDC1).

4.1.11 J11 – $\overline{\text{INT}}$/ $\overline{\text{RESET}}$/GND

J11 pin 1 is connected to the open-drain output $\overline{\text{INT}}$. J11 pin 2 is connected to the open-drain output $\overline{\text{RESET}}$. All open-drain outputs are pulled up with a resistor to the pullup voltage PULLUP. Pullup is connected to VLDO1 with R10 on the EVM. PULLUP also can be connected to VIN and VDCDC1 with the resistors R20 and R21. J13 pin 3 is connected to GND.

4.1.12 J12 – SYS/GPIO0/GPIO1/GPIO2/GPIO3/SYS

Four GPIOs are available on this header.

- J12 pin 1 is connected to the SYS voltage.
- J12 pin 2 is connected to GPIO0.
- J12 pin 3 is connected to GPIO1.
- J12 pin 4 is connected to GPIO2.
- J12 pin 5 is connected to GPIO3.

4.1.13 J13

J13 is the interface connector for the I2C interface. Connect a 10-pin ribbon cable between J13 and the USB-to-GPIO interface.

4.1.14 JP1

JP1 connects the cathode of the LED D2 to GPIO2. If GPIO2 is configured as a current sink, JP1 can be removed to measure the current through the LED with an ammeter.

If GPIO2 is configured as an input or output, JP1 must be removed to disconnect the LED D2.

4.1.15 JP2

JP2 connects the cathode of the LED D1 to GPIO3. If GPIO3 is configured as a current sink, JP2 can be removed to measure the current through the LED with an ammeter.

If GPIO3 is configured as an input or output, JP2 must be removed to disconnect the LED D1.

4.1.16 JP3 – HOLD_DCDC1

Connect a shorting jumper between HOLD_DCDC1 and SYS to enable DCDC1. Note that if a power supply is connected to AC, DCDC1 is enabled independent of the status of HOLD_DCDC1.

If the IC is supplied from BAT, DCDC1 is enabled when $\overline{\text{PB\_IN}}$ is pulled low. To keep DCDC1 enabled, HOLD_DCDC1 must be pulled high before $\overline{\text{PB\_IN}}$ is released high.

4.1.17 JP4 – HOLD_LDO1

Connect a shorting jumper between HOLD_LDO1 and SYS to enable LDO1. Note that if a power supply is connected to AC LDO is enabled independent of the status of HOLD_LDO1.

If the IC is supplied from BAT, LDO is enabled when $\overline{\text{PB\_IN}}$ is pulled low. To keep LDO1 enabled, HOLD_LDO11 must be pulled high before $\overline{\text{PB\_IN}}$ is released high.

4.1.18 S1 – PB_IN

This is the Push-Button Input. Pressing S1 pulls $\overline{\text{PB\_IN}}$ to GND and therefore enables DCDC1 and LDO1. To keep DCDC1/LDO1 enabled, the individual HOLD pins must be pulled high before $\overline{\text{PB\_IN}}$ is released high.

If a power supply is present at AC, both DCDC1 and LDO1 are enabled independent of the HOLD pins.

5 Setup

5.1 Software Setup

To download the software, go the TPS65721 product folder on the TI Web site (www.ti.com). Download the software, and execute it to install the software.

5.2 Hardware Setup

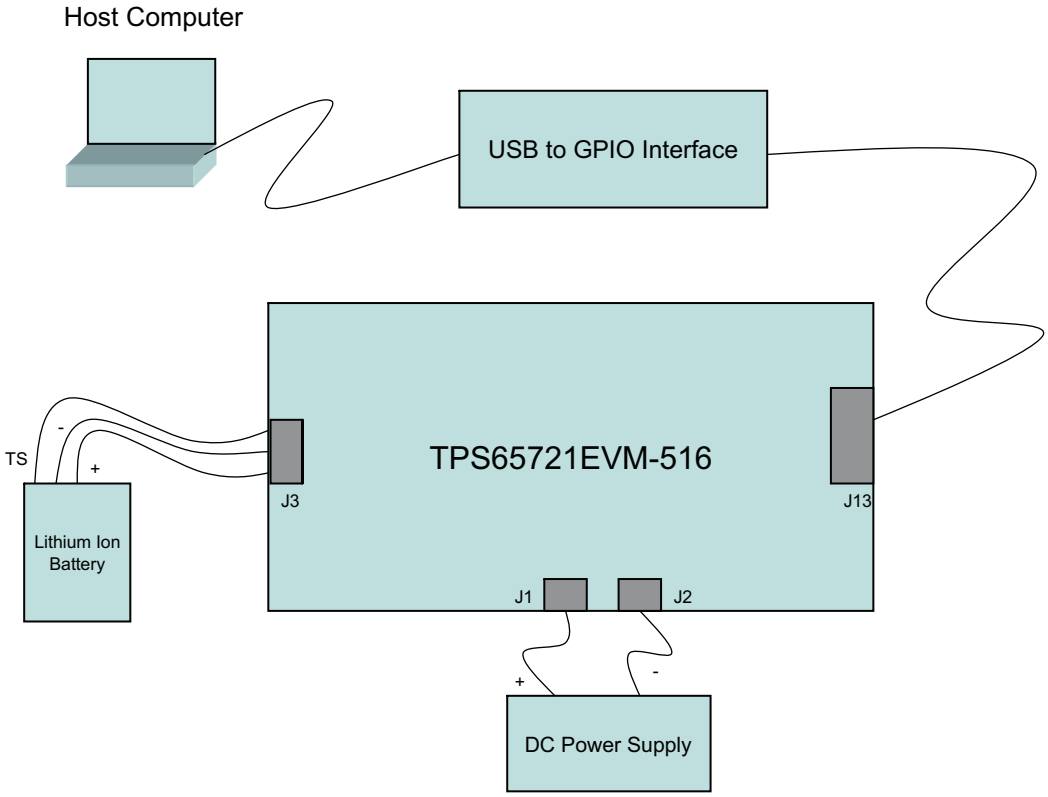


Figure 2. Hardware Board Connection

5.3 Running the Software

Click on the TPS65720_1EVM icon to start the software. If no icon appears on the host computer, then use the start button in the lower left corner of the screen to browse the program folders to find the software. The default directory for software installation is Program Files\Texas Instruments\TPS65720_1EVM.

Once started, the software dialog box appears (see Figure 3), and asks to select whether a TPS65720 or TPS65721 is connected.

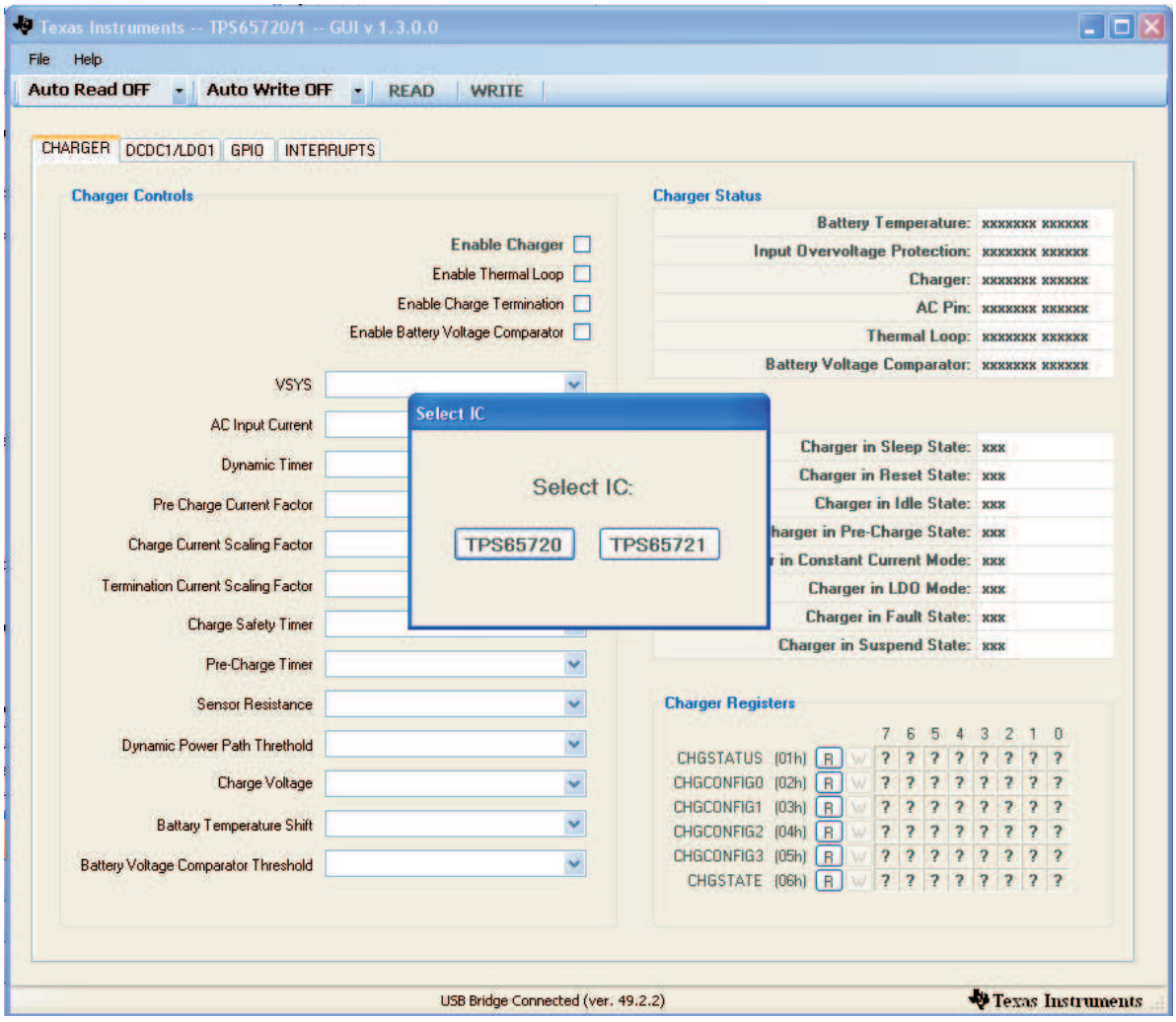


Figure 3. Starting the Software

Once the used device is selected, the software starts up (see Figure 4).

By clicking on the Tabs CHARGER , DCDC1/LDO1, GPIO, and INTERRUPTS, the user can navigate through the different Views .

The window that first appears allows control of all charger settings and shows all the charger status flags. In the CHARGER tab, the user can enable/disable the charger, change charger parameters as regulated output voltage on the Power Path (VSYS), charge voltage, safety timers, etc.

In the lower right corner of the window, all charger-related Charger Registers are displayed.

See the TPS65721 data sheet for detailed description on these registers.

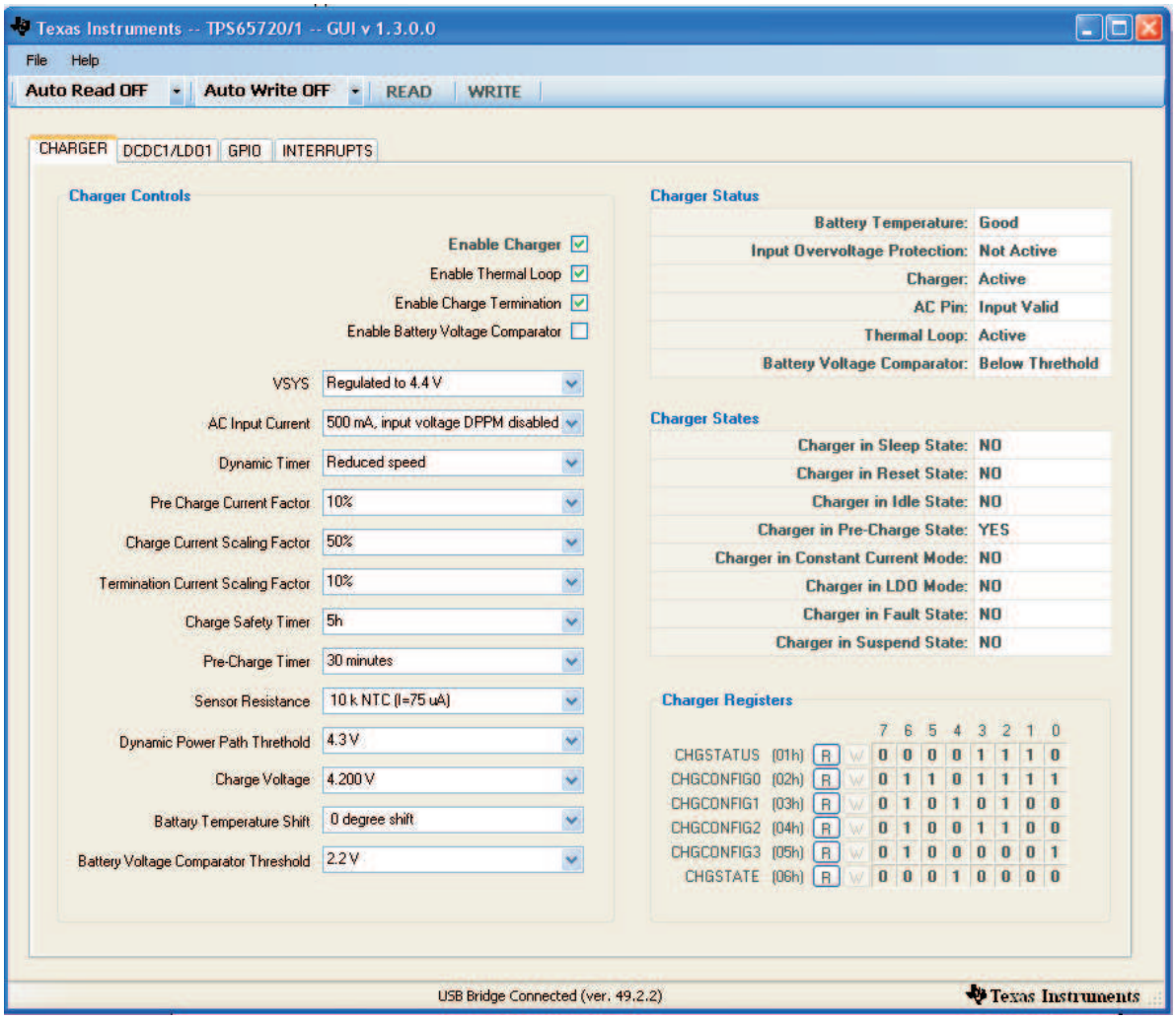


Figure 4. Software Charger View

The DCDC1/LDO1 control window (see Figure 5) allows control of the operating mode (PWM/PFM) for the DC/DC converter, output voltage of LDO1 (TPS65720 only), and shows the status flags related to DCDC1 and LDO1.

In the lower right corner of the window, all DCDC1/LDO1-related User Registers are displayed.

See the TPS65721 data sheet for a detailed description on these registers.

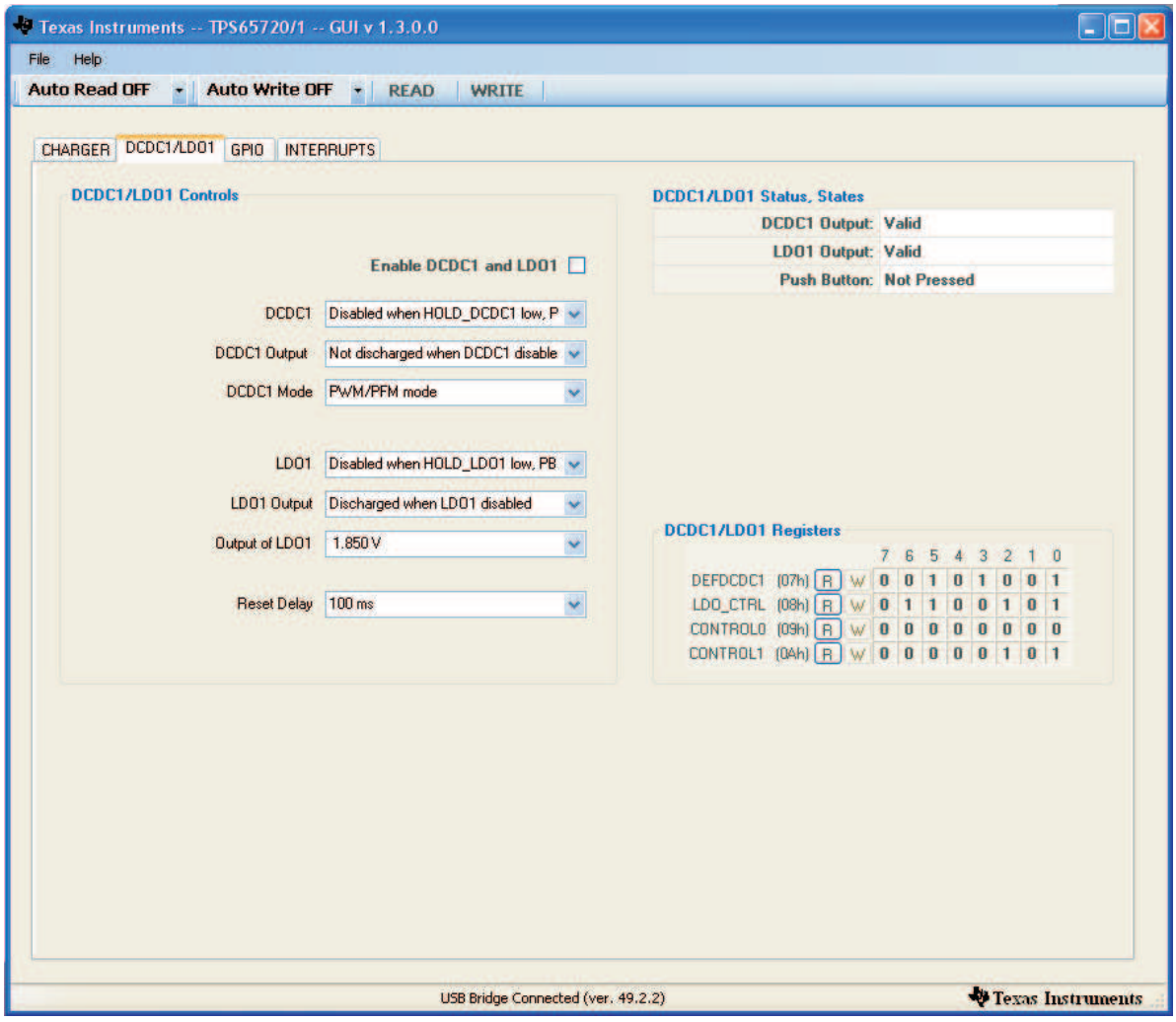


Figure 5. DCDC1/LDO1 View

The GPIO control window (see Figure 6) allows control of the fours GPIOs of the TPS65720/1. The GPIOs can be configured as input or output. In addition GPIO2 and GPIO3 can configured as current sink to drive an external LED.

In the lower right corner of the window, all GPIO-related User Registers are displayed.

See the TPS65721 data sheet for the detailed description on these registers.

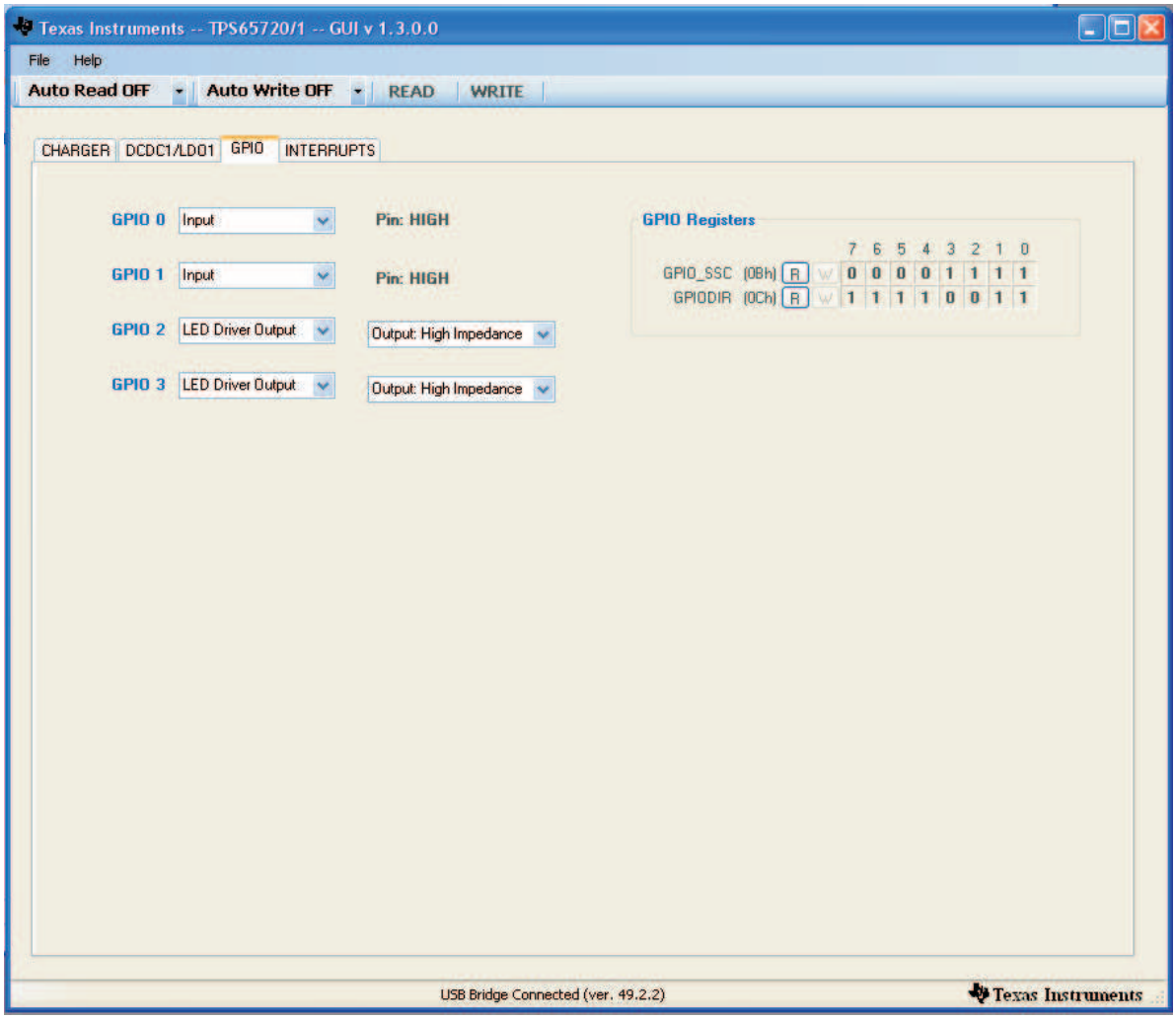


Figure 6. GPIO View

The INTERRUPT control window allows the user to configure and mask interrupts. The default setup is that all interrupts are masked. If an event is masked, it is ignored and no interrupt is generated. If an event is not masked, an interrupt is generated based on that event. If any interrupt is pending, the $\overline{\text{INT}}$ pin is driven low.

In the lower right corner of the window, all INTERRUPT-related User Registers are displayed.

See the TPS65721 data sheet for a detailed description on these registers.

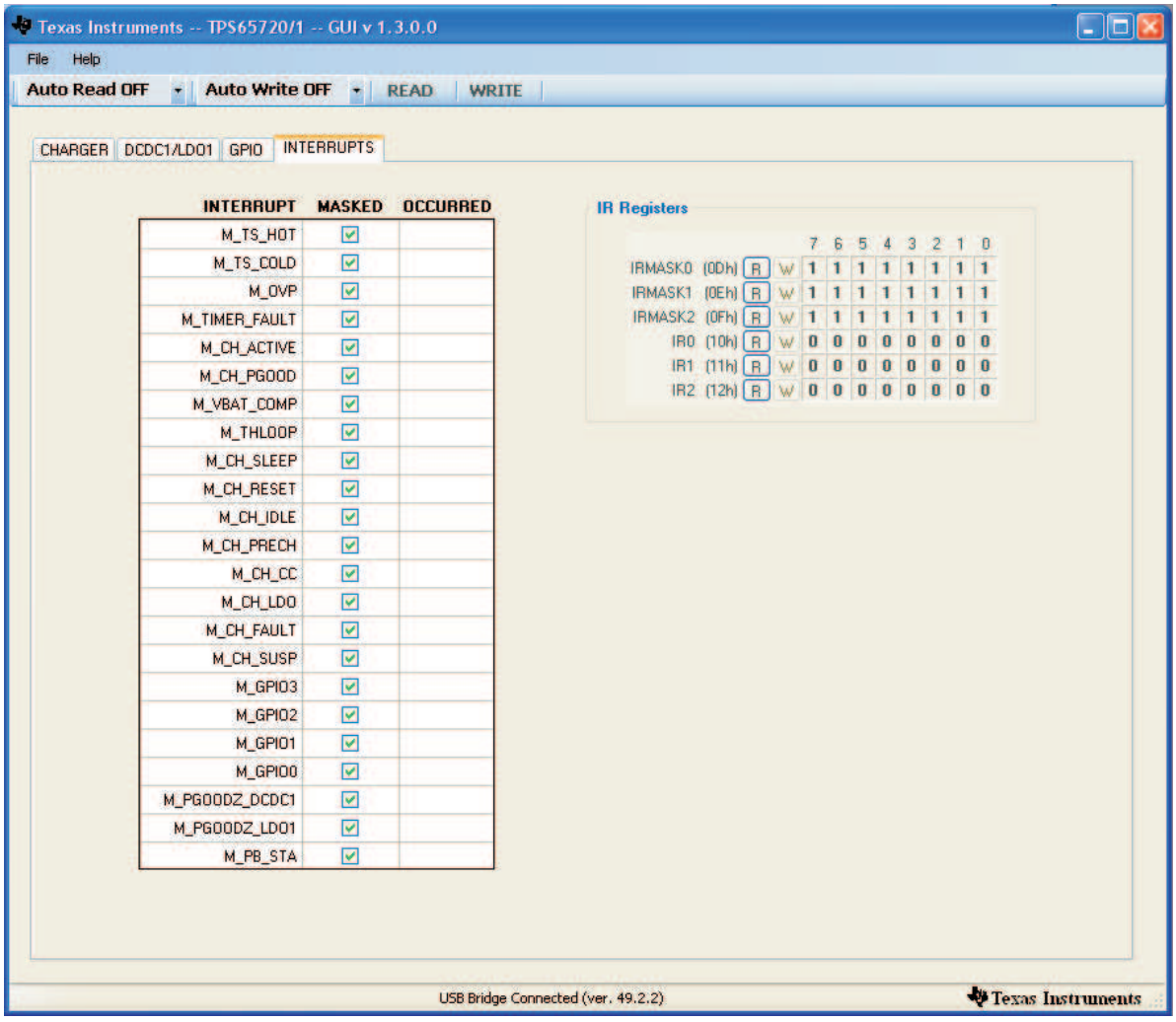


Figure 7. Interrupts View

6 TPS65721EVM Assembly Drawings and Layout

The following figures (Figure 8 through Figure 10) show the design of the TPS65721EVM printed-circuit board.

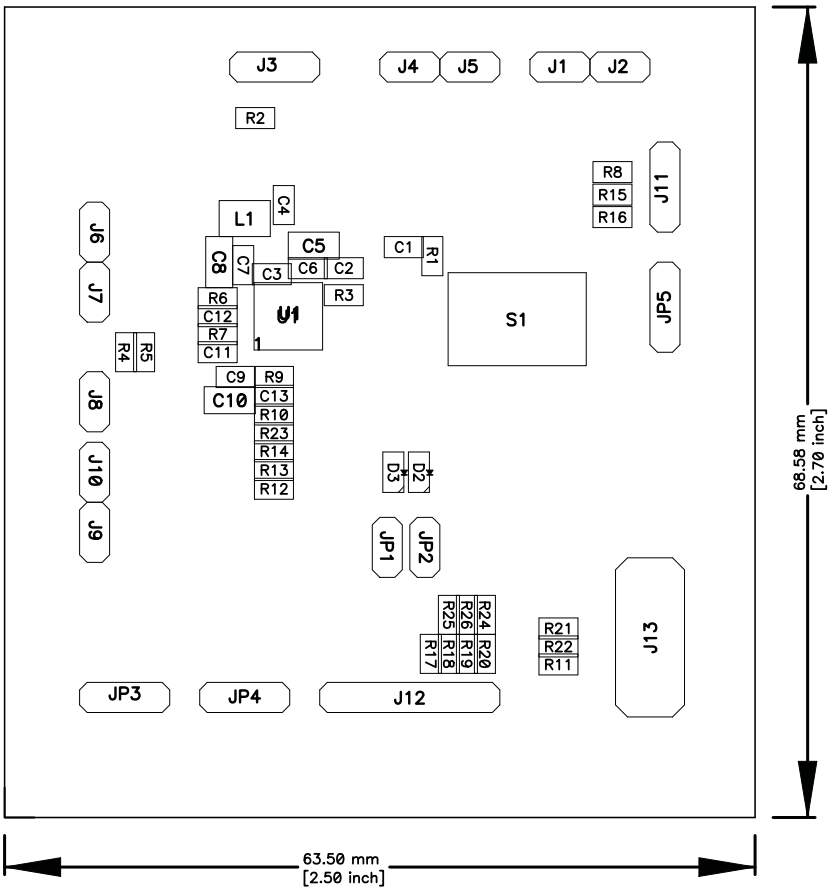


Figure 8. TPS65721EVM Component Placement (Viewed From Top)

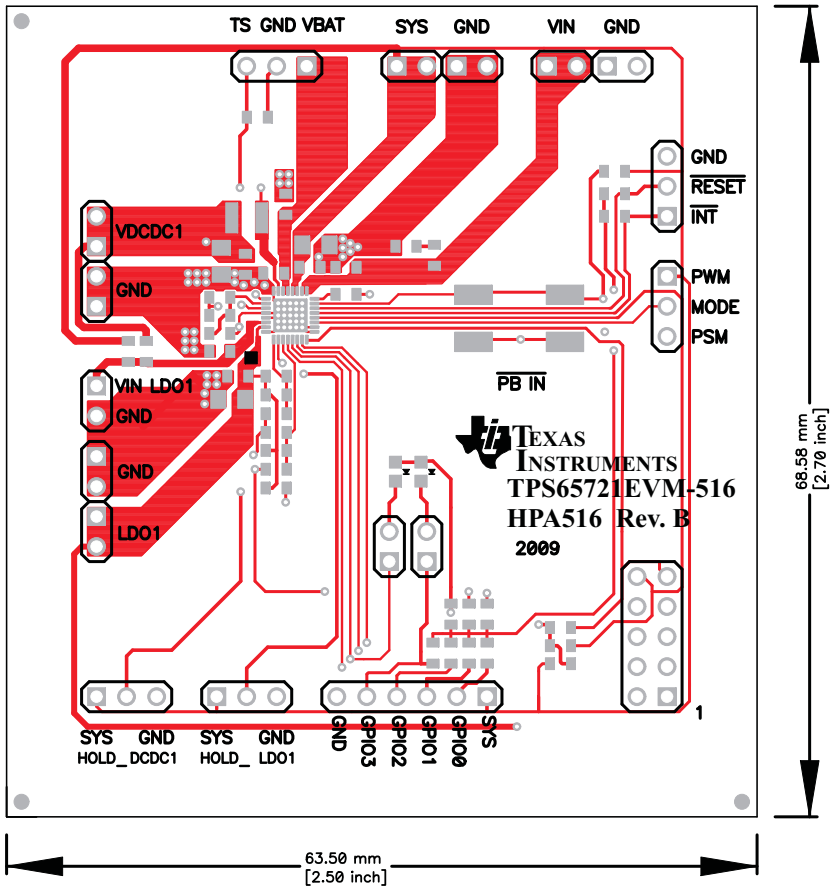


Figure 9. TPS65721EVM Top Copper (Viewed From Top)

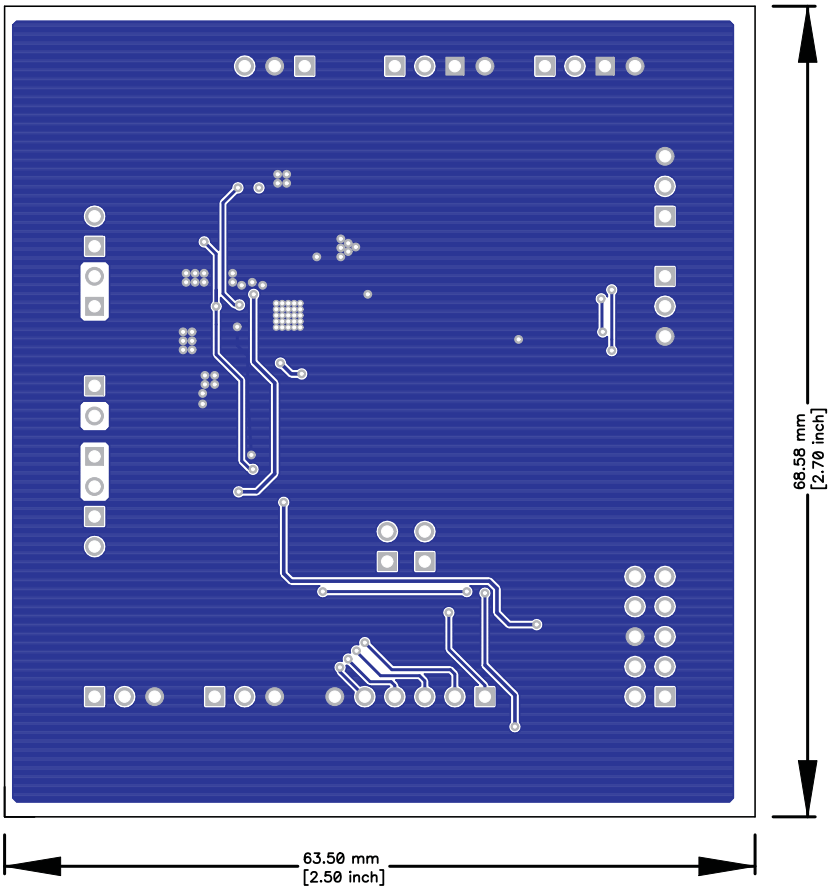


Figure 10. TPS65721EVM Bottom Copper (X-Ray View)

7 Bill of Materials

Table 2. HPA516B Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	open	Capacitor, Ceramic, 35V, X5R, 10%	0603		
0	C10	open	Capacitor, Ceramic, 6.3V, X5R, 10%	0805		
1	C11	2.2uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM155R60J22ME15D	Murata
2	C12, C13	22pF	Capacitor, Ceramic, 50V, COG, 5%	0603	GRM1885C1H220JA01D	Murata
1	C2	1uF	Capacitor, Ceramic, 35V, X5R, 10%	0603	GMK107BJ105K	Taiyo Yuden
1	C3	1uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	JMK107BJ105KK-T	Taiyo Yuden
0	C4	open	Capacitor, Ceramic, 10V, X7R, 10%	0603		
0	C5	open		0805		
2	C6, C9	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	GRM188R60J475K	Murata
1	C7	10uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J106ME47D	Murata
1	C8	open	Capacitor, Ceramic, 6.3V, X5R, 20%	0805	LMK212BJ475_G	Murata
1	D1	LTL29S	Diode LED, green, 60 mW, 15mA	0603	LT L29S-N2Q1-25	Osram
1	D2	LSL29K	Diode LED, red. 40 mW, 20mA	0603	LS L29K-G1H2-1	Osram
1	L1	2.2uH	Inductor, Power, 1.1 A, 110 milliohms	2.5 × 2.0 mm	MIPSA2520D1R0	FDK
0	R1, R5, R14, R17, R18, R25, R26	open	Resistor, Chip, 1/16W, 1%	0603	std	std
1	R10	150k	Resistor, Chip, 1/16W, 1%	0603	std	std
1	R11	0	Resistor, Chip, 1/16W, 5%	0603	std	std
1	R12	open	Resistor, Chip, 1/16W, 5%	0603	std	std
1	R2	10k	Resistor, Chip, 1/16W, 1%	0603	std	std
2	R21, R22	3.3k	Resistor, Chip, 1/16W, 5%	0603	std	std
1	R3	1k	Resistor, Chip, 1/16W, 1%	0603	std	std
2	R4, R24	0	Resistor, Chip, 1/16W, 1%	0603	std	std
2	R6, R7	330k	Resistor, Chip, 1/16W, 1%	0603	std	std
7	R8, R13, R15, R16, R19, R20, R23	100k	Resistor, Chip, 1/16W, 1%	0603	std	std
1	R9	200k	Resistor, Chip, 1/16W, 1%	0603	std	std
1	U1	TPS65721RSN	IC, PMU for Bluetooth Headsets	QFN-32	TPS65721RSM	TI
1	--		PCB, 2.2 In x 2.7 In x 0.062 In		HPA516	Any

Notes 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 4.35 V to 28 V and the output voltage range of 0.6 V to 5.6 V for dc/dc converter and 0.8 V to 3.3 V for LDO.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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