



CYPRESS

CY7C1347D

# 128K x 36 Synchronous-Pipelined Cache SRAM

## Features

- **Fast access times: 2.5 and 3.5 ns**
- **Fast clock speed: 250, 225, 200, and 166 MHz**
- **1.5-ns set-up time and 0.5-ns hold time**
- **Fast  $\overline{OE}$  access times: 2.5 ns and 3.5 ns**
- **Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)**
- **3.3V  $-5\%$  and  $+10\%$  power supply**
- **3.3V or 2.5V I/O supply**
- **5V tolerant inputs except I/Os**
- **Clamp diodes to  $V_{SS}$  at all inputs and outputs**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Three chip enables for depth expansion and address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write Cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down for portable applications**
- **JTAG boundary scan**
- **JEDEC standard pinout**
- **Low profile 119-lead, 14-mm x 22-mm BGA (Ball Grid Array) and 100-pin TQFP packages**

## Functional Description

This Cypress Synchronous Burst SRAM employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

The CY7C1347D SRAM integrate 131,072 x 36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining Chip Enable ( $\overline{CE}$ ), depth-expansion Chip Enables ( $\overline{CE2}$  and  $\overline{CE3}$ ), Burst Control Inputs (ADSC, ADSP, and ADV), Write Enables (BWA, BWb, BWc, BWd, and BWE), and Global Write (GW).

Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and Burst Mode Control (MODE). The data outputs (Q), enabled by  $\overline{OE}$ , are also asynchronous.

Addresses and chip enables are registered with either Address Status Processor (ADSP) or Address Status Controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate self-timed Write cycle. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BWA controls DQa. BWb controls DQb. BWc controls DQc. BWD controls DQd. BWA, BWb, BWc, and BWD can be active only with BWE being LOW. GW being LOW causes all bytes to be written.

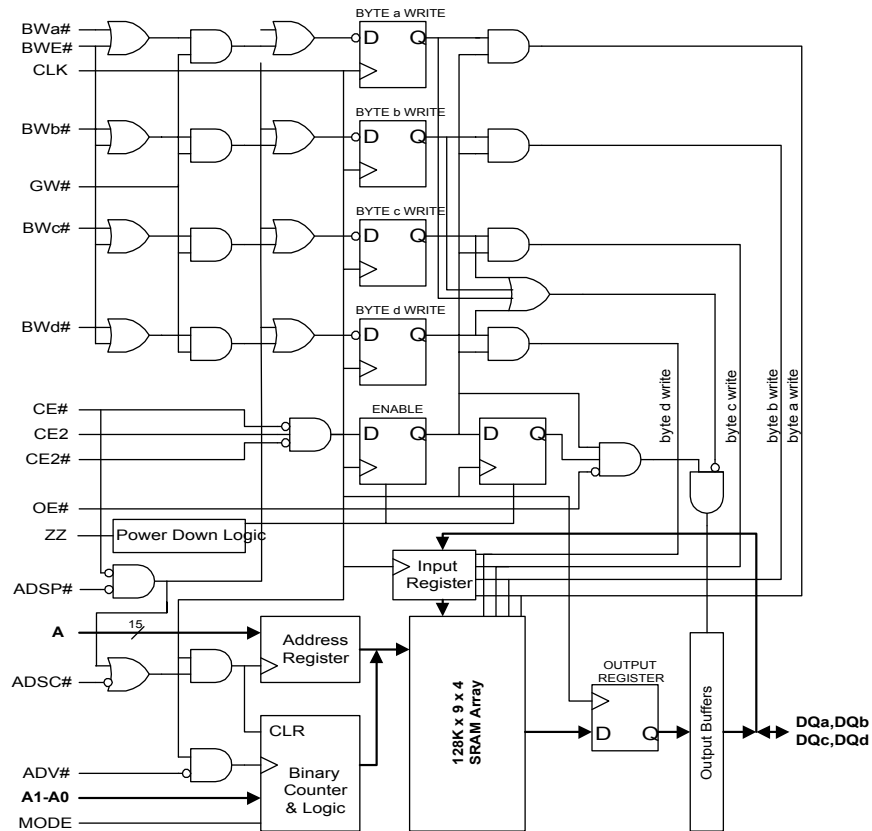
Four pins are used to implement JTAG test capabilities: Test Mode Select (TMS), Test Data-in (TDI), Test Clock (TCK), and Test Data-out (TDO). The JTAG circuitry is used to serially shift data to and from the device. JTAG inputs use LVTTTL/LVCMOS levels to shift data during this testing mode of operation.

The CY7C1347D operates from a +3.3V power supply. All inputs and outputs are LVTTTL-compatible

## Selection Guide

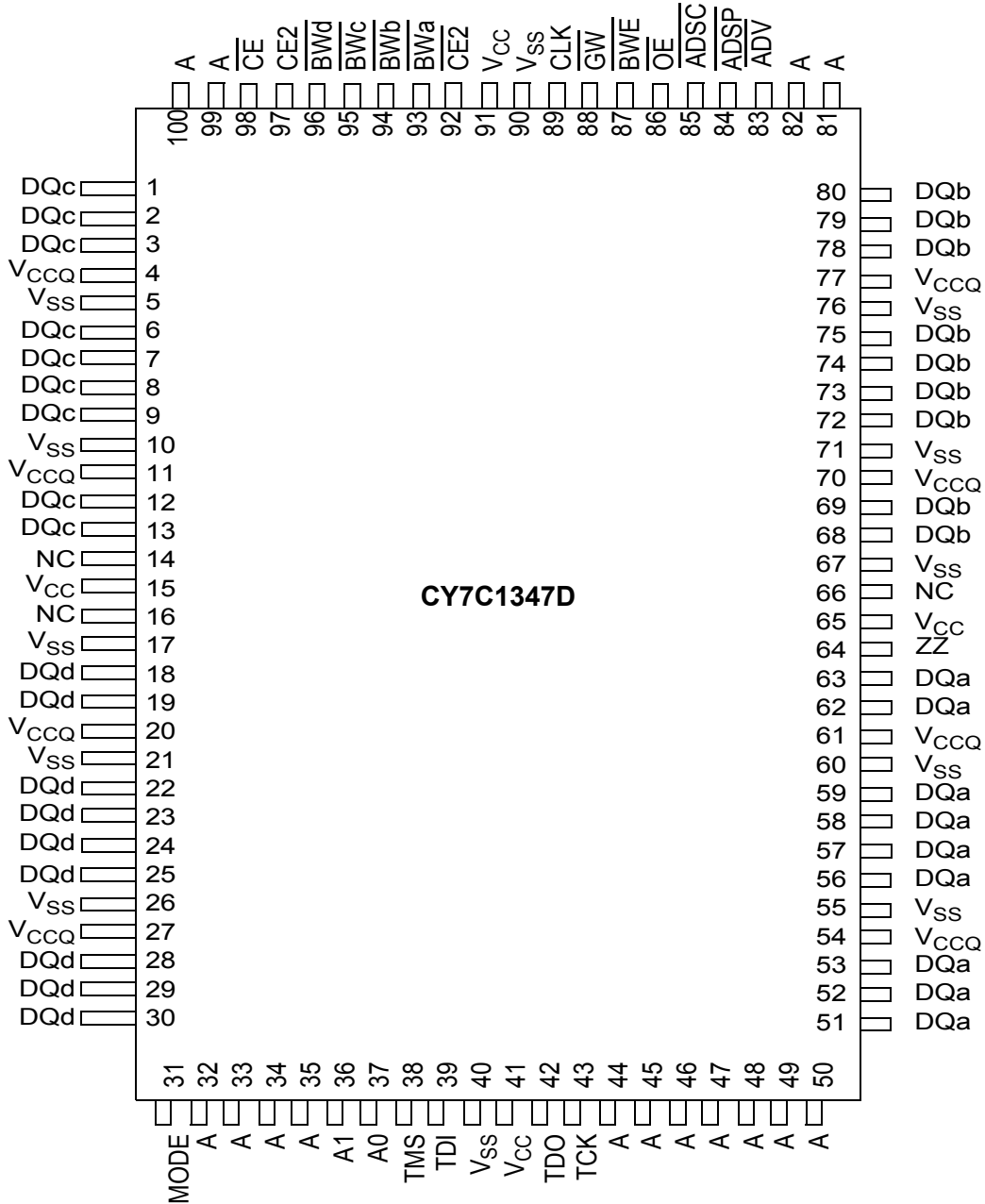
|                                   | CY7C1347D-250 | CY7C1347D-225 | CY7C1347D-200 | CY7C1347D-166 |
|-----------------------------------|---------------|---------------|---------------|---------------|
| Maximum Access Time (ns)          | 2.5           | 2.5           | 2.5           | 3.5           |
| Maximum Operating Current (mA)    | 450           | 400           | 360           | 300           |
| Maximum CMOS Standby Current (mA) | 10            | 10            | 10            | 10            |

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Functional Block Diagram—CY7C1347D<sup>[1]</sup>**

**Note:**

1. The functional block diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Pin Configurations**
**100-Pin TQFP  
Top View**

**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Pin Configurations** (continued)

**119-Ball BGA  
Top View**

|          | 1                | 2               | 3               | 4               | 5               | 6               | 7                |
|----------|------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| <b>A</b> | V <sub>CCQ</sub> | A               | A               | ADSP            | A               | A               | V <sub>CCQ</sub> |
| <b>B</b> | NC               | CE2             | A               | ADSC            | A               | CE2             | NC               |
| <b>C</b> | NC               | A               | A               | V <sub>CC</sub> | A               | A               | NC               |
| <b>D</b> | DQc              | DQc             | V <sub>SS</sub> | NC              | V <sub>SS</sub> | DQb             | DQb              |
| <b>E</b> | DQc              | DQc             | V <sub>SS</sub> | CE              | V <sub>SS</sub> | DQb             | DQb              |
| <b>F</b> | V <sub>CCQ</sub> | DQc             | V <sub>SS</sub> | OE              | V <sub>SS</sub> | DQb             | V <sub>CCQ</sub> |
| <b>G</b> | DQc              | DQc             | BWc             | ADV             | BWb             | DQb             | DQb              |
| <b>H</b> | DQc              | DQc             | V <sub>SS</sub> | GW              | V <sub>SS</sub> | DQb             | DQb              |
| <b>J</b> | V <sub>CCQ</sub> | V <sub>CC</sub> | NC              | V <sub>CC</sub> | NC              | V <sub>CC</sub> | V <sub>CCQ</sub> |
| <b>K</b> | DQd              | DQd             | V <sub>SS</sub> | CLK             | V <sub>SS</sub> | DQa             | DQa              |
| <b>L</b> | DQd              | DQd             | BWd             | NC              | BWa             | DQa             | DQa              |
| <b>M</b> | V <sub>CCQ</sub> | DQd             | V <sub>SS</sub> | BWE             | V <sub>SS</sub> | DQa             | V <sub>CCQ</sub> |
| <b>N</b> | DQd              | DQd             | V <sub>SS</sub> | A1              | V <sub>SS</sub> | DQa             | DQa              |
| <b>P</b> | DQd              | DQd             | V <sub>SS</sub> | A0              | V <sub>SS</sub> | DQa             | DQa              |
| <b>R</b> | NC               | A               | MODE            | V <sub>CC</sub> | NC              | A               | NC               |
| <b>T</b> | NC               | NC              | A               | A               | A               | NC              | ZZ               |
| <b>U</b> | V <sub>CCQ</sub> | TMS             | TDI             | TCK             | TDO             | NC              | V <sub>CCQ</sub> |

**CY7C1347D Pin Descriptions**

| BGA Pins  | QFP Pins   | Name                     | Type                  | Description  |
|---|--|--------------------------|-----------------------|--|
| 4P<br>4N<br>2A, 3A, 5A, 6A,<br>3B, 5B, 2C, 3C,<br>5C, 6C, 2R, 6R,<br>3T, 4T, 5T | 37<br>36<br>35, 34, 33, 32,<br>100, 99, 82, 81,<br>44, 45, 46, 47,<br>48, 49, 50 | A0<br>A1<br>A            | Input-<br>Synchronous | Addresses: These inputs are registered and must meet the set-up and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.   |
| 5L<br>5G<br>3G<br>3L  | 93<br>94<br>95<br>96   | BWa<br>BWb<br>BWc<br>BWd | Input-<br>Synchronous | Byte Write: A <u>byte write</u> is LOW for a Write cycle and HIGH for a Read cycle. <u>BWa</u> controls DQa. <u>BWb</u> controls DQb. <u>BWc</u> controls DQc. <u>BWd</u> controls DQd. Data I/O are high impedance if either of these inputs are LOW, conditioned by BWE being LOW. |
| 4M  | 87   | BWE                      | Input-<br>Synchronous | Write Enable: This active LOW input gates byte write operations and must meet the set-up and hold times around the rising edge of CLK.   |
| 4H  | 88   | GW                       | Input-<br>Synchronous | Global Write: This active LOW input allows a full 36-bit Write to occur independent of the BWE and BWn lines and must meet the set-up and hold times around the rising edge of CLK.  |
| 4K  | 89   | CLK                      | Input-<br>Synchronous | Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet set-up and hold times around the clock's rising edge.  |
| 4E  | 98   | CE                       | Input-<br>Synchronous | Chip Enable: This active LOW input is used to enable the device and to gate ADSP.  |
| 6B  | 92   | CE2                      | Input-<br>Synchronous | Chip Enable: This active LOW input is used to enable the device.   |
| 2U  | 38   | TMS                      | Input                 | IEEE 1149.1 test inputs. LVTTTL-level inputs. If JTAG feature is not utilized, this pin can be disconnected or connected to V <sub>cc</sub> .  |

**CY7C1347D Pin Descriptions** (continued)

| BGA Pins   | QFP Pins   | Name | Type   | Description  |
|--|------------|------|--------|--|
| 2U   | 39         | TDI  | Input  | IEEE 1149.1 test inputs. LVTTTL-level inputs. If JTAG feature is not utilized, this pin can be disconnected or connected to V <sub>CC</sub> .                    |
| 3U   | 43         | TCK  | Input  | IEEE 1149.1 test inputs. LVTTTL-level inputs. If JTAG feature is not utilized, this pin can be disconnected or connected to V <sub>SS</sub> or V <sub>CC</sub> . |
| 5U   | 42         | TDO  | Output | IEEE 1149.1 test output. LVTTTL-level output. If JTAG feature is not utilized, this pin should be disconnected.  |
| 1B, 7B, 1C, 7C, 4D, 3J, 5J, 4L, 1R, 5R, 7R, 1T, 2T, 6T, 6U | 14, 16, 66 | NC   | –      | No Connect: These signals are not internally connected.  |

**Burst Address Table (MODE = NC/V<sub>CC</sub>)**

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| A...A00                  | A...A01                   | A...A10                  | A...A11                   |
| A...A01                  | A...A00                   | A...A11                  | A...A10                   |
| A...A10                  | A...A11                   | A...A00                  | A...A01                   |
| A...A11                  | A...A10                   | A...A01                  | A...A00                   |

**Burst Address Table (MODE = GND)**

| First Address (external) | Second Address (internal) | Third Address (internal) | Fourth Address (internal) |
|--------------------------|---------------------------|--------------------------|---------------------------|
| A...A00                  | A...A01                   | A...A10                  | A...A11                   |
| A...A01                  | A...A10                   | A...A11                  | A...A00                   |
| A...A10                  | A...A11                   | A...A00                  | A...A01                   |
| A...A11                  | A...A00                   | A...A01                  | A...A10                   |

**Truth Table** [2, 3, 4, 5, 6, 7]

| Operation                    | Address Used | $\overline{\text{CE}}$ | $\overline{\text{CE2}}$ | CE2 | $\overline{\text{ADSP}}$ | $\overline{\text{ADSC}}$ | $\overline{\text{ADV}}$ | $\overline{\text{Write}}$ | $\overline{\text{OE}}$ | CLK | DQ     |
|------------------------------|--------------|------------------------|-------------------------|-----|--------------------------|--------------------------|-------------------------|---------------------------|------------------------|-----|--------|
| Deselected Cycle, Power-down | None         | H                      | X                       | X   | X                        | L                        | X                       | X                         | X                      | L-H | High-Z |
| Deselected Cycle, Power-down | None         | L                      | X                       | L   | L                        | X                        | X                       | X                         | X                      | L-H | High-Z |
| Deselected Cycle, Power-down | None         | L                      | H                       | X   | L                        | X                        | X                       | X                         | X                      | L-H | High-Z |
| Deselected Cycle, Power-down | None         | L                      | X                       | L   | H                        | L                        | X                       | X                         | X                      | L-H | High-Z |
| Deselected Cycle, Power-down | None         | L                      | H                       | X   | H                        | L                        | X                       | X                         | X                      | L-H | High-Z |
| Read Cycle, Begin Burst      | External     | L                      | L                       | H   | L                        | X                        | X                       | X                         | L                      | L-H | Q      |
| Read Cycle, Begin Burst      | External     | L                      | L                       | H   | L                        | X                        | X                       | X                         | H                      | L-H | High-Z |
| Write Cycle, Begin Burst     | External     | L                      | L                       | H   | H                        | L                        | X                       | L                         | X                      | L-H | D      |
| Read Cycle, Begin Burst      | External     | L                      | L                       | H   | H                        | L                        | X                       | H                         | L                      | L-H | Q      |
| Read Cycle, Begin Burst      | External     | L                      | L                       | H   | H                        | L                        | X                       | H                         | H                      | L-H | High-Z |
| Read Cycle, Continue Burst   | Next         | X                      | X                       | X   | H                        | H                        | L                       | H                         | L                      | L-H | Q      |
| Read Cycle, Continue Burst   | Next         | X                      | X                       | X   | H                        | H                        | L                       | H                         | H                      | L-H | High-Z |
| Read Cycle, Continue Burst   | Next         | H                      | X                       | X   | X                        | H                        | L                       | H                         | L                      | L-H | Q      |
| Read Cycle, Continue Burst   | Next         | H                      | X                       | X   | X                        | H                        | L                       | H                         | H                      | L-H | High-Z |
| Write Cycle, Continue Burst  | Next         | X                      | X                       | X   | H                        | H                        | L                       | L                         | X                      | L-H | D      |
| Write Cycle, Continue Burst  | Next         | H                      | X                       | X   | X                        | H                        | L                       | L                         | X                      | L-H | D      |
| Read Cycle, Suspend Burst    | Current      | X                      | X                       | X   | H                        | H                        | H                       | H                         | L                      | L-H | Q      |
| Read Cycle, Suspend Burst    | Current      | X                      | X                       | X   | H                        | H                        | H                       | H                         | H                      | L-H | High-Z |

**Notes:**

- X means "Don't Care." H means logic HIGH. L means logic LOW.  
Write = L means  $[\overline{\text{BWE}} + \overline{\text{BWA}} \cdot \overline{\text{BWB}} \cdot \overline{\text{BWC}} \cdot \overline{\text{BWD}}] \cdot \text{GW}$  equals LOW. Write = H means  $[\overline{\text{BWE}} + \overline{\text{BWA}} \cdot \overline{\text{BWB}} \cdot \overline{\text{BWC}} \cdot \overline{\text{BWD}}] \cdot \text{GW}$  equals HIGH.  $\overline{\text{BWA}}$  enables write to DQa.  $\overline{\text{BWB}}$  enables write to DQb.  $\overline{\text{BWC}}$  enables write to DQc.  $\overline{\text{BWD}}$  enables write to DQd.
- All inputs except OE must meet set-up and hold times around the rising edge (LOW to HIGH) of CLK.
- Suspending burst generates wait cycle.
- For a write operation following a read operation,  $\overline{\text{OE}}$  must be HIGH before the input data required set-up time plus High-Z time for  $\overline{\text{OE}}$  and staying HIGH throughout the input data hold time.
- This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
- ADSP LOW along with chip being selected always initiates a Read cycle at the L-H edge of CLK. A Write cycle can be performed by setting  $\overline{\text{Write}}$  LOW for the CLK L-H edge of the subsequent wait cycle. Refer to Write timing diagram for clarification.



**Truth Table** (continued)<sup>[2, 3, 4, 5, 6, 7]</sup>

| Operation                  | Address Used | $\overline{\text{CE}}$ | $\overline{\text{CE2}}$ | CE2 | $\overline{\text{ADSP}}$ | $\overline{\text{ADSC}}$ | $\overline{\text{ADV}}$ | $\overline{\text{Write}}$ | $\overline{\text{OE}}$ | CLK | DQ     |
|----------------------------|--------------|------------------------|-------------------------|-----|--------------------------|--------------------------|-------------------------|---------------------------|------------------------|-----|--------|
| Read Cycle, Suspend Burst  | Current      | H                      | X                       | X   | X                        | H                        | H                       | H                         | L                      | L-H | Q      |
| Read Cycle, Suspend Burst  | Current      | H                      | X                       | X   | X                        | H                        | H                       | H                         | H                      | L-H | High-Z |
| Write Cycle, Suspend Burst | Current      | X                      | X                       | X   | H                        | H                        | H                       | L                         | X                      | L-H | D      |
| Write Cycle, Suspend Burst | Current      | H                      | X                       | X   | X                        | H                        | H                       | L                         | X                      | L-H | D      |

**Partial Truth Table for Read/Write**

| FUNCTION        | $\overline{\text{GW}}$ | $\overline{\text{BWE}}$ | $\overline{\text{BWa}}$ | $\overline{\text{BWb}}$ | $\overline{\text{BWc}}$ | $\overline{\text{BWd}}$ |
|-----------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Read            | H                      | H                       | X                       | X                       | X                       | X                       |
| Read            | H                      | L                       | H                       | H                       | H                       | H                       |
| Write one byte  | H                      | L                       | L                       | H                       | H                       | H                       |
| Write all bytes | H                      | L                       | L                       | L                       | L                       | L                       |
| Write all bytes | L                      | X                       | X                       | X                       | X                       | X                       |

**IEEE 1149.1 Serial Boundary Scan (JTAG)**
**Overview**

This device incorporates a serial boundary scan access port (TAP). This port is designed to operate in a manner consistent with IEEE Standard 1149.1-1990 (commonly referred to as JTAG), but does not implement all of the functions required for IEEE 1149.1 compliance. Certain functions have been modified or eliminated because their implementation places extra delays in the critical speed path of the device. Nevertheless, the device supports the standard TAP controller architecture (the TAP controller is the state machine that controls the TAPs operation) and can be expected to function in a manner that does not conflict with the operation of devices with IEEE Standard 1149.1-compliant TAPs. The TAP operates using LVTTTL/LVCMOS logic level signaling.

**Disabling the JTAG Feature**

It is possible to use this device without using the JTAG feature. To disable the TAP controller without interfering with normal operation of the device, TCK should be tied LOW ( $V_{SS}$ ) to prevent clocking the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be pulled up to  $V_{CC}$  through a resistor. TDO should be left unconnected. Upon power-up the device will come up in a reset state which will not interfere with the operation of the device.

**Test Access Port (TAP)**
**TCK –Test Clock (INPUT)**

Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.

**TMS – Test Mode Select (INPUT)**

The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

**TDI –Test Data In (INPUT)**

The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction register (refer to *Figure 1*). It is allowable to leave this pin unconnected if it is not used in an application. The pin is pulled up internally, resulting in a logic HIGH level. TDI is connected to the most significant bit (MSB) of any register (see *Figure 2*).

**TDO – Test Data Out (OUTPUT)**

The TDO output pin is used to serially clock data-out from the registers. The output that is active depending on the state of the TAP state machine (refer to *Figure 1*). Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO. TDO is connected to the least significant bit (LSB) of any register (see *Figure 2*).

**Performing a TAP Reset**

The TAP circuitry does not have a reset pin ( $\overline{\text{TRST}}$ , which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH ( $V_{CC}$ ) for five rising edges of TCK and pre-loads the instruction register with the IDCODE command. This type of reset does not affect the operation of the system logic. The reset affects test logic only.

At power-up, the TAP is reset internally to ensure that TDO is in a High-Z state.

**Test Access Port (TAP) Registers**
**Overview**

The various TAP registers are selected (one at a time) via the sequences of ones and zeros input to the TMS pin as the TCK is strobed. Each of the TAPs registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on subsequent falling edge of TCK. When a register is selected, it is connected between the TDI and TDO pins.

## Instruction Register

The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run test/idle or the various data register states. The instructions are three bits long. The register can be loaded when it is placed between the TDI and TDO pins. The parallel outputs of the instruction register are automatically preloaded with the IDCODE instruction upon power-up or whenever the controller is placed in the test-logic reset state. When the TAP controller is in the Capture-IR state, the two least significant bits of the serial instruction register are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

## Bypass Register

The bypass register is a single-bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the device TAP to another device in the scan chain with minimum delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

## Boundary Scan Register

The Boundary scan register is connected to all the input and bidirectional I/O pins (not counting the TAP pins) on the device. This also includes a number of NC pins that are reserved for future needs. There are a total of 70 bits for x36 device and 51 bits for x18 device. The boundary scan register, under the control of the TAP controller, is loaded with the contents of the device I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE-Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order table describes the order in which the bits are connected. The first column defines the bit's position in the boundary scan register. The MSB of the register is connected to TDI, and LSB is connected to TDO. The second column is the signal name and the third column is the bump number. The third column is the TQFP pin number and the fourth column is the BGA bump number.

## Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the device as described in the Identification Register Definitions table.

## TAP Controller Instruction Set

### Overview

There are two classes of instructions defined in the IEEE Standard 1149.1-1990; the standard (public) instructions and device specific (private) instructions. Some public instructions are mandatory for IEEE 1149.1 compliance. Optional public instructions must be implemented in prescribed ways.

Although the TAP controller in this device follows the IEEE 1149.1 conventions, it is not IEEE 1149.1 compliant because some of the mandatory instructions are not fully implemented.

The TAP on this device may be used to monitor all input and I/O pads, but can not be used to load address, data, or control signals into the device or to preload the I/O buffers. In other words, the device will not perform IEEE 1149.1 EXTEST, INTEST, or the preload portion of the SAMPLE/PRELOAD command.

When the TAP controller is placed in Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction sets for this device are listed in the following tables.

### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this device.

The TAP controller does not recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the device responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between two instructions. Unlike SAMPLE/PRELOAD instruction, EXTEST places the device outputs in a High-Z state.

### IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in the instruction upon power-up and at any time the TAP controller is placed in the test-logic reset state.

### SAMPLE-Z

If the High-Z instruction is loaded in the instruction register, all output pins are forced to a High-Z state and the boundary scan register is connected between TDI and TDO pins when the TAP controller is in a Shift-DR state.

### SAMPLE/PRELOAD

SAMPLE/PRELOAD is an IEEE 1149.1 mandatory instruction. The PRELOAD portion of the command is not implemented in this device, so the device TAP controller is not fully IEEE 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded in the instruction register and the TAP controller is in the Capture-DR state, a snap shot of the data in the device's input and I/O buffers is loaded into the boundary scan register. Because the device system clock(s) are independent from the TAP clock (TCK), it is possible for the TAP to attempt to capture the input and I/O ring contents while the buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results can not be expected. To guarantee that the boundary scan register will capture the correct value of a signal, the device input signals must be stabilized long enough to meet the TAP controller's capture setup plus hold time ( $t_{CS}$  plus  $t_{CH}$ ). The device clock input(s) need not be paused for any other TAP operation except capturing the input and I/O ring contents into the boundary scan register.

Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins. Because the PRELOAD portion of the command is not implemented in this device, moving the controller to the Update-DR state with the SAMPLE/PRELOAD instruction loaded in the instruction register has the same effect as the Pause-DR command.

**BYPASS**

When the BYPASS instruction is loaded in the instruction register and the TAP controller is in the Shift-DR state, the bypass register is placed between TDI and TDO. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

**Reserved**

Do not use these instructions. They are reserved for future use.

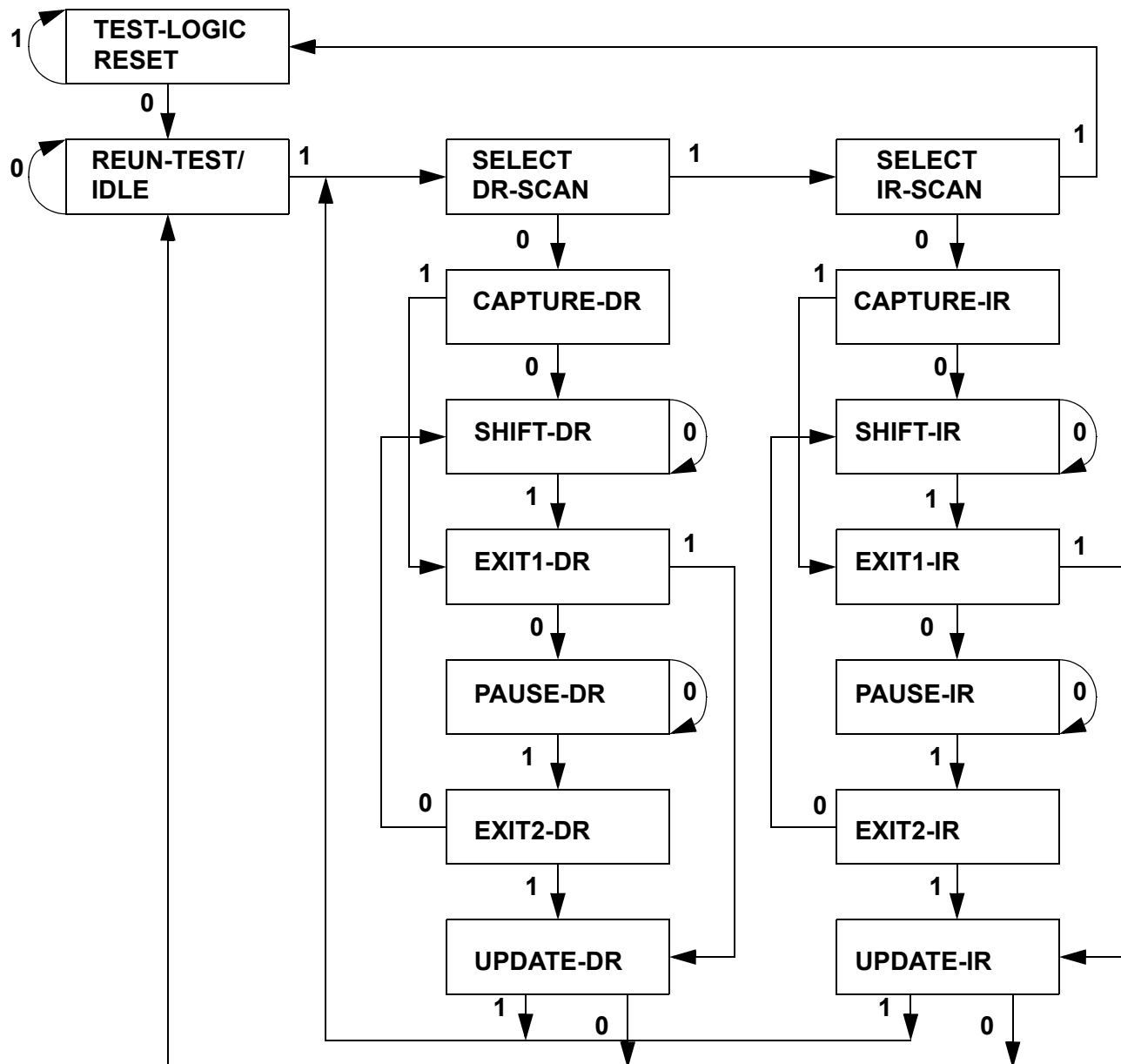
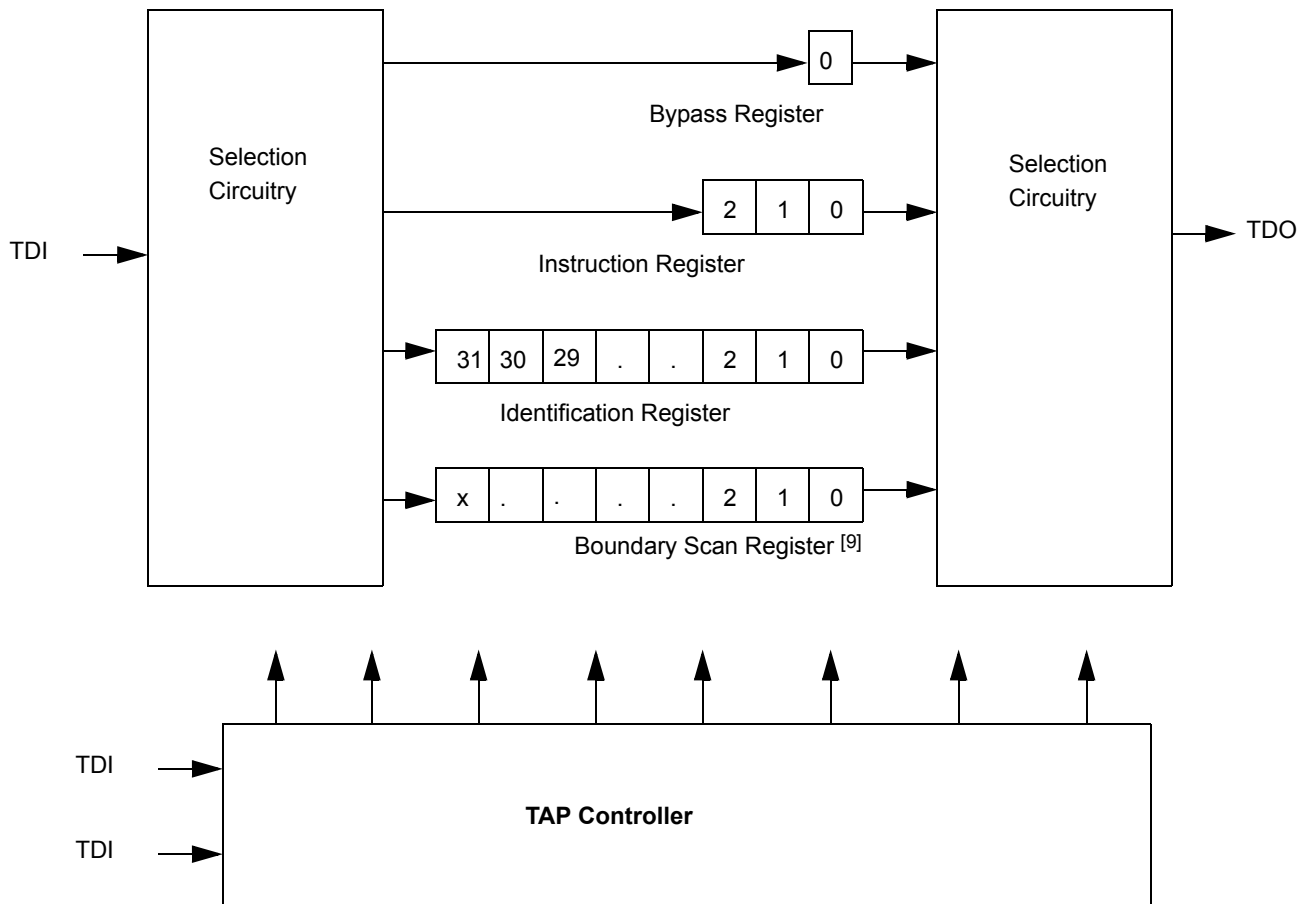


Figure 1. TAP Controller State Diagram<sup>[8]</sup>

**Note:**

8. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.




**Figure 2. TAP Controller Block Diagram**
**TAP DC Electrical Characteristics** ( $20^{\circ}\text{C} \leq T_j \leq 110^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{V} - 0.2\text{V}$  and  $+0.3\text{V}$  unless otherwise noted)

| Parameter | Description  | Test Conditions                                       | Min.            | Max.            | Unit          |
|-----------|--|---|-----------------|-----------------|---------------|
| $V_{IH}$  | Input High (Logic 1) Voltage: Inputs <sup>[10, 11]</sup>         | $V_{CCQ} = 3.3\text{V}$                               | 2.0             | 4.6             | V             |
|           |  | $V_{CCQ} = 2.5\text{V}$                               | 1.7             | 4.6             | V             |
|           | Input High (Logic 1) Voltage: Data <sup>[10, 11]</sup>           | $V_{CCQ} = 3.3\text{V}$                               | 2.0             | $V_{CCQ} + 0.3$ | V             |
|           |  | $V_{CCQ} = 2.5\text{V}$                               | 1.7             | $V_{CCQ} + 0.3$ |               |
| $V_{IL}$  | Input Low (Logic 0) Voltage: Inputs and Data <sup>[10, 11]</sup> | $V_{CCQ} = 3.3\text{V}$                               | -0.5            | 0.8             | V             |
|           |  | $V_{CCQ} = 2.5\text{V}$                               | -0.3            | 0.7             | V             |
| $IL_I$    | Input Leakage Current  | $0\text{V} \leq V_{IN} \leq V_{CC}$                   | -5.0            | 5.0             | $\mu\text{A}$ |
| $IL_I$    | TMS and TDI Input Leakage Current                                | $0\text{V} \leq V_{IN} \leq V_{CC}$                   | -30             | 30              | $\mu\text{A}$ |
| $IL_O$    | Output Leakage Current   | Output disabled, $0\text{V} \leq V_{IN} \leq V_{CCQ}$ | -5.0            | 5.0             | $\mu\text{A}$ |
| $V_{OLC}$ | LVC MOS Output Low Voltage <sup>[10, 12]</sup>                   | $I_{OLC} = 100\ \mu\text{A}$                          |                 | 0.2             | V             |
| $V_{OHC}$ | LVC MOS Output High Voltage <sup>[10, 12]</sup>                  | $I_{OHC} = 100\ \mu\text{A}$                          | $V_{CCQ} - 0.2$ |                 | V             |

**Notes:**

9. X = 69.

 10. All Voltage referenced to  $V_{SS}$  (GND).

 11. Overshoot:  $V_{IH}(AC) \leq V_{CC} + 1.5\text{V}$  for  $t \leq t_{KHKH}/2$ , Undershoot:  $V_{IL}(AC) \leq -0.5\text{V}$  for  $t \leq t_{KHKH}/2$ . Power-up:  $V_{IH} \leq 3.6\text{V}$  and  $V_{CC} \leq 3.135\text{V}$  and  $V_{CCQ} \leq 1.4\text{V}$  for  $t \leq 200\text{ms}$ . During normal operation,  $V_{CCQ}$  must not exceed 3.6V. Control input signals (such as R/W, ADV/LD, etc.) may not have pulse widths less than  $t_{KHKL}$  (min.).

12. This parameter is sampled.

**TAP DC Electrical Characteristics** ( $20^{\circ}\text{C} \leq T_j \leq 110^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{V} - 0.2\text{V}$  and  $+0.3\text{V}$  unless otherwise noted) (continued)

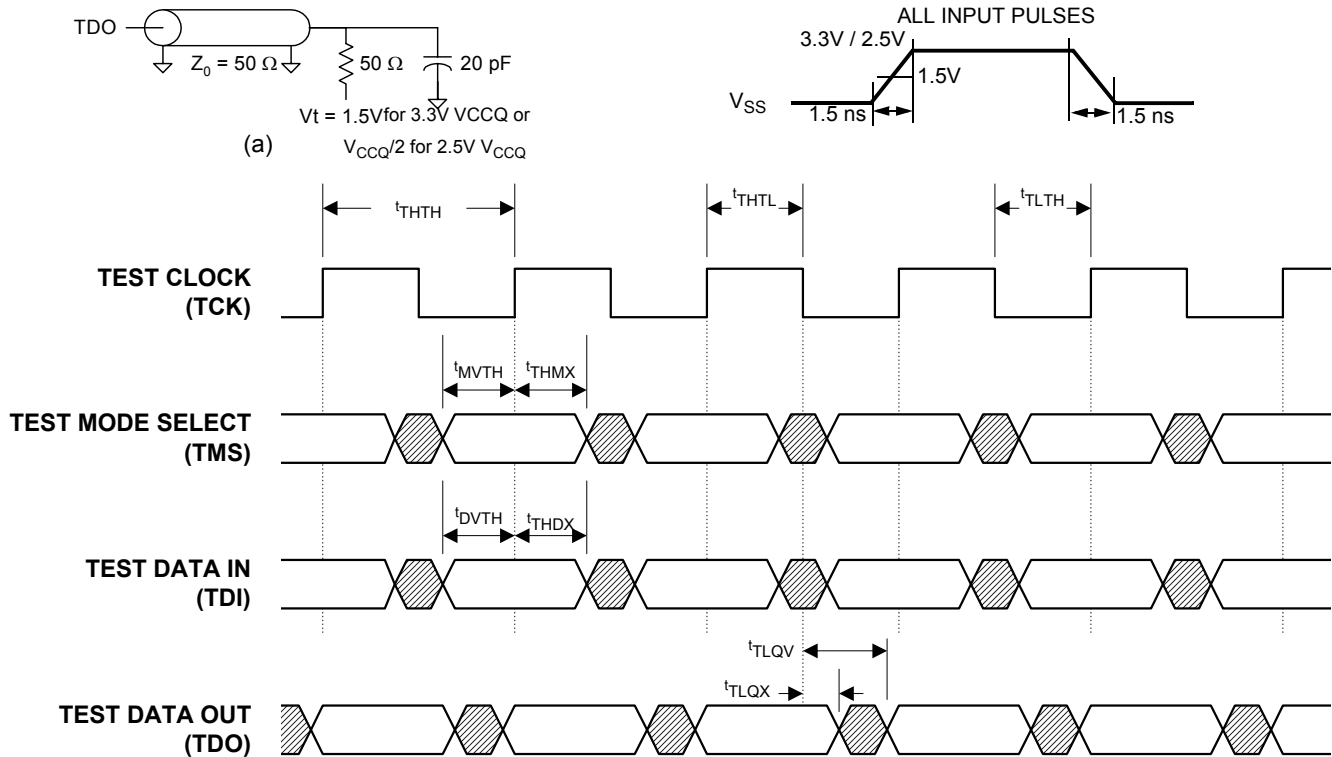
| Parameter        | Description                                | Test Conditions  | Min. | Max. | Unit |
|------------------|--|--|------|------|------|
| V <sub>OLT</sub> | LVTTTL Output Low Voltage <sup>[10]</sup>  | $V_{CC} = \text{Min. } V_{CCQ} = 3.3\text{V}, I_{OLT} = 8.0\text{ mA}$ |      | 0.4  | V    |
|                  |  | $V_{CC} = \text{Min. } V_{CCQ} = 2.5\text{V}, I_{OLT} = 2.0\text{ mA}$ |      | 0.7  | V    |
|                  |  | $V_{CC} = \text{Min. } V_{CCQ} = 2.5\text{V}, I_{OLT} = 1.0\text{ mA}$ |      | 0.4  | V    |
| V <sub>OHT</sub> | LVTTTL Output High Voltage <sup>[10]</sup> | $V_{CC} = \text{Min. } V_{CCQ} = 3.3\text{V}, I_{OH} = -4.0\text{ mA}$ | 2.4  |      | V    |
|                  |  | $V_{CC} = \text{Min. } V_{CCQ} = 2.5\text{V}, I_{OH} = -2.0\text{ mA}$ | 2.0  |      | V    |

**TAP AC Switching Characteristics** Over the Operating Range<sup>[13, 14]</sup>

| Parameter           | Description             | Min. | Max | Unit |
|---------------------|-------------------------|------|-----|------|
| <b>Clock</b>        |                         |      |     |      |
| t <sub>THTH</sub>   | Clock Cycle Time        | 20   |     | ns   |
| f <sub>TF</sub>     | Clock Frequency         |      | 50  | MHz  |
| t <sub>THTL</sub>   | Clock HIGH Time         | 8    |     | ns   |
| t <sub>TLTH</sub>   | Clock LOW Time          | 8    |     | ns   |
| <b>Output Times</b> |                         |      |     |      |
| t <sub>TLQX</sub>   | TCK LOW to TDO Unknown  | 0    |     | ns   |
| t <sub>TLQV</sub>   | TCK LOW to TDO Valid    |      | 10  | ns   |
| t <sub>DVTH</sub>   | TDI Valid to TCK HIGH   | 5    |     | ns   |
| t <sub>THDX</sub>   | TCK HIGH to TDI Invalid | 5    |     | ns   |
| <b>Set-up Times</b> |                         |      |     |      |
| t <sub>MVTH</sub>   | TMS Set-up              | 5    |     | ns   |
| t <sub>CS</sub>     | Capture Set-up          | 5    |     | ns   |
| <b>Hold Times</b>   |                         |      |     |      |
| t <sub>THMX</sub>   | TMS Hold                | 5    |     | ns   |
| t <sub>CH</sub>     | Capture Hold            | 5    |     | ns   |

**Notes:**

13. t<sub>CS</sub> and t<sub>CH</sub> refer to the set-up and hold time requirements of latching data from the boundary scan register.  
 14. Test conditions are specified using the load in TAP AC Test Conditions.

**TAP Timing and Test Conditions**

**Identification Register Definitions**

| Instruction Field                  | 128K x 36   | Description                                    |
|------------------------------------|-------------|--|
| Revision Number (31:28)            | XXXX        | Reserved for revision number.                  |
| Device Depth (27:23)               | 00111       | Defines depth of words.                        |
| Device Width (22:18)               | 00011       | Defines width of bits.                         |
| Reserved (17:12)                   | XXXXXX      | Reserved for future use.                       |
| Cypress Jedec Id Code (11:1)       | 00011100100 | Allows unique identification of DEVICE vendor. |
| ID Register Presence Indicator (0) | 1           | Indicates the presence of an ID register.      |

**Scan Register Sizes**

| Register Name | Bit Size (x36) |
|---------------|----------------|
| Instruction   | 3              |
| Bypass        | 1              |
| ID            | 32             |
| Boundary Scan | 51             |

**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Instruction Codes**

| Instruction    | Code | Description  |
|----------------|------|--|
| EXTEST         | 000  | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state. This instruction is not IEEE 1149.1-compliant.   |
| IDCODE         | 001  | Preloads ID register with vendor ID code and places it between TDI and TDO. This instruction does not affect device operations.  |
| SAMPLE-Z       | 010  | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all device outputs to High-Z state.  |
| RESERVED       | 011  | Do not use these instructions; they are reserved for future use.   |
| SAMPLE/PRELOAD | 100  | Captures I/O ring contents. Places the boundary scan register between TDI and TDO. This instruction does not affect device operations. This instruction does not implement IEEE 1149.1 PRELOAD function and is therefore not 1149.1-compliant. |
| RESERVED       | 101  | Do not use these instructions; they are reserved for future use.   |
| RESERVED       | 110  | Do not use these instructions; they are reserved for future use.   |
| BYPASS         | 111  | Places the bypass register between TDI and TDO. This instruction does not affect device operations.  |

**Boundary Scan Order**

| Bit# | Signal Name | TQFP | Bump ID |
|------|-------------|------|---------|
| 1    | A           | 44   | 2R      |
| 2    | A           | 45   | 3T      |
| 3    | A           | 46   | 4T      |
| 4    | A           | 47   | 5T      |
| 5    | A           | 48   | 6R      |
| 6    | A           | 49   | 3B      |
| 7    | A           | 50   | 5B      |
| 8    | DQa         | 51   | 6P      |
| 9    | DQa         | 52   | 7N      |
| 10   | DQa         | 53   | 6M      |
| 11   | DQa         | 56   | 7L      |
| 12   | DQa         | 57   | 6K      |
| 13   | DQa         | 58   | 7P      |
| 14   | DQa         | 59   | 6N      |
| 15   | DQa         | 62   | 6L      |
| 16   | DQa         | 63   | 7K      |
| 17   | ZZ          | 64   | 7T      |
| 18   | DQb         | 68   | 6H      |
| 19   | DQb         | 69   | 7G      |
| 20   | DQb         | 72   | 6F      |
| 21   | DQb         | 73   | 7E      |
| 22   | DQb         | 74   | 6D      |
| 23   | DQb         | 75   | 7H      |
| 24   | DQb         | 78   | 6G      |
| 25   | DQb         | 79   | 6E      |
| 26   | DQb         | 80   | 7D      |
| 27   | A           | 81   | 6A      |
| 28   | A           | 82   | 5A      |
| 29   | ADV         | 83   | 4G      |

**Boundary Scan Order (continued)**

| Bit# | Signal Name     | TQFP | Bump ID |
|------|-----------------|------|---------|
| 30   | ADSP            | 84   | 4A      |
| 31   | ADSC            | 85   | 4B      |
| 32   | OE              | 86   | 64F     |
| 33   | BWE             | 87   | 4M      |
| 34   | GW              | 88   | 4H      |
| 35   | CLK             | 89   | 4K      |
| 36   | CE <sub>2</sub> | 92   | 6B      |
| 37   | BWa             | 93   | 5L      |
| 38   | BWb             | 94   | 5G      |
| 39   | BWc             | 95   | 3G      |
| 40   | BWd             | 96   | 3L      |
| 41   | CE <sub>2</sub> | 97   | 2B      |
| 42   | CE              | 98   | 4E      |
| 43   | A               | 99   | 3A      |
| 44   | A               | 100  | 2A      |
| 45   | DQc             | 1    | 2D      |
| 46   | DQc             | 2    | 1E      |
| 47   | DQc             | 3    | 2F      |
| 48   | DQc             | 6    | 1G      |
| 49   | DQc             | 7    | 2H      |
| 50   | DQc             | 8    | 1D      |
| 51   | DQc             | 9    | 2E      |
| 52   | DQc             | 12   | 2G      |
| 53   | DQc             | 13   | 1H      |
| 54   | NC              | 14   | 5R      |
| 55   | DQd             | 18   | 2K      |
| 56   | DQd             | 19   | 1L      |
| 57   | DQd             | 22   | 2M      |
| 58   | DQd             | 23   | 1N      |

 NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Boundary Scan Order** (continued)

| Bit# | Signal Name | TQFP | Bump ID |
|------|-------------|------|---------|
| 59   | DQd         | 24   | 2P      |
| 60   | DQd         | 25   | 1K      |
| 61   | DQd         | 28   | 2L      |
| 62   | DQd         | 29   | 2N      |
| 63   | DQd         | 30   | 1P      |
| 64   | MODE        | 31   | 3R      |
| 65   | A           | 32   | 2C      |
| 66   | A           | 33   | 3C      |
| 67   | A           | 34   | 5C      |
| 68   | A           | 35   | 6C      |
| 69   | A1          | 36   | 4N      |
| 70   | A0          | 37   | 4P      |



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on  $V_{CC}$  Supply Relative to  $V_{SS}$  ..... -0.5V to +4.6V  
 $V_{IN}$  ..... -0.5V to  $V_{CC}+0.5V$   
 Storage Temperature (plastic) ..... -55°C to +150°  
 Junction Temperature ..... +150°

Power Dissipation..... 1.0W  
 Short Circuit Output Current..... 50 mA

**Operating Range**

| Range | Ambient Temperature <sup>[15]</sup> | $V_{CC}$      |
|-------|-------------------------------------|---------------|
| Com'l | 0°C to +70°C                        | 3.3V -5%/+10% |

**Electrical Characteristics** Over the Operating Range

| Parameter | Description  | Test Conditions  | Min.  | Max.            | Unit    |
|-----------|--|--|-------|-----------------|---------|
| $V_{IH}$  | Input High (Logic 1) Voltage: Inputs <sup>[10, 11]</sup>         | $V_{CCQ} = 3.3 V$  | 2.0   | 4.6             | V       |
|           |  | $V_{CCQ} = 2.5V$   | 1.7   | 4.6             | V       |
|           | Input High (Logic 1) Voltage: Data <sup>[10, 11]</sup>           | $V_{CCQ} = 3.3 V$  | 2.0   | $V_{CCQ} + 0.3$ | V       |
|           |  | $V_{CCQ} = 2.5V$   | 1.7   | $V_{CCQ} + 0.3$ |         |
| $V_{IL}$  | Input Low (Logic 0) Voltage: Inputs and Data <sup>[10, 11]</sup> | $V_{CCQ} = 3.3 V$  | -0.5  | 0.8             | V       |
|           |  | $V_{CCQ} = 2.5V$   | -0.3  | 0.7             | V       |
| $I_{LI}$  | Input Leakage Current  | $0V \leq V_{IN} \leq V_{CC}$                                     | -5    | 5               | $\mu A$ |
| $I_{LI}$  | MODE and ZZ Input Leakage Current <sup>[17]</sup>                | $0V \leq V_{IN} \leq V_{CC}$                                     | -30   | 30              | $\mu A$ |
| $I_{LO}$  | Output Leakage Current   | Output(s) disabled, $0V \leq V_{OUT} \leq V_{CC}$                | -5    | 5               | $\mu A$ |
| $V_{OH}$  | Output High Voltage <sup>[10]</sup>                              | $V_{CC} = \text{Min}, V_{CCQ} = 3.3 V, I_{OH} = -4.0 \text{ mA}$ | 2.4   |                 | V       |
|           |  | $V_{CC} = \text{Min}, V_{CCQ} = 2.5V, I_{OH} = -2.0 \text{ mA}$  | 2.0   |                 | V       |
| $V_{OL}$  | Output Low Voltage <sup>[10]</sup>                               | $V_{CC} = \text{Min}, V_{CCQ} = 3.3V, I_{OL} = 8.0 \text{ mA}$   |       | 0.4             | V       |
|           |  | $V_{CC} = \text{Min}, V_{CCQ} = 2.5V, I_{OH} = 2.0 \text{ mA}$   |       | 0.7             | V       |
|           |  | $V_{CC} = \text{Min}, V_{CCQ} = 2.5V, I_{OH} = 1.0 \text{ mA}$   |       | 0.4             | V       |
| $V_{CC}$  | Supply Voltage <sup>[10]</sup>                                   |  | 3.135 | 3.6             | V       |
| $V_{CCQ}$ | I/O Supply Voltage <sup>[10]</sup>                               | 3.3 V Range  | 3.135 | 3.6             | V       |
|           |  | 2.5 V Range  | 2.375 | 2.9             | V       |

| Parameter | Description   | Conditions   | Typ. | -4  | -4.4 | -5  | -6  | Unit |
|-----------|---|--|------|-----|------|-----|-----|------|
| $I_{CC}$  | Power Supply Current: Operating <sup>[18, 19, 20]</sup> | Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$ ; cycle time $\geq t_{KC}$ min.; $V_{CC} = \text{Max.}$ ; outputs open        | 150  | 450 | 400  | 360 | 300 | mA   |
| $I_{SB2}$ | CMOS Standby <sup>[19, 20]</sup>                        | Device deselected; $V_{CC} = \text{Max.}$ ; all inputs $\leq V_{SS} + 0.2$ or $\geq V_{CC} - 0.2$ ; all inputs static; CLK frequency = 0 | 5    | 10  | 10   | 10  | 10  | mA   |
| $I_{SB3}$ | TTL Standby <sup>[19, 20]</sup>                         | Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$ ; all inputs static; $V_{CC} = \text{Max.}$ ; CLK frequency = 0             | 10   | 20  | 20   | 20  | 20  | mA   |
| $I_{SB4}$ | Clock Running <sup>[19, 20]</sup>                       | Device deselected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$ ; $V_{CC} = \text{Max.}$ ; CLK cycle time $\geq t_{KC}$ min.                | 40   | 140 | 125  | 110 | 90  | mA   |

**Notes:**

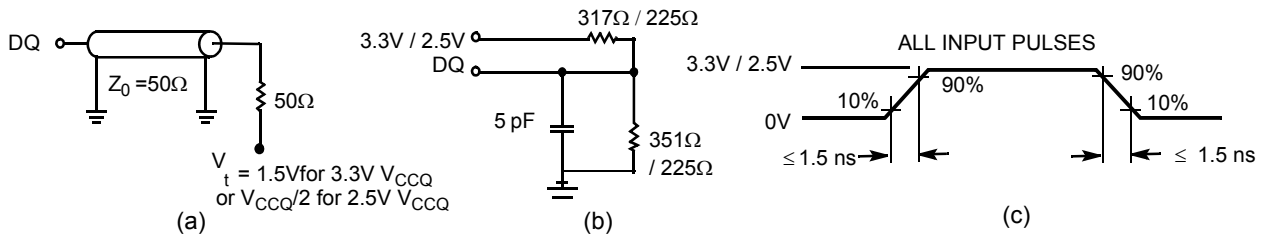
15.  $T_A$  is the case temperature.
16. Overshoot:  $V_{IH} \leq +6.0V$  for  $t \leq t_{KC}/2$ .  
Undershoot:  $V_{IL} \leq -2.0V$  for  $t \leq t_{KC}/2$ .
17. Output loading is specified with  $C_L = 5 \text{ pF}$  as in AC Test Loads.
18.  $I_{CC}$  is given with no output current.  $I_{CC}$  increases with greater output loading and faster cycle times.
19. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
20. Typical values are measured at 3.3V, 25°C, and 20-ns cycle time.

**Capacitance<sup>[12]</sup>**

| Parameter      | Description                   | Test Conditions   | Typ. | Max. | Unit |
|----------------|-------------------------------|---|------|------|------|
| C <sub>I</sub> | Input Capacitance             | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 3.3V | 5    | 7    | pF   |
| C <sub>O</sub> | Input/Output Capacitance (DQ) |   | 7    | 8    | pF   |

**Thermal Resistance**

| Parameter       | Description                              | Test Conditions   | TQFP Typ. | BGA Typ. | Unit |
|-----------------|--|---|-----------|----------|------|
| Θ <sub>JA</sub> | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB | 25        | 50       | °C/W |
| Θ <sub>JC</sub> | Thermal Resistance (Junction to Case)    |   | 9         | 8        | °C/W |

**AC Test Loads and Waveforms<sup>[21]</sup>**

**Switching Characteristics Over the Operating Range<sup>[22]</sup>**

| Parameter           | Description                                       | 250 MHz |      | 225 MHz |      | 200 MHz |      | 166 MHz |      | Unit |
|---------------------|---|---------|------|---------|------|---------|------|---------|------|------|
|                     |   | Min.    | Max. | Min.    | Max. | Min.    | Max. | Min.    | Max. |      |
| <b>Clock</b>        |   |         |      |         |      |         |      |         |      |      |
| t <sub>KC</sub>     | Clock Cycle Time                                  | 4.0     |      | 4.4     |      | 5.0     |      | 6.0     |      | ns   |
| t <sub>KH</sub>     | Clock HIGH Time                                   | 1.6     |      | 1.7     |      | 2.0     |      | 2.4     |      | ns   |
| t <sub>KL</sub>     | Clock LOW Time                                    | 1.6     |      | 1.7     |      | 2.0     |      | 2.4     |      | ns   |
| <b>Output Times</b> |   |         |      |         |      |         |      |         |      |      |
| t <sub>KQ</sub>     | Clock to Output Valid                             |         | 2.4  |         | 2.5  |         | 3.0  |         | 3.5  | ns   |
| t <sub>KQX</sub>    | Clock to Output Invalid                           | 1.25    |      | 1.25    |      | 1.25    |      | 1.25    |      | ns   |
| t <sub>KQLZ</sub>   | Clock to Output in Low-Z <sup>[12, 17, 23]</sup>  | 0       |      | 0       |      | 0       |      | 0       |      | ns   |
| t <sub>KQHZ</sub>   | Clock to Output in High-Z <sup>[12, 17, 23]</sup> | 1.25    | 3.0  | 1.25    | 3.0  | 1.25    | 3.0  | 1.25    | 4.0  | ns   |
| t <sub>OEQ</sub>    | OE to Output Valid <sup>[24]</sup>                |         | 2.5  |         | 2.5  |         | 2.5  |         | 3.5  | ns   |
| t <sub>OELZ</sub>   | OE to Output in Low-Z <sup>[12, 17, 23]</sup>     | 0       |      | 0       |      | 0       |      | 0       |      | ns   |
| t <sub>OEHZ</sub>   | OE to Output in High-Z <sup>[12, 17, 23]</sup>    |         | 2.5  |         | 2.5  |         | 2.5  |         | 3.5  | ns   |
| <b>Set-up Times</b> |   |         |      |         |      |         |      |         |      |      |
| t <sub>S</sub>      | Address, Controls, and Data In <sup>[25]</sup>    | 1.5     |      | 1.5     |      | 1.5     |      | 1.5     |      | ns   |
| <b>Hold Times</b>   |   |         |      |         |      |         |      |         |      |      |
| t <sub>H</sub>      | Address, Controls, and Data In <sup>[25]</sup>    | 0.5     |      | 0.5     |      | 0.5     |      | 0.5     |      | ns   |

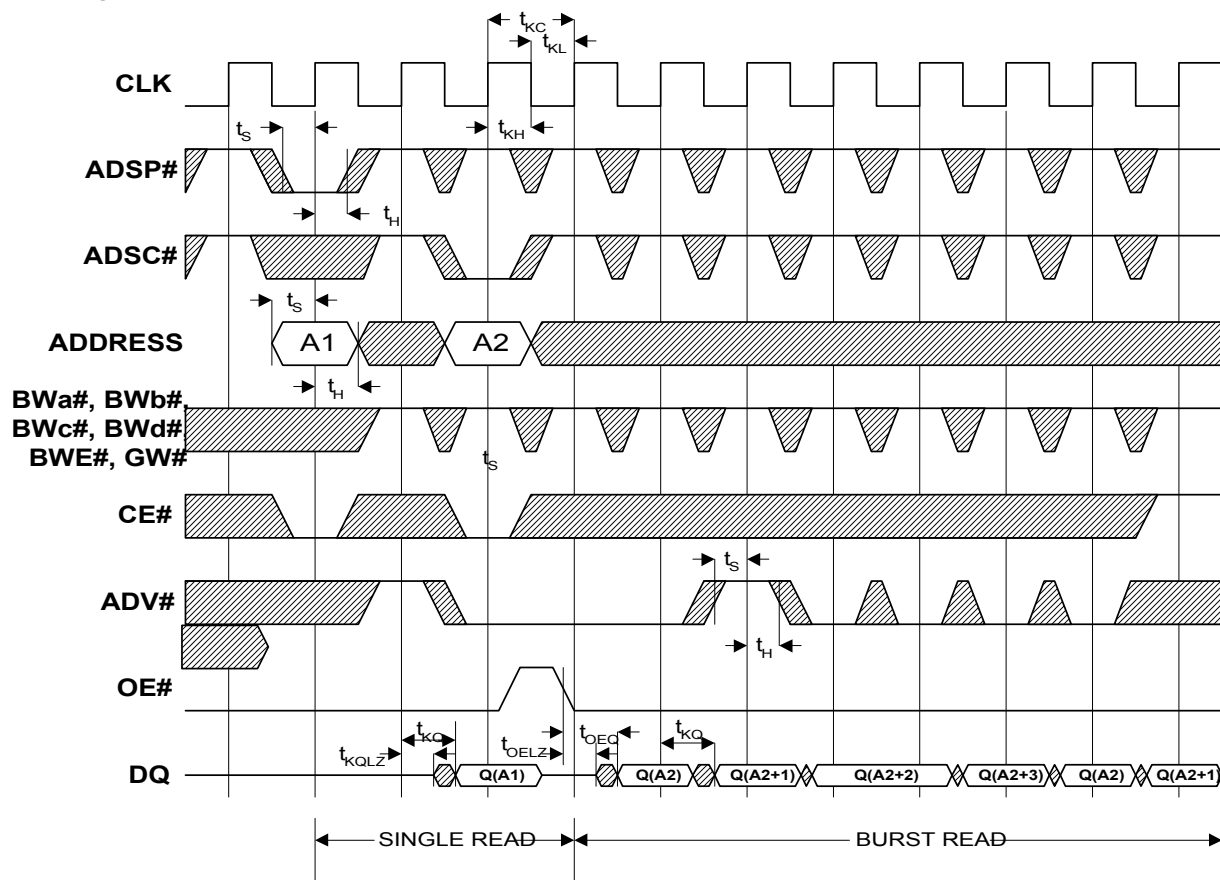
**Notes:**

21. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5V for t < t<sub>TCYC</sub>/2; undershoot: V<sub>IL</sub>(AC) < 0.5V for t < t<sub>TCYC</sub>/2; power-up: V<sub>IH</sub> < 2.6V and V<sub>DD</sub> < 2.4V and V<sub>DDQ</sub> < 1.4V for t < 200 ms.
22. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted.
23. At any given temperature and voltage condition, t<sub>KQHZ</sub> is less than t<sub>KQLZ</sub> and t<sub>OEHZ</sub> is less than t<sub>OELZ</sub>.
24. OE is a "Don't Care" when a byte write enable is sampled LOW.
25. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for "don't care" as defined in the truth table.

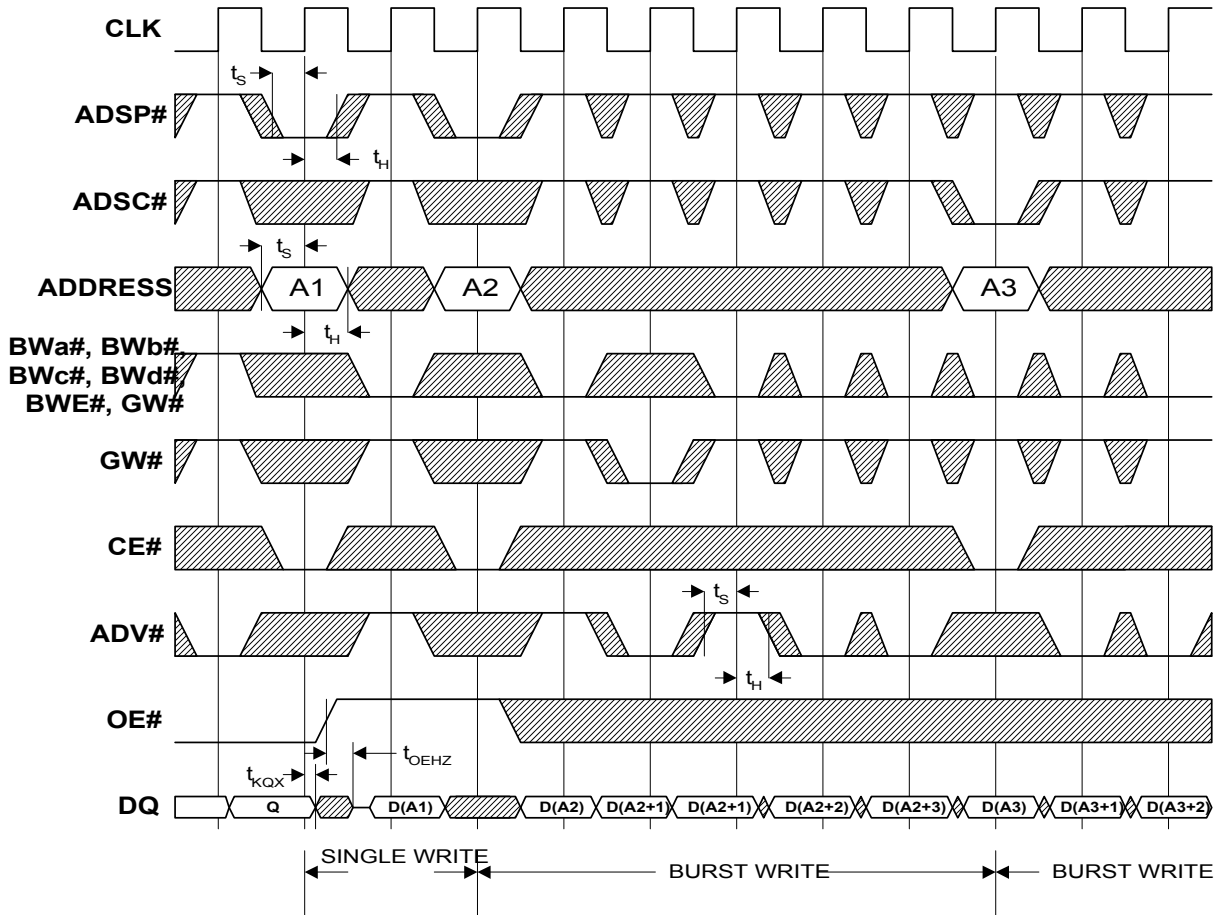
**Typical Output Buffer Characteristics**

| Output High Voltage |                    | Pull-Up Current    |              | Output Low Voltage |                    | Pull-Down Current |                    |
|---------------------|--------------------|--------------------|--------------|--------------------|--------------------|-------------------|--------------------|
| $V_{OH}$ (V)        | $I_{OH}$ (mA) Min. | $I_{OH}$ (mA) Max. | $V_{OL}$ (V) | $I_{OL}$ (mA) Min. | $I_{OL}$ (mA) Max. | $V_{OL}$ (V)      | $I_{OL}$ (mA) Max. |
| -0.5                | -38                | -105               | -0.5         | 0                  | 0                  | -0.5              | 0                  |
| 0                   | -38                | -105               | 0            | 0                  | 0                  | 0                 | 0                  |
| 0.8                 | -38                | -105               | 0.4          | 10                 | 20                 | 0.8               | 20                 |
| 1.25                | -26                | -83                | 0.8          | 20                 | 40                 | 1.25              | 31                 |
| 1.5                 | -20                | -70                | 1.6          | 40                 | 80                 | 1.6               | 40                 |
| 2.3                 | 0                  | -30                | 2.8          | 40                 | 80                 | 2.8               | 40                 |
| 2.7                 | 0                  | -10                | 3.2          | 40                 | 80                 | 3.2               | 40                 |
| 2.9                 | 0                  | 0                  | 3.4          | 40                 | 80                 | 3.4               | 40                 |
| 3.4                 | 0                  | 0                  |              |                    |                    |                   |                    |

**Switching Waveforms**

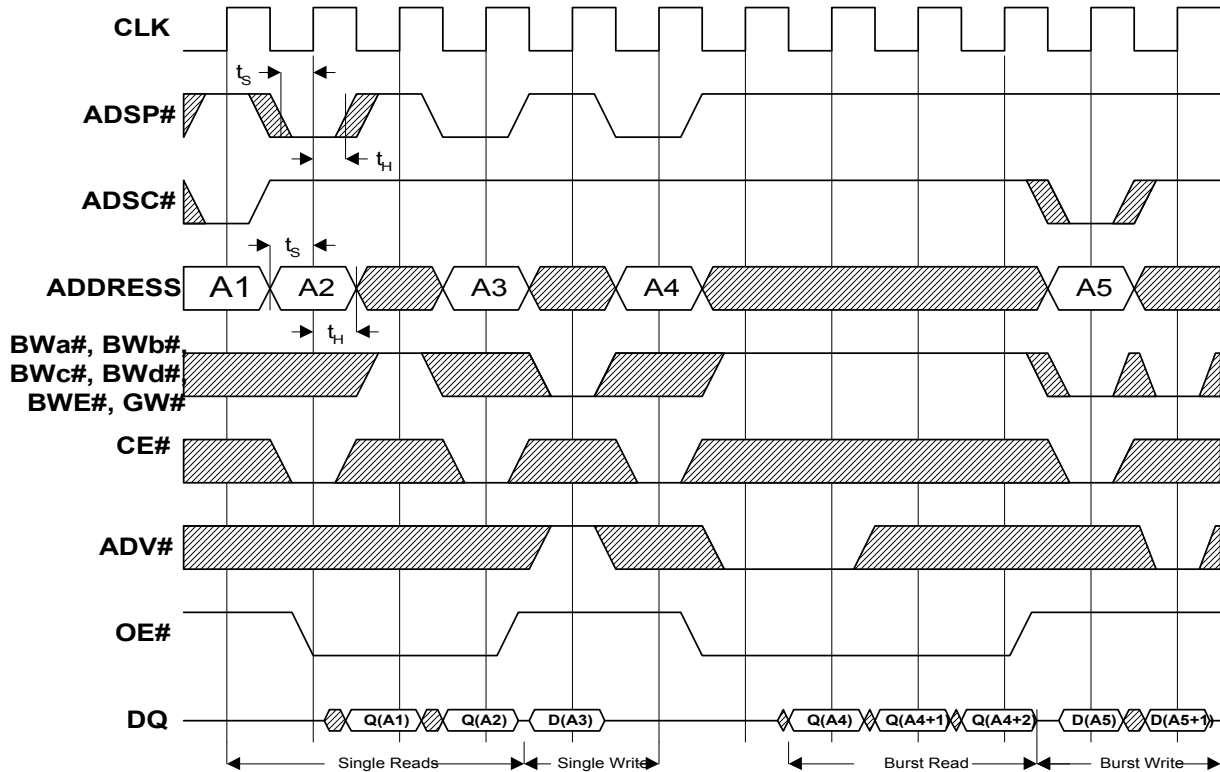
 Read Timing<sup>[26, 27]</sup>

**Notes:**

- 26.  $\overline{CE}$  active in this timing diagram means that all chip enables  $\overline{CE}$ , CE2, and  $\overline{CE2}$  are active.
- 27. For X18 product, there are only BwA and BwB for byte write control.

**Switching Waveforms (continued)**
**Write Timing<sup>[26, 27]</sup>**


**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Switching Waveforms (continued)**

 Read/Write Timing<sup>[26, 27]</sup>

**Ordering Information**

| Speed (MHz) | Ordering Code    | Package Name | Package Type                                  | Operating Range |
|-------------|------------------|--------------|---|-----------------|
| 250         | CY7C1347D-250AC  | A101         | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack | Commercial      |
|             | CY7C1347D-250BGC | BG119        | 119-Lead FBGA (14 x 22 x 2.4 mm)              |                 |
| 225         | CY7C1347D-225BGC | BG119        | 119-Lead FBGA (14 x 22 x 2.4 mm)              |                 |
| 200         | CY7C1347D-200AC  | A101         | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack |                 |
| 166         | CY7C1347D-166AC  | A101         | 100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack |                 |
|             |                  |              |   |                 |

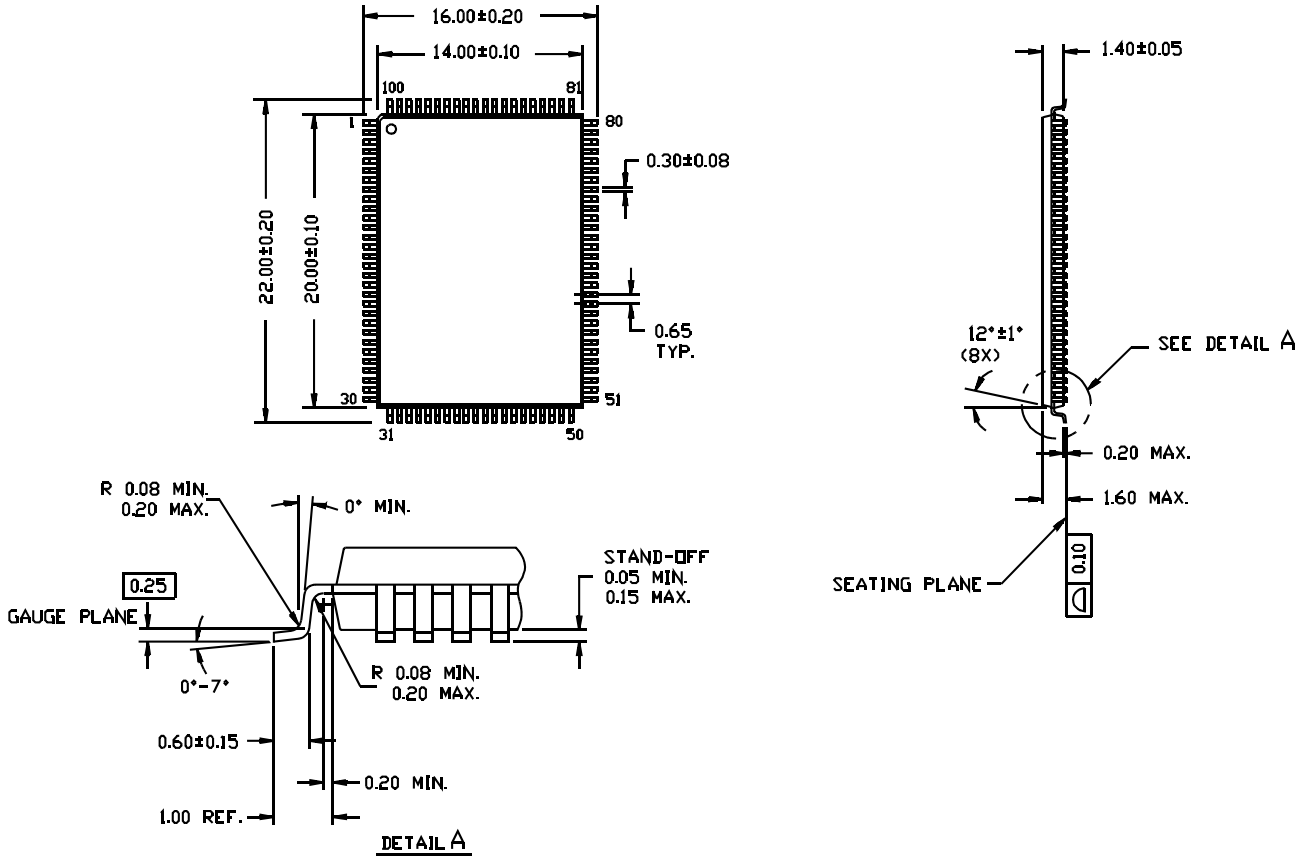
 NOT RECOMMENDED FOR NEW DESIGNS  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE



Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101

DIMENSIONS ARE IN MILLIMETERS.

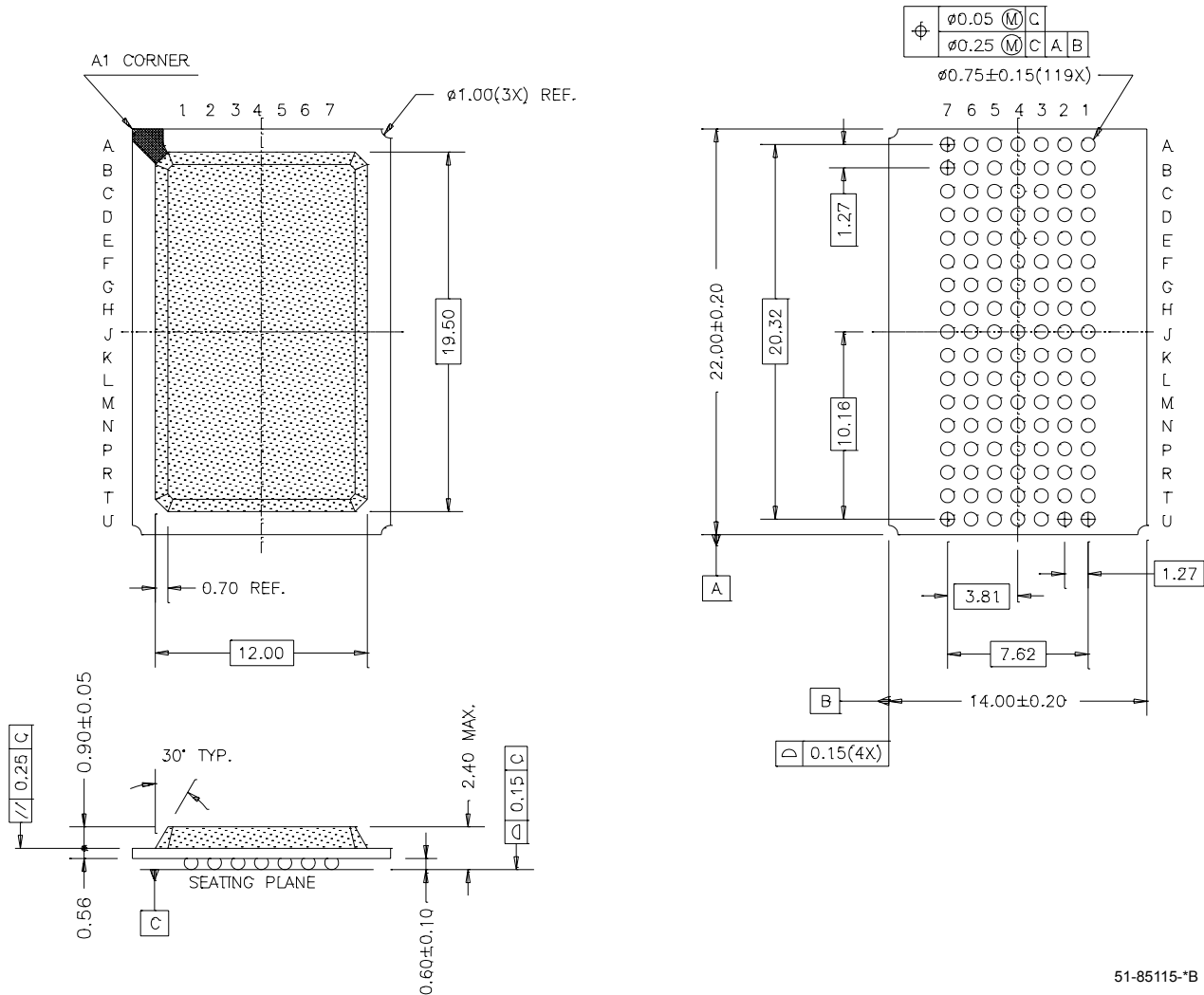


51-85050-\*A

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

Package Diagrams (continued)

119-Lead FBGA (14 x 22 x 2.4 mm) BG119



51-85115-\*B

All product and company names mentioned in this document may be the trademarks of their respective holders.

NOT RECOMMENDED FOR NEW DESIGNS  
ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE

**Document History Page**

| Document Title: CY7C1347D: 128K x 36 Synchronous-Pipelined Cache SRAM<br>Document Number: 38-05022 |         |            |                 |  |
|--|---------|------------|-----------------|--|
| Rev.   | ECN No. | Issue Date | Orig. of Change | Description of Change  |
| **   | 106740  | 05/07/01   | RCS             | New data sheet   |
| *A   | 107485  | 06/06/01   | RCS             | Added Minimum and Maximum values for 2.5V V <sub>CCQ</sub> and all other subsequent parameters<br>Defined alternate options for non-utilized JTAG pins |
| *B   | 121064  | 11/13/02   | DSG             | Updated package drawing 51-85115 (BG119) to rev. *B  |
| *C   | 122474  | 01/18/03   | RBI             | Added power up requirements to AC test loads and waveforms information   |
| *D   | 212291  | See ECN    | VBL             | Corrected Ordering Info section : delete 166BGA, 200BGA, 225AC   |
| *E   | 289731  | See ECN    | NJY             | Corrected the typo on page 4 for TMS pin connection  |

**NOT RECOMMENDED FOR NEW DESIGNS**  
 ONE OR MORE ORDERABLE PARTS ASSOCIATED WITH THIS DOCUMENT IS OBSOLETE. FOR  
 REPLACEMENT PART INQUIRIES, PLEASE CONTACT YOUR LOCAL SALES REPRESENTATIVE