



MM54HC280/MM74HC280 9-Bit Odd/Even Parity Generator/Checker

General Description

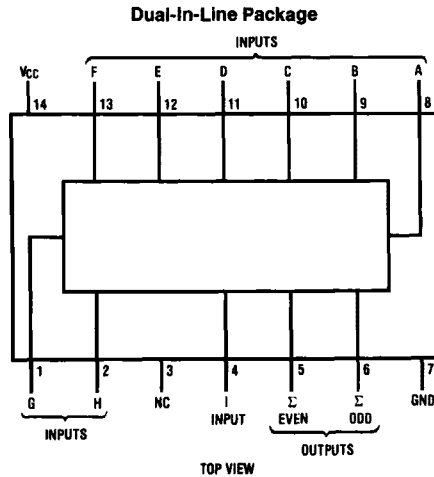
The MM54HC280/MM74HC280 utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits. It possesses the ability to drive 10 LS-TTL loads.

This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μ A maximum (74HC)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5121-1

Order Number MM54HC280* or MM74HC280*

*Please look into Section 8, Appendix D for availability of various package types.

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Function Table

| Numbers of Inputs A thru 1 that are High | Outputs | |
|---|---------------|--------------|
| | Σ Even | Σ Odd |
| 0, 2, 4, 6, 8 | H | L |
| 1, 3, 5, 7, 9 | L | H |

H = high level, L = low level

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------------|
| Supply Voltage (V_{CC}) | -0.5 to +7.0V |
| DC Input Voltage (V_{IN}) | -1.5 to $V_{CC} + 1.5V$ |
| DC Output Voltage (V_{OUT}) | -0.5 to $V_{CC} + 0.5V$ |
| Clamp Diode Current (I_{IK}, I_{OK}) | ± 20 mA |
| DC Output Current, per pin (I_{OUT}) | ± 25 mA |
| DC V_{CC} or GND Current, per pin (I_{CC}) | ± 50 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temp. (T_L) (Soldering 10 seconds) | 260°C |

Operating Conditions

| | Min | Max | Units |
|--|-----|----------|-------|
| Supply Voltage (V_{CC}) | 2 | 6 | V |
| DC Input or Output Voltage (V_{IN}, V_{OUT}) | 0 | V_{CC} | V |
| Operating Temp. Range (T_A) | | | |
| MM74HC | -40 | +85 | °C |
| MM54HC | -55 | +125 | °C |
| Input Rise or Fall Times (t_r, t_f) | | | |
| $V_{CC} = 2.0V$ | | 1000 | ns |
| $V_{CC} = 4.5V$ | | 500 | ns |
| $V_{CC} = 6.0V$ | | 400 | ns |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | | 74HC | 54HC | Units |
|----------|-----------------------------------|---|----------|--------------------|-------------------|-----------------------------|------------------------------|---------|
| | | | | | | $T_A = -40$ to $85^\circ C$ | $T_A = -55$ to $125^\circ C$ | |
| | | | | Typ | Guaranteed Limits | | | |
| V_{IH} | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | 4.2 | V |
| V_{IL} | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | 1.8 | V |
| V_{OH} | Minimum High Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | 5.9 | V |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| | | | | | | | | |
| V_{OL} | Maximum Low Level Output Voltage | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | | | | | | | |
| I_{IN} | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0V | | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I_{CC} | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ | 6.0V | | 8.0 | 80 | 160 | μA |

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, C_L=15\text{ pF}, t_r=t_f=6\text{ ns}$

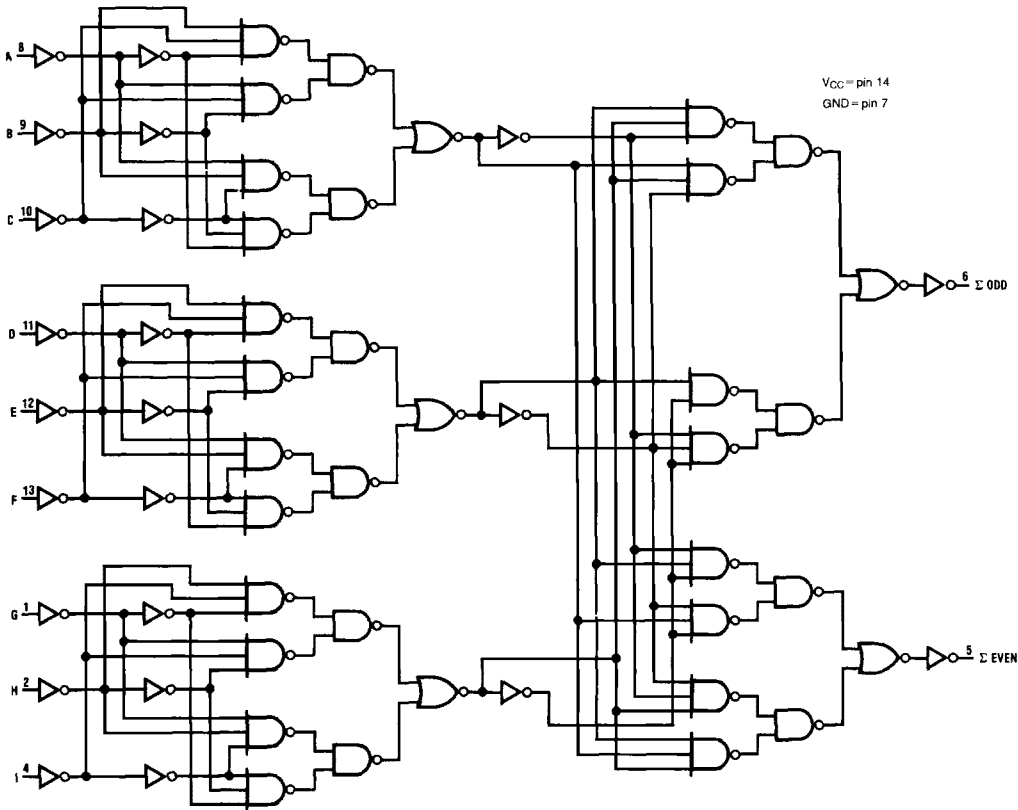
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|--------------------|--|------------|-----|------------------|-------|
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Σ Even | | 28 | 35 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Σ Odd | | 28 | 35 | ns |

AC Electrical Characteristics $V_{CC}=2.0V\text{ to }6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

| Symbol | Parameter | Conditions | V_{CC} | $T_A=25^{\circ}C$ | | | Units |
|--------------------|--|------------|----------|-------------------|---|--|-------|
| | | | | Typ | 74HC $T_A=-40\text{ to }85^{\circ}C$ | 54HC $T_A=-55\text{ to }125^{\circ}C$ | |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Σ Even | | 2.0V | 103 | 205 | 258 | ns |
| | | | 4.5V | 21 | 41 | 52 | ns |
| | | | 6.0V | 17 | 35 | 44 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Σ Odd | | 2.0V | 103 | 205 | 258 | ns |
| | | | 4.5V | 21 | 41 | 52 | ns |
| | | | 6.0V | 17 | 35 | 44 | ns |
| t_{TLH}, t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | ns |
| | | | 4.5V | 8 | 15 | 19 | ns |
| | | | 6.0V | 7 | 13 | 16 | ns |
| C_{PD} | Power Dissipation Capacitance (Note 5) | | | 83 | | | pF |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



'HC280

TL/F/5121-2