



# Quad D-Type Positive Edge-Triggered Flip-Flop

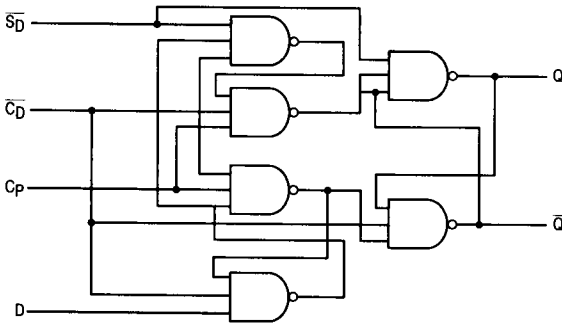
ELECTRICALLY TESTED PER:  
MIL-M-38510/34101

The 54F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the clock Pulse input.

### Asynchronous Inputs:

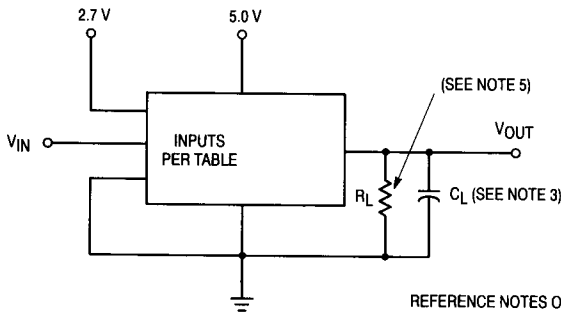
- LOW Input to  $\bar{S}_D$  sets Q to HIGH level
- LOW Input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-30

## Military 54F74



### AVAILABLE AS:

- 1) JAN: JM38510/34101BXA
- 2) SMD: N/A
- 3) 883: 54F74/BXAJC

X = CASE OUTLINE AS FOLLOWS:  
PACKAGE: CERDIP: C  
CERFLAT: D  
LCC: 2

THE LETTER "M" APPEARS  
BEFORE THE / ON LCC.

### PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
$\bar{C}_D1$	1	1	2	GND
D1	2	2	3	VCC
CP1	3	3	4	VCC
$\bar{S}_D1$	4	4	6	VCC
Q1	5	5	8	OPEN
$\bar{Q}1$	6	6	9	OPEN
GND	7	7	10	GND
$\bar{Q}2$	8	8	12	OPEN
Q2	9	9	13	OPEN
$\bar{S}_D2$	10	10	14	VCC
CP2	11	11	16	VCC
D2	12	12	18	VCC
$\bar{C}_D2$	13	13	19	GND
VCC	14	14	20	VCC

BURN-IN CONDITIONS:  
VCC = 5.0 V MIN/6.0 V MAX

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs			Outputs	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	L	H
Reset (clear)	H	L	X	H	L
*Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

\*Both outputs will be HIGH when both,  $\overline{S}_D$  and  $\overline{C}_D$  are LOW, but the output states are unpredictable if  $\overline{S}_D$  and  $\overline{C}_D$  go HIGH simultaneously. If the levels at the set and clear are near  $V_{IL}$  maximum then we cannot guarantee to meet the minimum level for  $V_{OH}$ .

H, h = HIGH Voltage Level

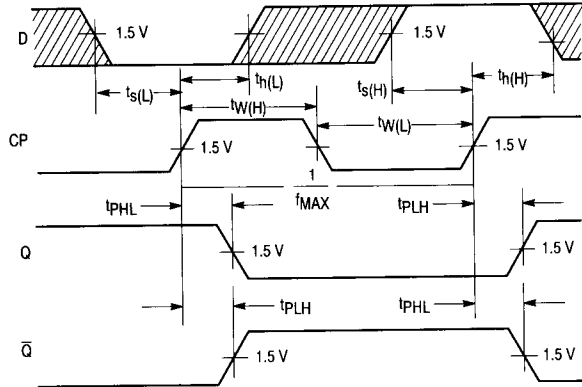
L, l = LOW Voltage Level

X = Don't Care

i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

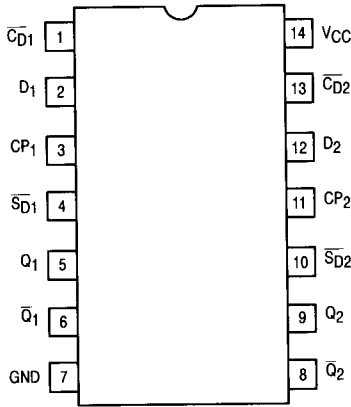
AC WAVEFORMS

Figure 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

CONNECTION DIAGRAM



LOGIC SYMBOLS

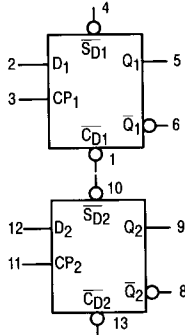
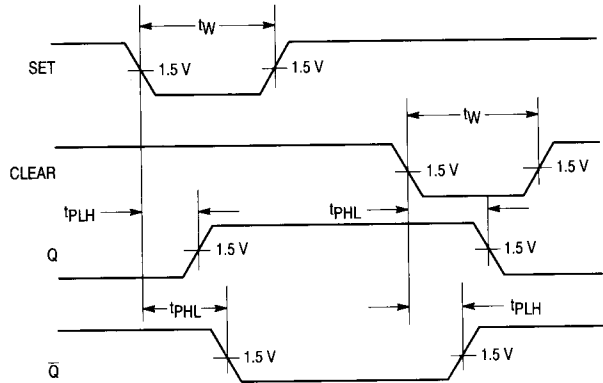


Figure 2. Set and Clear to Output Delays, Set and Clear Pulse Widths



## 54F74

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)		
		+25°C		+125°C		-55°C					
		Subgroup 1		Subgroup 2		Subgroup 3					
		Min	Max	Min	Max	Min	Max				
V <sub>OH</sub>	Logical "1" Output Voltage	2.5		2.5		2.5		V	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -1.0 mA, V <sub>IN</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V.		
V <sub>OL</sub>	Logical "0" Output Voltage		0.5		0.5		0.5	V	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA, V <sub>IH</sub> = 2.0 V, V <sub>IL</sub> = 0.8 V.		
V <sub>IC</sub>	Input Clamping Voltage		-1.2					V	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, other inputs are open.		
I <sub>IH</sub>	Logical "1" Input Current		20		20		20	μA	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 4.5 V, V <sub>IH</sub> = 2.7 V, D & CP = 0 V, CD 2.7 V.		
I <sub>IHH</sub>	Logical "1" Input Current		100		100		100	μA	V <sub>CC</sub> = 5.5 V, V <sub>IHH</sub> = 7.0 V, V <sub>IH</sub> = 4.5 V, D & CP = 0 V, CD 4.5 V.		
I <sub>IL</sub>	Logical "0" Input Current	CP,D	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.5V, SD = 0 V, CP = 4.5 V	CD = 4.5 V.
		CD,SD	-0.09	-1.8	-0.09	-1.8	-0.09	-1.8			D = 4.5 V.
I <sub>OD</sub>	Diode Current	60		60		60		mA	V <sub>CC</sub> = 4.5 V, CD = 0 V, SD = 5.5 V, other inputs are open, V <sub>OUT</sub> = 2.5 V.		
I <sub>OS</sub>	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V <sub>CC</sub> = 5.5 V, SD = 0 V, other inputs are open, V <sub>OUT</sub> = 0 V.		
I <sub>CC</sub>	Power Supply Current		16		16		16	mA	V <sub>CC</sub> = 5.5 V, CD = 5.5 V, other inputs = 0 V.		
V <sub>IH</sub>	Logical "1" Input Voltage	2.0		2.0		2.0		V	V <sub>CC</sub> = 4.5 V.		
V <sub>IL</sub>	Logical "0" Input Voltage		0.8		0.8		0.8	V	V <sub>CC</sub> = 4.5 V.		
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V <sub>CC</sub> = 4.5 V, (Repeat at), V <sub>CC</sub> = 5.5 V, V <sub>INL</sub> = 0.5 V, and V <sub>INH</sub> = 2.5 V.		

## 54F74

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t <sub>PHL1</sub>	Propagation Delay /Data-Output CP to Q or $\bar{Q}$	4.4	8.0	3.8	10.5	3.8	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PLH1</sub>	Propagation Delay /Data-Output CP to Q or $\bar{Q}$	3.8	6.8	3.8	8.5	3.8	8.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PHL2</sub>	Propagation Delay /Data-Output CP to Q or $\bar{Q}$	4.4	8.0	3.8	10.5	3.8	10.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PLH2</sub>	Propagation Delay /Data-Output CP to Q or $\bar{Q}$	3.8	6.8	3.8	8.5	3.8	8.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PHL3</sub>	Propagation Delay /Data-Output CD to Q or $\bar{Q}$	3.5	9.0	3.2	11.5	3.2	11.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PLH3</sub>	Propagation Delay /Data-Output CD to Q or $\bar{Q}$	3.2	6.1	3.2	8.0	3.2	8.0	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PHL4</sub>	Propagation Delay /Data-output SD to Q or $\bar{Q}$	3.5	9.0	3.5	11.5	3.5	11.5	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>PLH4</sub>	Propagation Delay /Data-Output SD to Q or $\bar{Q}$	3.2	6.1	3.2	8.0	3.2	8.0	ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
f <sub>MAX</sub>	Maximum Clock Frequency	100		80		80		MHz	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 499 Ω ± 5.0%.
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set Up Time D High or Low to CP	3.0		3.0		3.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, (Information only, No Testing Required).
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time D High or Low to CP	2.0		2.0		2.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, (Information only, No Testing Required).
t <sub>rec</sub>	Recovery Time SD or CD to CP	3.0		3.0		3.0		ns	V <sub>CC</sub> = 5.0 V, C <sub>L</sub> = 50 pF, (Information only, No Testing Required).

## NOTES:

1. Input pulse has the following characteristics:

t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns, PRR ≤ 1.0 MHz, or as specified in table, PRR (Subgroups 10 and 11) have a duty cycle 50 ± 15%, t<sub>p</sub> = 5.0 ns (min).

2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).

3. C<sub>L</sub> = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.

4. Voltage measurements are to be made with respect to network ground terminal.

5. R<sub>L</sub> = 499 Ω ± 5.0%.

6. When testing f<sub>MAX</sub> the output frequency shall be 1/2 the input frequency, f<sub>MAX</sub> minimum limit specified is the frequency of the input pulse.

7. Clock, Clear and Set inputs need to be in the proper configuration for specified output conditions.