

4721B/4721BX

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1024-BIT (256 x 4) RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

FAIRCHILD CMOS LSI

DESCRIPTION — The 4721B/4721BX is a 1024-Bit Random Access Memory, organized 256 words x 4 bits, with 3-state outputs. It has four Data Inputs (D₀-D₃), eight Address Inputs (A₀-A₇), an active LOW Write Enable Input (WE), two Chip Select Inputs, one active LOW (CS₀) and one active HIGH (CS₁), four 3-State Data Outputs (Q₀-Q₃) and an active LOW Output Enable Input (EO).

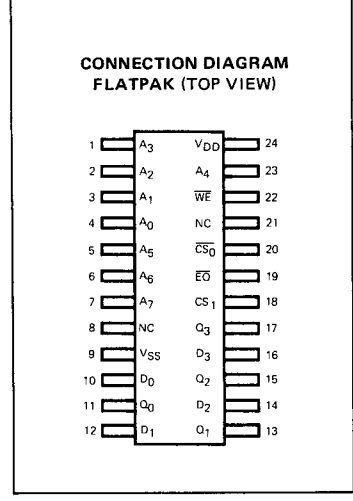
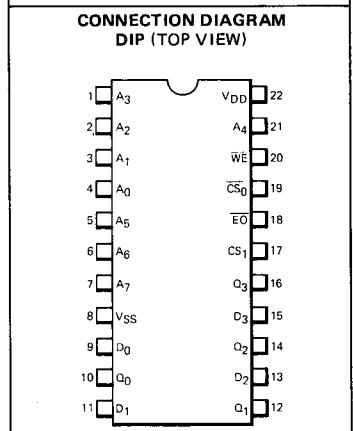
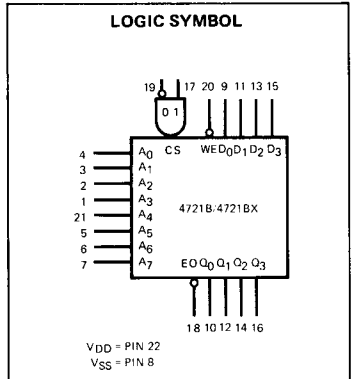
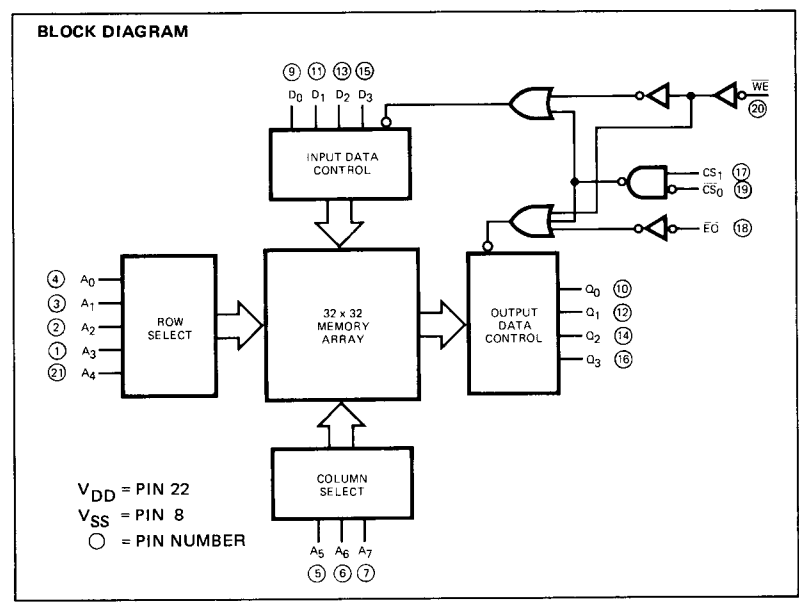
Information on the Data Inputs (D₀-D₃) is written into the memory location selected by the Address Inputs (A₀-A₇) when CS₀ and WE are LOW and CS₁ is HIGH. Under these conditions the Outputs (Q₀-Q₃) are held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A₀-A₇) while CS₀ is LOW and CS₁ and WE are HIGH. When CS₀ is HIGH or CS₁ is LOW all Outputs (Q₀-Q₃) are held in the high impedance OFF state. This allows other 3-state outputs to be wired together in a bus arrangement.

A HIGH on the active LOW Output Enable Input (EO) forces all Data Outputs (Q₀-Q₃) to a high impedance OFF status regardless of all other input conditions. The 4721B/4721BX offers fully static operation. The 4721B is specified to operate over a power supply voltage range of 5 ± 0.5 V. The 4721BX is specified to operate over a power supply voltage range of 4.5 V to 12.5 V.

- TYPICAL HOLDING VOLTAGE OF 1.5 V
- 3-STATE OUTPUTS
- ORGANIZATION — 256 WORDS X 4 BITS
- ON-CHIP DECODING
- FULLY STATIC OPERATION
- LOW POWER DISSIPATION
- HIGH SPEED
- TWO CHIP SELECT INPUTS FOR EASY MEMORY EXPANSION
- ACTIVE LOW OUTPUT ENABLE INPUT

PIN NAMES

- A₀ - A₇ Address Inputs
- D₀ - D₃ Data Inputs
- CS₀, CS₁ Chip Select (Active LOW and Active HIGH) Inputs
- WE Write Enable (Active LOW) Input
- Q₀ - Q₃ Data Outputs
- EO Output Enable (Active LOW) Input



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MODE SELECTION

INPUTS				OUTPUTS	MODE
\overline{EO}	$\overline{CS_0}$	CS_1	\overline{WE}	Q_n	
H	X	X	X	High Impedance	Output Disabled
H	L	H	L	High Impedance	Write — Output Disabled
H	L	H	H	High Impedance	Output Disabled
L	H	X	X	High Impedance	Inhibit
L	X	L	X	High Impedance	Inhibit
L	L	H	L	Data Written Into Memory	Write — Transparent
L	L	H	H	Data Written Into Memory	READ

L = LOW Level
H = HIGH Level
X = Don't Care

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 12.5$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
I_{OZH}	Output OFF Current HIGH	XC									1.6 12	μA	MIN, 25°C MAX	Output Returned to V_{DD} , $\overline{EO} = V_{DD}$
		XM									0.4 12			
I_{OZL}	Output OFF Current LOW	XC									-1.6 -12	μA	MIN, 25°C MAX	Output Returned to V_{SS} , $\overline{EO} = V_{DD}$
		XM									-0.4 -12			
I_{DD}	Quiescent Power Supply Current	XC		32.5 250			65 500				130 1000	μA	MIN, 25°C MAX	$\overline{CS_0} = V_{DD}$, $CS_1 = V_{SS}$
		XM		8.75 250			17.5 500				35 1000			

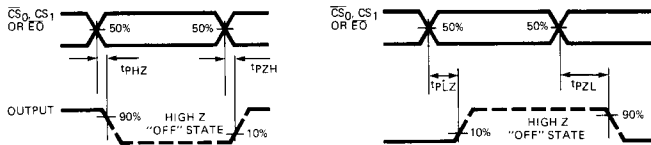
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ C$ (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 12.5$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	READ MODE Propagation Delay, Address to Output			420			240			180	ns	$C_L = 50$ pF, $R_L = 200$ k Ω Input Transition Times ≤ 20 ns ($R_L = 1$ k Ω to V_{SS}) ($R_L = 1$ k Ω to V_{DD}) ($R_L = 1$ k Ω to V_{SS}) ($R_L = 1$ k Ω to V_{DD})
				420			240			180		
t_{pZH}	Enable Time, $\overline{CS_0}$, CS_1 or \overline{EO} to Output			150			70			50	ns	
t_{pZL}	Disable Time, $\overline{CS_0}$, CS_1 or \overline{EO} to Output			150			70			50	ns	
t_{PHZ}	Output Transition Time			75			35			25	ns	
t_{TLH}	Output Transition Time			75			35			25	ns	
$t_{w\overline{WE}}$	WRITE MODE Minimum \overline{WE} Pulse Width			180			100			80	ns	
				150			120			115		
t_s	Set-Up Time, D_n to \overline{WE}			40			20			15	ns	
t_h	Hold Time, Address to \overline{WE}			150			120			115	ns	
t_s	Set-Up Time, Address to \overline{WE}			40			20			15	ns	
t_s	Set-Up Time, $\overline{CS_0}$ or CS_1 to \overline{WE}			150			120			115	ns	
t_h	Hold Time, $\overline{CS_0}$ or CS_1 to \overline{WE}			40			20			15		

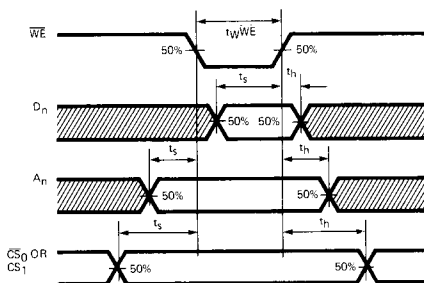
NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

AC WAVEFORMS



OUTPUT ENABLE AND DISABLE TIMES



MINIMUM \overline{WE} PULSE WIDTH AND SET-UP AND HOLD TIMES,
 D_n TO \overline{WE} , A_n TO \overline{WE} , AND $\overline{CS_0}$ OR $\overline{CS_1}$ TO \overline{WE}

NOTE:

Set-up and Hold Times are shown as positive values but may be specified as negative values.