HMA510

16 x 16-Bit CMOS Parallel Multiplier Accumulator

April 1997

Features

- **16 x 16-Bit Parallel Multiplication with Accumulation to a 35-Bit Result**
- **High-Speed (45ns) Multiply Accumulate Time**
- **Low Power CMOS Operation**
  - **I_{CCSB} = 500μA Maximum**
  - **I_{CCOP} = 7.0mA Maximum at 1.0MHz**
- **HMA510 is Compatible with the CY7C510 and the IDT7210**
- **Supports Two's Complement or Unsigned Magnitude Operations**
- **TTL Compatible Inputs/Outputs**
- **Three-State Outputs**

Ordering Information

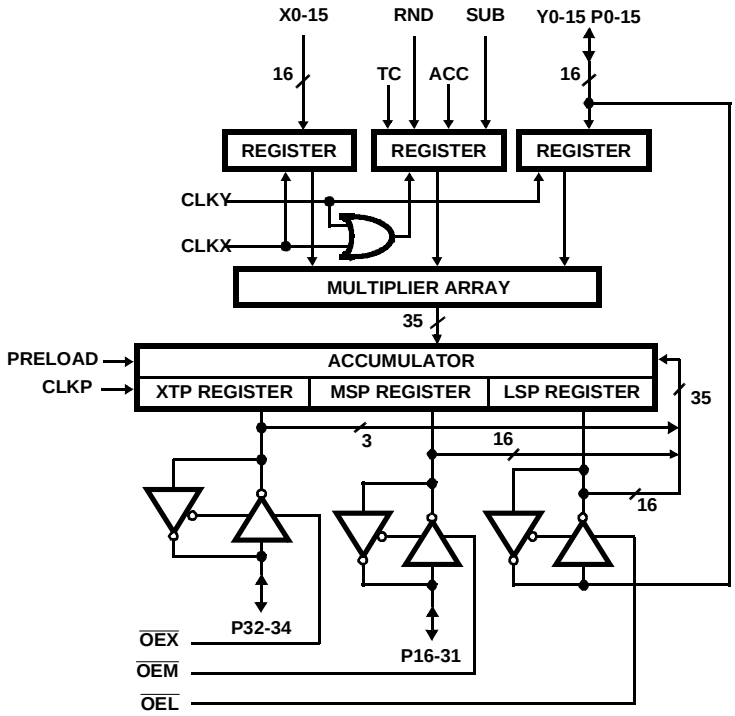
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HMA510JC-45	0 to 70	68 Ld PLCC	N68.95
HMA510JC-55	0 to 70	68 Ld PLCC	N68.95
HMA510GC-55	0 to 70	68 Ld CPGA	G68.B

Description

The HMA510 is a high speed, low power CMOS 16 x 16-bit parallel multiplier accumulator capable of operating at 45ns clocked multiply-accumulate cycles. The 16-bit X and Y operands may be specified as either two's complement or unsigned magnitude format. Additional inputs are provided for the accumulator functions which include: loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, and pre-loading the Accumulator Registers from the external inputs.

All inputs and outputs are registered. The registers are all positive edge triggered, and are latched on the rising edge of the associated clock signal. The 35-bit Accumulator Output Register is broken into three parts. The 16-bit least significant product (LSP), the 16-bit most significant product (MSP), and the 3-bit extended product (XTP) Registers. The XTP and MSP Registers have dedicated output ports, while the LSP Register shares the Y-inputs in a multiplexed fashion. The entire 35-bit Accumulator Output Register may be preloaded at any time through the use of the bidirectional output ports and the preloaded control.

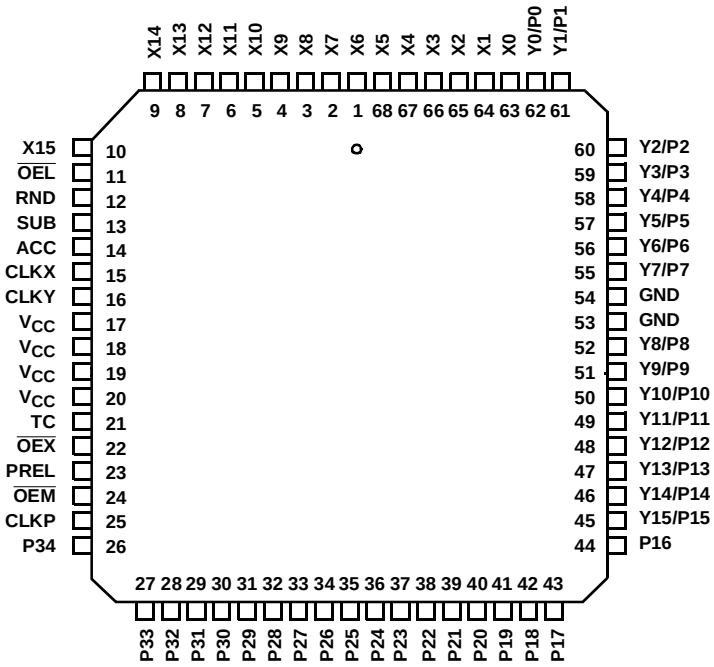
Block Diagram



File Number **2806.2**

Pinouts

68 LEAD PLCC
TOP VIEW



68 LEAD CPGA
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X15	RND	ACC	CLKY	TC	PREL	CLKP	P33	
10	X13	X14	$\overline{OEL}$	SUB	CLKX	V_{CC}	$\overline{OEX}$	$\overline{OEM}$	P34	P32	N/C
9	X11	X12								P30	P31
8	X9	X10								P28	P29
7	X7	X8								P26	P27
6	X5	X6								P24	P25
5	X3	X4								P22	P23
4	X1	X2								P20	P21
3	Y0/P0	X0								P18	P19
2	N/C	Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y8/P8	Y10/ P10	Y12/ P12	Y14/ P14	P16	P17
1		Y2/P2	Y4/P4	Y6/P6	GND	Y9/P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

Pin Descriptions

NAME	PLCC PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	17-20		The +5V power supply pins. 0.1µF capacitors between the V_{CC} and GND pins are recommended.
GND	53, 54		The device ground.
X0-X15	1-10, 63-68	I	X-Input Data. These 16 data inputs provide the multiplicand which may be in two's complement or unsigned magnitude format.
Y0-Y15/ P0-P15	45-52, 55-62	I/O	Y-Input/LSP Output Data. This 16-bit port is used to provide the multiplier which may be in two's complement or unsigned magnitude format. It may also be used for output of the Least Significant Product (P0-P15) or for preloading the LSP Register.
P16-P3	29-44	I/O	MSP Output Data. This 16-bit port is used to provide the Most Significant Product Output (P16-P31). It may also be used to preload the MSP Register.
P32-P34	26-28	I/O	XTP Output Data. This 3-bit port is used to provide the Extended Product Output (P32-P34). It may also be used to preload the XTP Register.
TC	21	I	Two's Complement Control. Input data is interpreted as two's complement when this control is HIGH. A LOW indicates the data is to be interpreted as unsigned magnitude format. This control is latched on the rising edge of CLKX or CLKY.
ACC	14	I	Accumulate Control. When this control is HIGH, the Accumulator Output Register contents are added to or subtracted from the current product, and the result is stored back into the accumulator Output Register. When LOW, the product is loaded into the accumulator Output Register overwriting the current contents. This control is also latched on the rising edge of CLKX or CLKY.
SUB	13	I	Subtract Control. When both SUB and ACC are HIGH, the Accumulator Register contents are subtracted from the current product. When ACC is HIGH and SUB is LOW, the Accumulator Register contents and the current product are summed. The SUB control input is latched on the rising edge of CLKX or CLKY.
RND	12	I	Round Control. When this control is HIGH, a one is added to the most significant bit of the LSP. When LOW, the product is unchanged.
PREL	23	I	Preload Control. When this control is HIGH, the three bidirectional ports may be used to preload the Accumulator Registers. The three-state controls ($\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$) must be HIGH, and the data will be preloaded on the rising edge of CLKP. When this control is LOW, the Accumulator Registers function in a normal manner.
$\overline{OEL}$	11	I	Y-Input/LSP Output Port Three-State Control. When $\overline{OEL}$ is HIGH, the output drivers are in the high impedance state. This state is required for Y-data input or preloading the LSP Register. When $\overline{OEL}$ is LOW, the port is enabled for LSP output.
$\overline{OEM}$	24	I	MSP Output Port Three-State Control. A LOW on this control line enables the port for output. When $\overline{OEM}$ is HIGH, the output drivers are in the high impedance state. This control must be HIGH for preloading the MSP Register.
$\overline{OEX}$	22	I	XTP Output Port Three-State Control. A LOW on this control line enables the port for output. When $\overline{OEX}$ is HIGH, the output drivers are in the high impedance state. This control must be HIGH for preloading the XTP Register.
CLKX	15	I	X-Register Clock. The rising edge of this clock latches the X-Data Input Register along with the TC, ACC, SUB and RND inputs.
CLKY	16	I	Y-Register Clock. The rising edge of this clock latches the Y-Data Input Register along with the TC, ACC, SUB and RND inputs.
CLKP	25	I	Product Register Clock. The rising edge of CLKP latches the LSP, MSP and XTP Registers. If the preload control is active, the data on the I/O ports is loaded into these registers. If preload is not active, the accumulated product is loaded into the registers.

Functional Description

The HMA510 is a high speed 16 x 16-bit multiplier accumulator (MAC). It consists of a 16-bit parallel multiplier follower by a 35-bit accumulator. All inputs and outputs are registered and are latched on the rising edge of the associated clock signal. The HMA510 is divided into four sections: the input section, the multiplier array, the accumulator and the output/preload section.

The input section has two 16-bit Operand Input Registers for the X and Y operands which are latched on the rising edge of CLKX and CLKY respectively. A four bit Control Register (TC, RND, ACC, SUB) is also included and is latched from either of the input clock signals.

The 16 x 16 multiplier array produces the 32-bit product of the input operands. Two's complement or unsigned magnitude operation can be selected by the use of the TC control. The 32-bit result may also be rounded through the use of the RND control. In this case, a '1' is added to the MSB of the LSP (bit P15). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator functions are controlled by the ACC, SUB and PREL control inputs. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be loaded from the bidirectional ports. The Accumulator Registers are updated at the rising edge of the CLKP signal.

The output/preload section contains the Accumulator/Output Register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{OEX}$, $\overline{OEM}$ and $\overline{OEL}$. When PREL is high, the output buffers are in a high impedance state. When one of the controls $\overline{OEX}$, $\overline{OEM}$ or $\overline{OEL}$ are also high, data present at the outputs will be preloaded into the associated register on the rising edge of CLKP. When PREL is low, the signals $\overline{OEX}$, $\overline{OEM}$ and $\overline{OEL}$ are enable controls for their respective three-state output ports.

TABLE 1. PRELOAD FUNCTION TABLE

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	OUTPUT REGISTERS		
				XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = Output Buffers at High Impedance (Disabled).
Q = Output Buffers at LOW Impedance. Contents of Output Register Available Through Output Ports.
PL = Output disabled. Preload data supplied to the output pins will be loaded into the register at the rising edge of CLKP.

TABLE 2. ACCUMULATOR FUNCTION TABLE

PREL	ACC	SUB	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

Input Formats

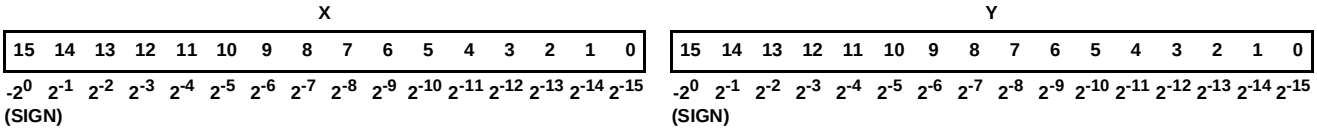


FIGURE 1. FRACTIONAL TWO's COMPLEMENT INPUT

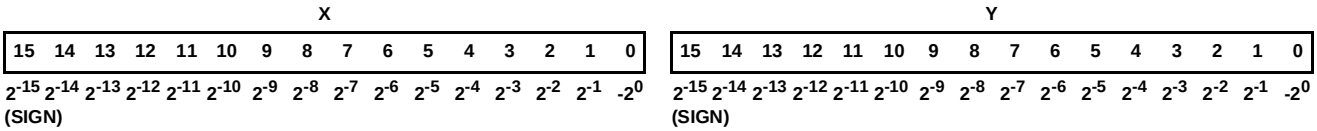


FIGURE 2. INTEGER TWO'S COMPLEMENT INPUT

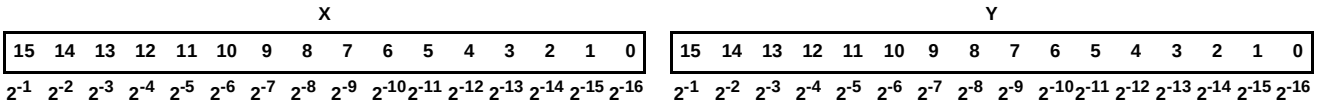


FIGURE 3. UNSIGNED FRACTIONAL INPUT

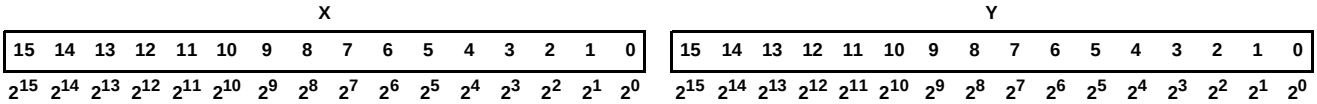


FIGURE 4. UNSIGNED INTEGER INPUT

Output Formats

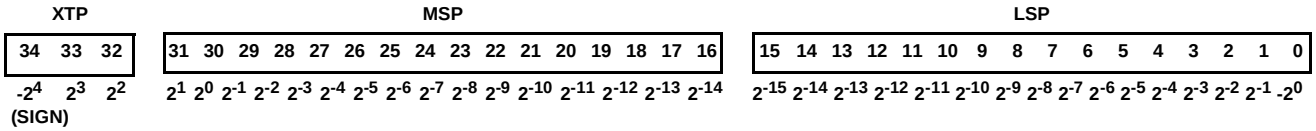


FIGURE 5. TWO'S COMPLEMENT FRACTIONAL OUTPUT

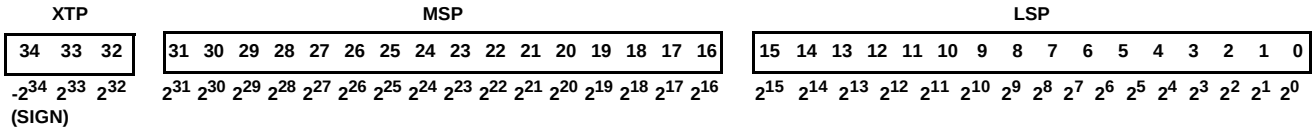


FIGURE 6. TWO'S COMPLEMENT INTEGER OUTPUT

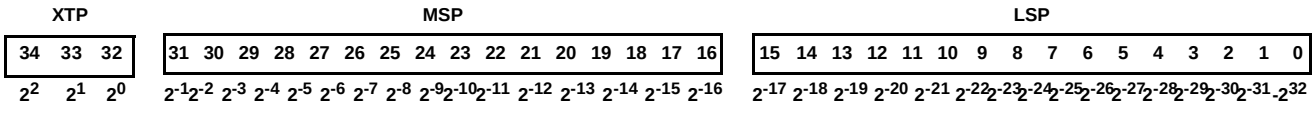


FIGURE 7. UNSIGNED FRACTIONAL OUTPUT

Output Formats

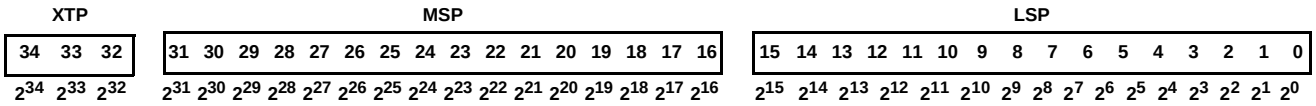


FIGURE 8. UNSIGNED INTEGER OUTPUT

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied. . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
68 Lead PLCC	43.2	15.1
68 Lead PGA	42.69	10.0

Maximum Package Power Dissipation at 70^oC
PLCC 1.7W
PGA 2.46/W
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature
PLCC . . . . . 150^oC
PGA . . . . . 175^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 4800 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0^oC to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400mA, V_{CC} = 4.75V	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +4.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
Output or I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, Outputs Open	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 1.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V (Note 2)	-	7.0	mA

NOTE:

2. Operating Supply Current is proportional to frequency, typical rating is 5.0mA/MHz.

Capacitance T_A = 25^oC, Note 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Capacitance	C_{IN}	FREQ = 1MHz, V_{CC} = Open all Measurements are Referenced to Device Ground	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF
I/O Capacitance	$C_{I/O}$		-	15	pF

NOTES:

3. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0^oC to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	HMA510-45		HMA510-55		UNITS
			MIN	MAX	MIN	MAX	
Multiply Accumulate Time	T_{MA}		-	45	-	55	ns

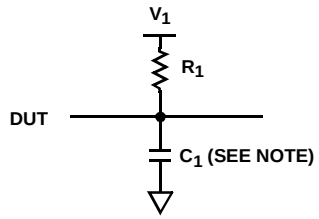
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	HMA510-45		HMA510-55		UNITS
			MIN	MAX	MIN	MAX	
Output Delay	T_D		-	25	-	30	ns
Three-State Enable Time	T_{ENA}	Note 4	-	25	-	30	ns
Three-State Disable Time	T_{DIS}	Note 4	-	25	-	30	ns
Input Setup Time	T_S		18	-	20	-	ns
Input Hold Time	T_H		2	-	2	-	ns
Clock High Pulse Width	T_{PWH}		15	-	20	-	ns
Clock Low Pulse Width	T_{PWL}		15	-	20	-	ns
Output Rise Time	t_R	From 0.8V to 2.0V	-	8	-	8	ns
Output Fall Time	t_F	From 2.0V to 0.8V	-	8	-	8	ns

NOTES:

4. Transition is measured at ±200mV from steady state voltage with loading specified in AC Test Circuit; V_1 = 1.5V, R_1 = 500Ω and C_L = 40pF.
5. For AC Test load, refer to AC Test Circuit with V_1 = 2.4V, R_1 = 500Ω and C_L = 40pF.

AC Test Circuit



NOTE: Includes Stray and Jig Capacitance

AC Testing Input, Output Waveforms

NOTE: AC Testing: All Parameters tested as per test circuit. Input rise and fall times are driven at 1ns/V.

Timing Diagram

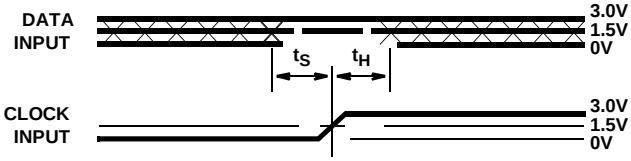


FIGURE 9. SETUP AND HOLD TIME

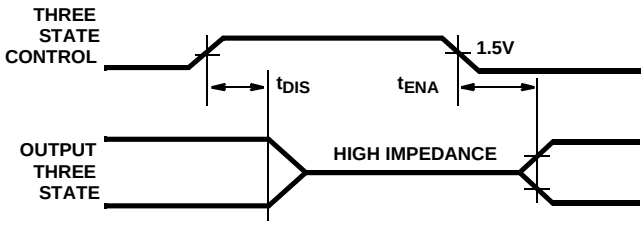


FIGURE 10. THREE-STATE CONTROL

Timing Diagram

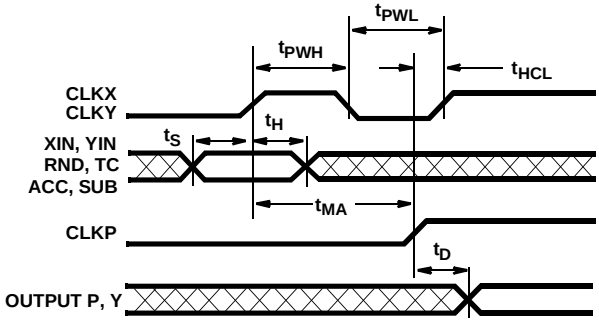


FIGURE 11. HMA510 TIMING DIAGRAM

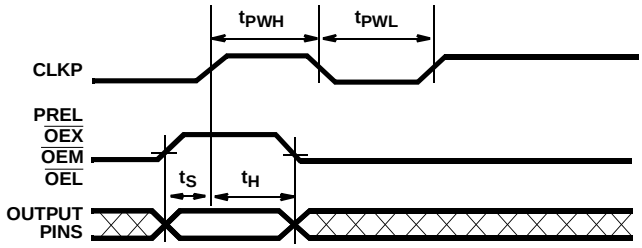


FIGURE 12. PRELOAD TIMING DIAGRAM

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