ONSEMI,

MOSFET – N-Channel, POWERTRENCH[®]

100 V, 2.7 A, 109 m Ω

FDN8601

General Description

This N–Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Features

- Max $r_{DS(on)} = 109 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 1.5 \text{ A}$
- Max $r_{DS(on)} = 175 \text{ m}\Omega$ at $V_{GS} = 6 \text{ V}$, $I_D = 1.2 \text{ A}$
- High Performance Trench Technology for Extremely Low $r_{\mbox{DS}(\mbox{on})}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Primary DC–DC Switch
- Load Switch

MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

		(1 (,
Symbol	Parameter		Ratings	Unit
V _{DS}	Drain to Source Volta	ige	100	V
V _{GS}	Gate to Source Voltag	ge	±20	V
I _D	Continuous (Note 1a)	2.7	А	
	Pulsed	12		
E _{AS}	Single Pulse Avalanche Energy (Note 3)		13	mJ
PD	Power Dissipation	oation (Note 1a)		W
		(Note 1b)	0.6	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Symbol	Parameter	Ratings	Unit
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction to Case (Note 1)	75	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	80	°C/W

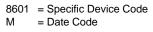
V _{DS}	r _{DS(on)} MAX	I _D MAX
20 V	109 mΩ @ 10 V	2.7 A
	175 mΩ @ 6 V	



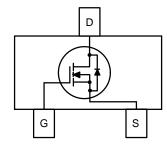
SOT-23/SUPERSOT[™]-23, 3 LEAD, 1.4x2.9 CASE 527AG

MARKING DIAGRAM





PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise noted)

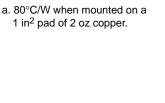
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
OFF CHARA	CTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$	100	_	_	V
$\frac{\Delta {\sf BV}_{\sf DSS}}{\Delta {\sf T}_{\sf J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25°C	-	68	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V	_	_	±100	nA
ON CHARAC	TERISTICS (Note 2)					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$	2.0	3.0	4.0	V
$\frac{\Delta V_{\text{GS(th)}}}{\Delta T_{\text{J}}}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \ \mu\text{A}$, referenced to 25°C	-	-8	-	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 1.5 A	-	85.4	109	mΩ
		V _{GS} = 6 V, I _D = 1.2 A	-	117	175	1
		V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	-	143	183	
9FS	Forward Transconductance	V _{DS} = 10 V, I _D = 1.5 A	_	8	_	S
OYNAMIC CH	HARACTERISTICS					
C _{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	156	210	pF
C _{oss}	Output Capacitance		_	47	65	pF
C _{rss}	Reverse Transfer Capacitance		_	2.7	5	pF
Rg	Gate Resistance		-	1.0	-	Ω
SWITCHING	CHARACTERISTICS (Note 2)					
t _{d(on)}	Turn–On Delay Time	$V_{DD} = 50 \text{ V}, \text{ I}_{D} = 1.5 \text{ A}, \text{ V}_{GS} = 10 \text{ V},$	-	4.3	10	ns
t _r	Rise Time	$R_{GEN} = 6 \Omega$	-	1.3	10	ns
t _{d(off)}	Turn–Off Delay Time		_	7.8	16	ns
t _f	Fall Time		-	3.4	10	ns
Qg	Total Gate Charge	V_{GS} = 0 V to 10 V V_{DD} = 50 V, I_{D} = 1.5 A	-	3	5	nC
Qg	Total Gate Charge $V_{GS} = 0 V \text{ to } 5 V V_{DD} = 50 V, I_D = 1.5 A$		-	1.8	3	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 50 V, I _D = 1.5 A	-	0.9	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	0.8	-	nC
ORAIN-SOU	RCE DIODE CHARACTERISTICS AND MAXI	MUM RATINGS				
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.5 A (Note 2)	-	0.81	1.3	V
t-r	Reverse Recovery Time	Ir = 1.5 A di/dt = 100 A/us	_	29	46	ns

Reverse Recovery Time $I_F = 1.5 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ t_{rr} 29 46 ns Qrr Reverse Recovery Charge 15 27 nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

 $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. 1.







2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%.

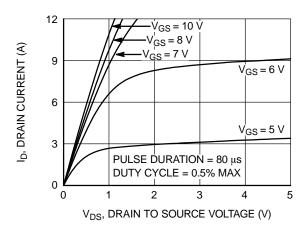
3. Starting $T_J = 25^{\circ}C$; N-ch: L = 3 mH, $I_{AS} = 3 \text{ A}$, $V_{DD} = 100 \text{ V}$, $V_{GS} = 10 \text{ V}$.

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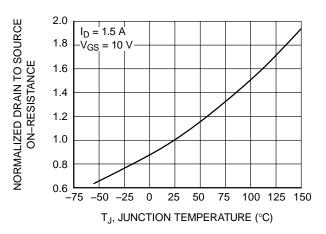
b. $180^{\circ}C/W$ when mounted on a minimum pad.

TYPICAL CHARACTERISTICS

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$









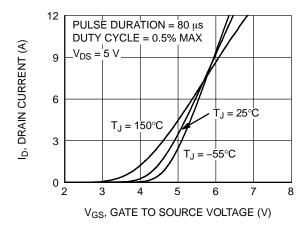


Figure 5. Transfer Characteristics

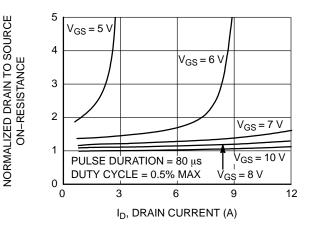


Figure 2. Normalized On–Resistance vs. Drain Current and Gate Voltage

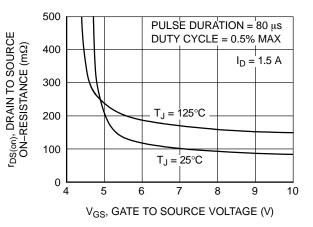
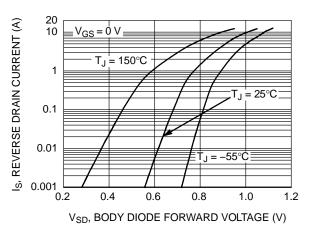


Figure 4. On–Resistance vs. Gate to Source Voltage





TYPICAL CHARACTERISTICS

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$ (continued)

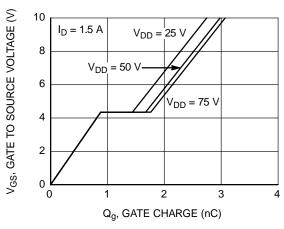


Figure 7. Gate Charge Characteristics

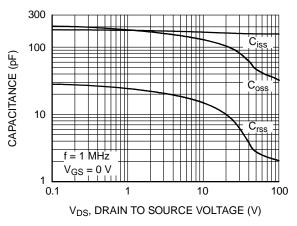


Figure 8. Capacitance vs. Drain to Source Voltage

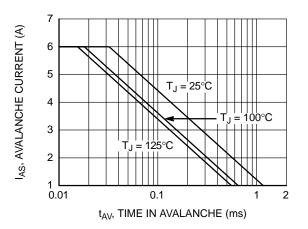


Figure 9. Unclamped Inductive Switching Capability

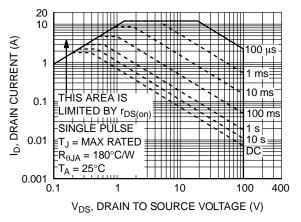


Figure 10. Forward Bias Safe Operating Area

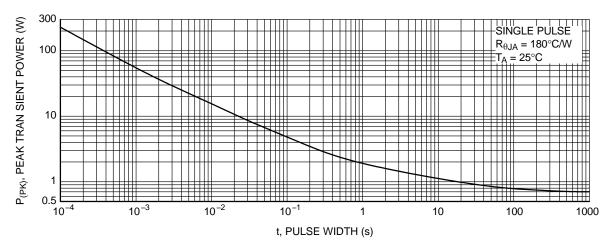


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$ (continued)

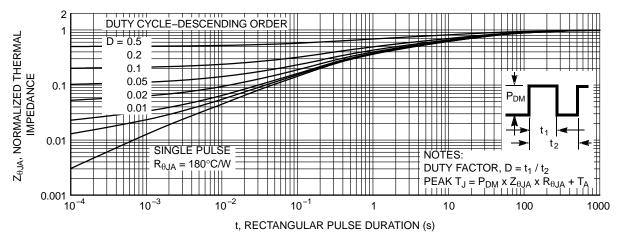


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDN8601	8601	SOT–23/SUPERSOT–23, 3 LEAD, 1.4x2.9 (Pb–Free, Halide Free)	7"	8 mm	3000 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

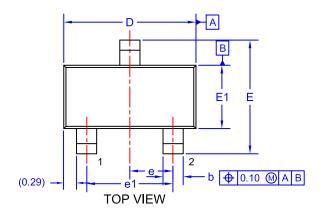
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SOT-23/SUPERSOT [™] -23, 3 LEAD, 1.4x2.9 CASE 527AG ISSUE A

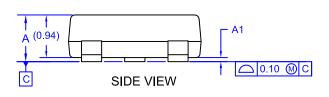
DATE 09 DEC 2019

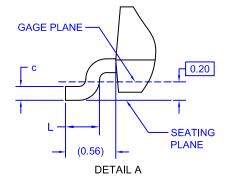


2.	ASME Y14.5M, 2009. ALL DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.						
	DIM MIN. NOM. MAX.						
	А	0.85	0.95	1.12			
	A1	0.00	0.05	0.10			
	b	0.370	0.435	0.508			
	с	0.085	0.150	0.180			
	D	2.80	2.92	3.04			
	Е	2.31	2.51	2.71			
	E1	1.20	1.40	1.52			
	е	0.95 BSC 1.90 BSC					
	e1						
	L	0.33	0.38	0.43			

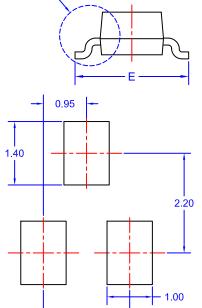
NOTES: UNLESS OTHERWISE SPECIFIED

1. DIMENSIONING AND TOLERANCING PER









LAND PATTERN RECOMMENDATION* *FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- 1.90

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot "●", may or may not be present. Some products may not follow the Generic Marking.

•	(Note: Microdot may be in	either location) not follow the Generic Marking.	,	
DOCUMENT NUMBER:	98AON34319E	Electronic versions are uncontrolled except when accessed directly from the D Printed versions are uncontrolled except when stamped "CONTROLLED COPY		
DESCRIPTION:	SOT-23/SUPERSOT-23, 3	LEAD, 1.4X2.9	PAGE 1 OF 1	

XXX = Specific Device Code

= Pb-Free Package

= Month Code

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GENERIC MARKING DIAGRAM*

XXXM=

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