

T-35-19

2-A Power-Switching Transistors

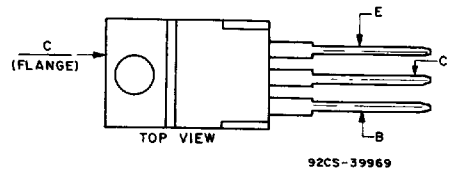
High-Voltage N-P-N Types for Off-Line Power Supplies and Other Switching Applications

Features:

- Performance information tailored for switching applications
- 100°C maximum limits specified for:
 - Switching times
 - Saturation voltages
 - Leakage currents
- 300 to 400V $V_{CE0(sus)}$
- Very fast turn-off $t_f < 180 \text{ nsec (typ.)}@1.5A$

The D44TD-series of n-p-n power transistors are designed for use in switching applications requiring high-voltage capability, fast switching speeds, and low-saturation voltages. They are particularly suited for off-line switching power supplies, solid state lighting ballast, inverters, solenoid/relay drivers, and deflection circuits.

TERMINAL DESIGNATIONS



POWER TRANSISTORS

JEDEC TO-220AB

MAXIMUM RATINGS ($T_A = 25^\circ \text{C}$) (unless otherwise specified)

RATING	SYMBOL	D44TD3	D44TD4	D44TD5	UNITS
Collector-Emitter Voltage	V_{CE0}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEX}	300	350	400	Volts
Collector-Emitter Voltage	V_{CEV}	400	500	600	Volts
Emitter Base Voltage	V_{EBO}	7	7	7	Volts
Collector Current — Continuous	I_C	2	2	2	A
	I_{CM}	4	4	4	A
Base Current — Continuous	I_B	0.5	0.5	0.5	A
	I_{BM}	1	1	1	A
Total Power Dissipation @ $T_c = 25^\circ \text{C}$ Derate above 25°C @ $T_c = 100^\circ \text{C}$	P_D	50	50	50	Watts
		20	20	20	
		0.4	0.4	0.4	W/ $^\circ \text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	$^\circ \text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.5	2.5	2.5	$^\circ \text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	$^\circ \text{C/W}$
Maximum Lead Temperature for Soldering Purpose: 1/8" from Case for 5 Seconds	T_L	260	260	260	$^\circ \text{C}$

(1) Pulse condition, $t_p \leq 5 \text{ msec}$.

D44TD Series**ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$) (unless otherwise specified)

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT	
T-35-19					
OFF CHARACTERISTICS ⁽¹⁾					
Collector-Emitter Sustaining Voltage ($I_C = 25\text{mA}$, $I_B = 0$)	D44TD3 D44TD4 D44TD5	$V_{CE0(sus)}$	300 350 400	— — —	Volts
Collector-Emitter Voltage ($I_C = 2.0\text{mA}$, $I_{B1} = I_{B2} = .4\text{A}$) ($V_{BE} = -5\text{V}$, $L = 200\ \mu\text{h}$)	D44TD3 D44TD4 D44TD5	V_{CEX}	300 350 400	— — —	Volts
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(OFF)} = -1.5\text{V}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(OFF)} = -1.5\text{V}$, $T_C = 100^\circ\text{C}$)		I_{CEV}	— —	0.1 1.0	mA
Emitter Cutoff Current ($V_{EB} = 7\text{V}$, $I_C = 0$)		I_{EBO}	—	1.0	mA

SECOND BREAKDOWN

Second Breakdown with Base Forward Biased	FBSOA	SEE FIGURE 13
Clamped Inductive SOA with Base Reversed Bias	RBSOA	SEE FIGURE 14

ON CHARACTERISTICS⁽¹⁾

DC Current Gain ($I_C = 1\text{A}$, $V_{CE} = 2\text{V}$) ($I_C = 2\text{A}$, $V_{CE} = 3\text{V}$)	h_{FE}	8 5	— —	—
Collector-Emitter Saturation Voltage ($I_C = 1\text{A}$, $I_B = .2\text{A}$) ($I_C = 2\text{A}$, $I_B = .4\text{A}$) ($I_C = 1\text{A}$, $I_B = .2\text{A}$, $T_C = 100^\circ\text{C}$)	$V_{CE(SAT)}$	— — —	0.6 1.0 1.0	Volts
Base-Emitter Saturation Voltage ($I_C = 2\text{A}$, $I_B = .4\text{A}$) ($I_C = 2\text{A}$, $I_B = .4\text{A}$, $T_C = 100^\circ\text{C}$)	$V_{BE(SAT)}$	— —	1.2 1.2	Volts

DYNAMIC CHARACTERISTICS

Current Gain — Bandwidth Product ($I_C = .25\text{A}$, $V_{CE} = 10\text{V}$, $f_{test} = 1.0\text{MHz}$)	f_T	15	50	MHz
Output Capacitance ($V_{CB} = 10\text{V}$, $I_E = 0$, $f = 0.1\text{MHz}$)	C_{OB}	10	25	pF

SWITCHING CHARACTERISTICS

		MAXIMUM			
Resistive Load (See Figure 17 for Test Circuit)		T_C	25°C	100°C	
Delay Time	$V_{CC} = 250\text{V}$, $I_C = 1.5\text{A}$ $I_{B1} = I_{B2} = 0.3\text{A}$, $t_p = 25\ \mu\text{sec}$	t_d	.06	.08	μs
Rise Time		t_r	0.6	0.8	μsec
Storage Time		t_s	2.5	3.0	μsec
Fall Time		t_f	0.5	0.8	μsec
Inductive Load, Clamped (See Figure 17 for Test Circuit)					
Storage Time	$V_{CLAMP} = 250\text{V}$, $I_C = 1.5\text{A}$, $I_{B1} = I_{B2} = 0.3\text{A}$, $t_p = 25\ \mu\text{sec}$ $V_{BE(OFF)} = -5\text{V}$	t_{sv}	3.0	3.5	μs
Fall Time		t_f	0.3	0.6	μsec
		TYPICAL			
Storage Time	$L = 200\ \mu\text{h}$	t_s	2.1	2.6	μsec
Fall Time		t_f	0.18	0.23	μsec

(1) Pulse Duration = $300\ \mu\text{s}$, Duty Factor $\leq 2\%$. Do not measure on a curve tracer.

TYPICAL DC CHARACTERISTICS

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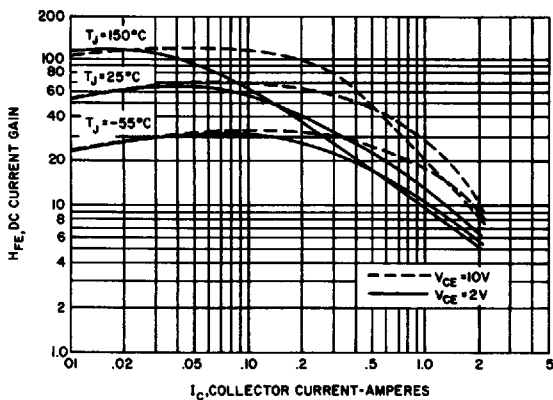


FIGURE 1. DC CURRENT GAIN

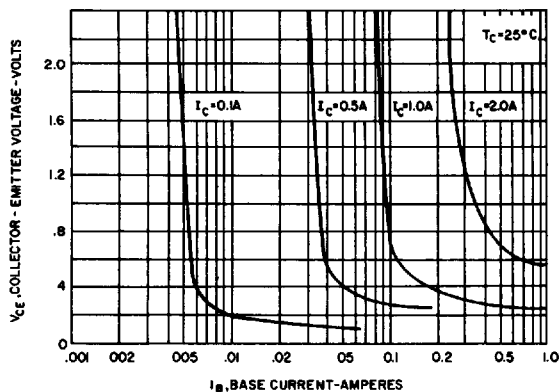


FIGURE 2. COLLECTOR SATURATION REGION

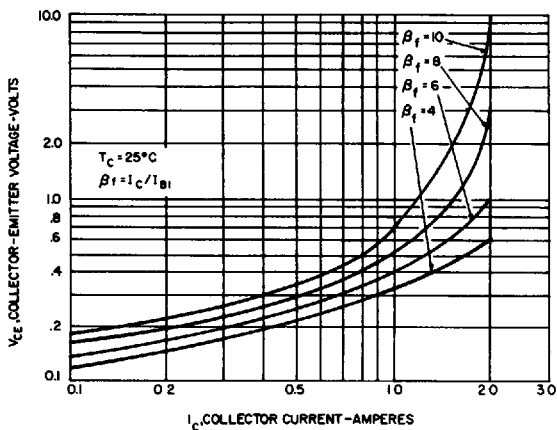


FIGURE 3. $V_{CE(SAT)}$ VS. I_C , $T_C = 25^\circ C$

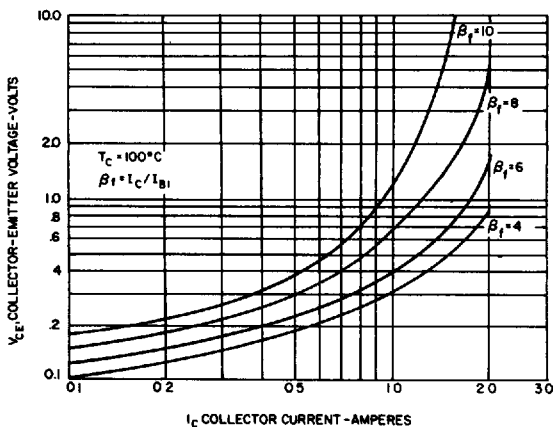


FIGURE 4. $V_{CE(SAT)}$ VS. I_C , $T_C = 100^\circ C$

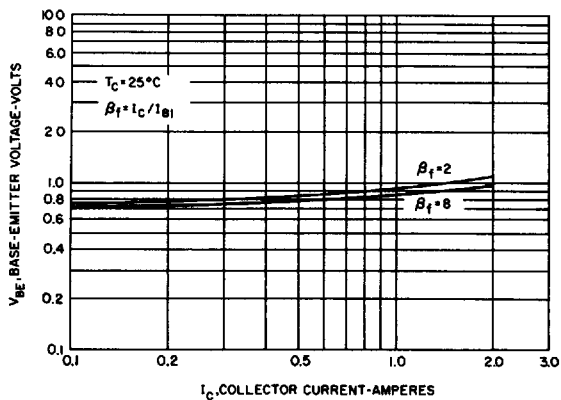


FIGURE 5. $V_{BE(SAT)}$ VS. I_C

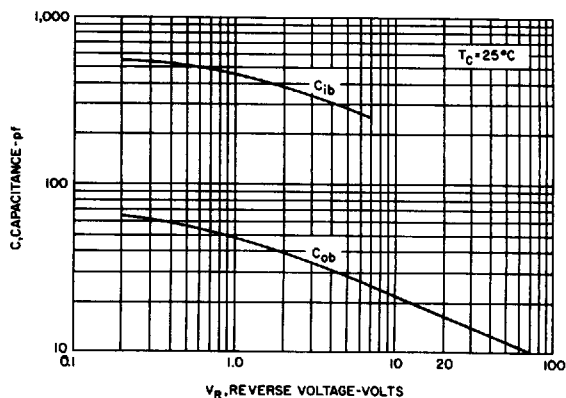


FIGURE 6. CAPACITANCE

POWER TRANSISTORS

TYPICAL SWITCHING CHARACTERISTICS

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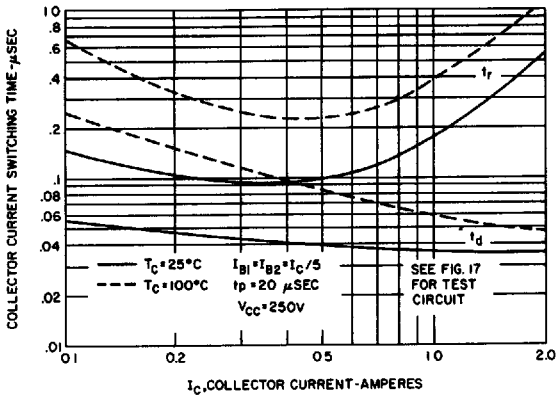


FIGURE 7. TURN-ON TIME RESISTIVE LOAD

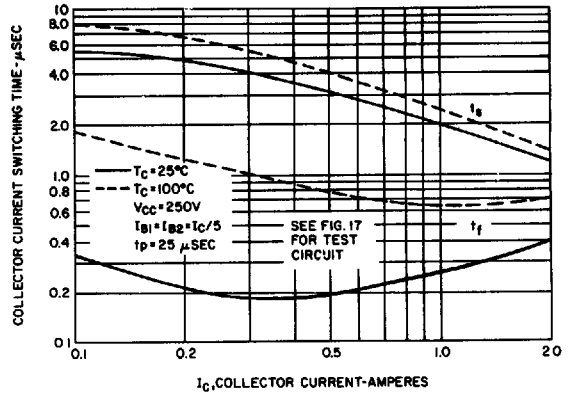


FIGURE 8. TURN-OFF TIME RESISTIVE LOAD

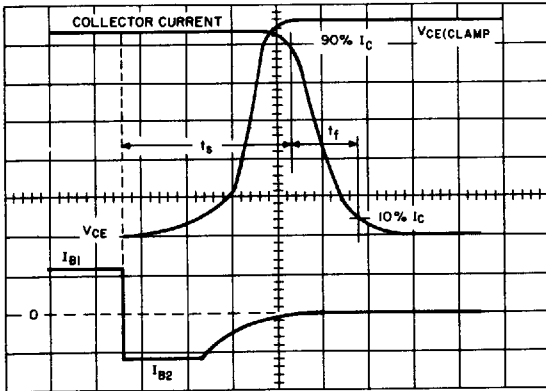


FIGURE 9. INDUCTIVE TURN-OFF WAVEFORMS

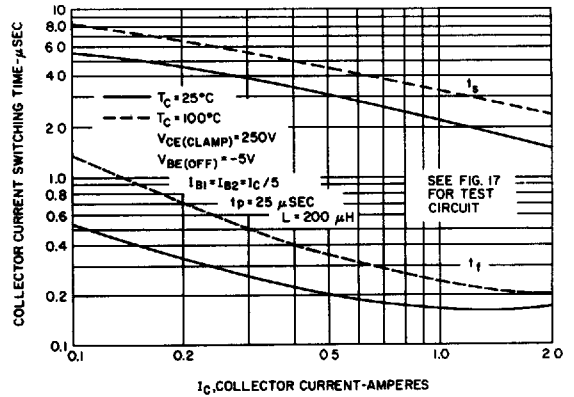


FIGURE 10. CLAMPED INDUCTIVE TURN-OFF TIME

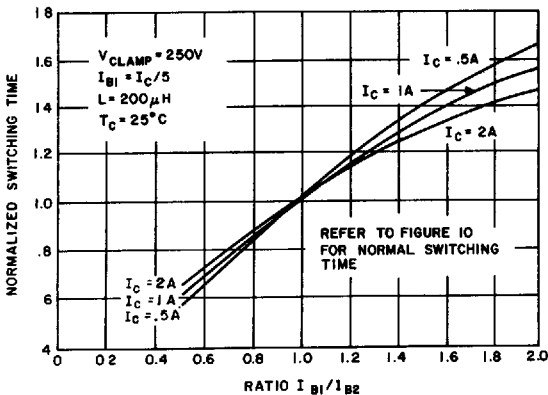


FIGURE 11. STORAGE TIME VARIATION WITH I_{B2}

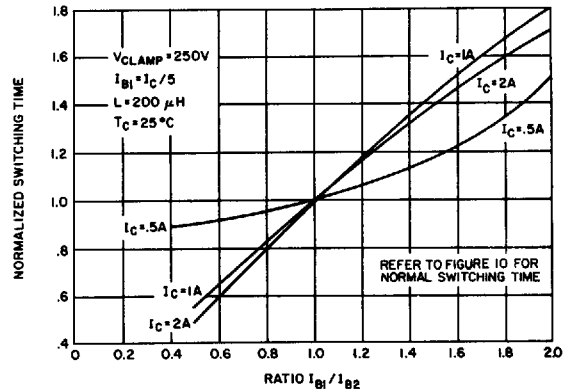


FIGURE 12. FALL TIME VARIATION WITH I_{B2}

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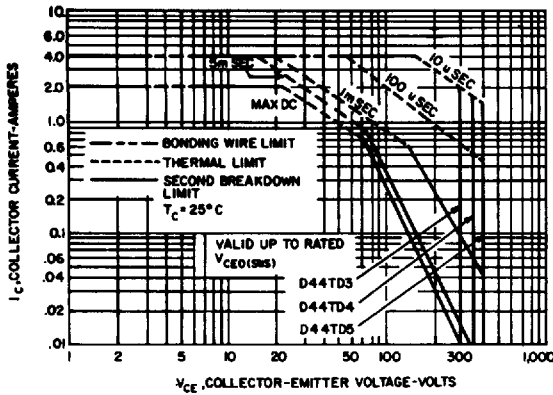


FIGURE 13. FORWARD BIAS SAFE OPERATING AREA

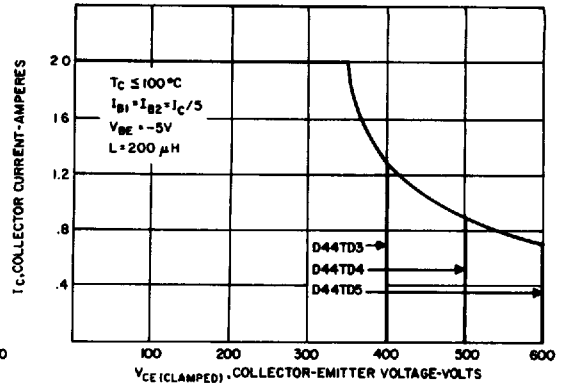


FIGURE 14. CLAMPED REVERSE BIAS SAFE OPERATING AREA

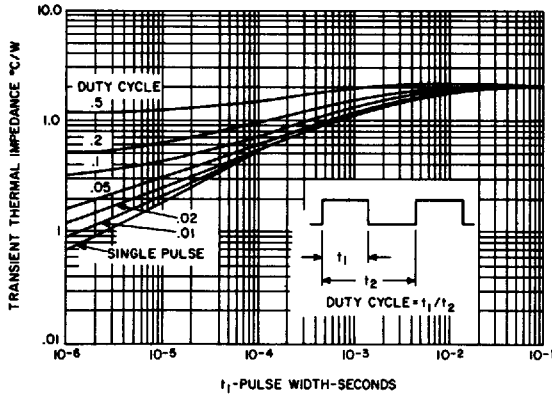


FIGURE 15. TRANSIENT THERMAL RESPONSE

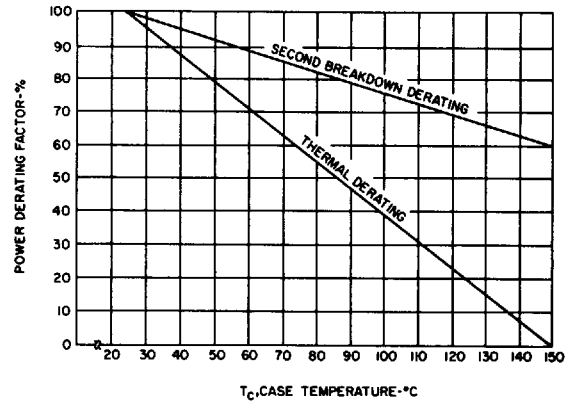


FIGURE 16. POWER DERATING CURVE

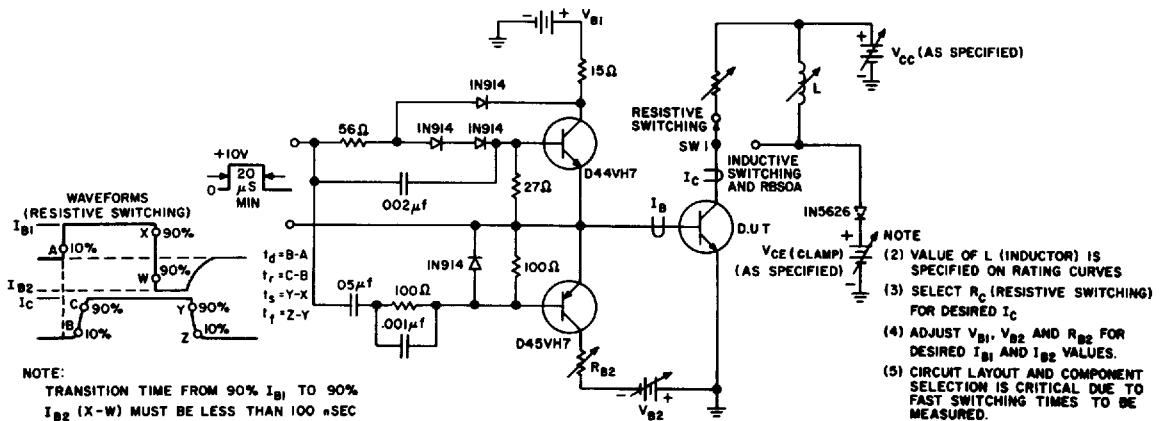


FIGURE 17. TEST CIRCUIT FOR SWITCHING TIMES AND RBSOA