

Features

- Very high speed: 45 ns
- Temperature ranges
 - Industrial: -40 °C to +85 °C
- Wide voltage range: 2.20 V–3.60 V
- Pin compatible with CY62137CV/CV25/CV30/CV33, CY62137V, and CY62137EV30
- Ultra low standby power
 - Typical standby current: 1 μA
 - Maximum standby current: 5 μA (Industrial)
- Ultra low active power
 - Typical active current: 1.6 mA at f = 1 MHz (45 ns speed)
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Byte power down feature
- Available in Pb free 48-ball very fine-pitch ball grid array (VFBGA) and 44-pin thin small outline package (TSOP) II package

Functional Description

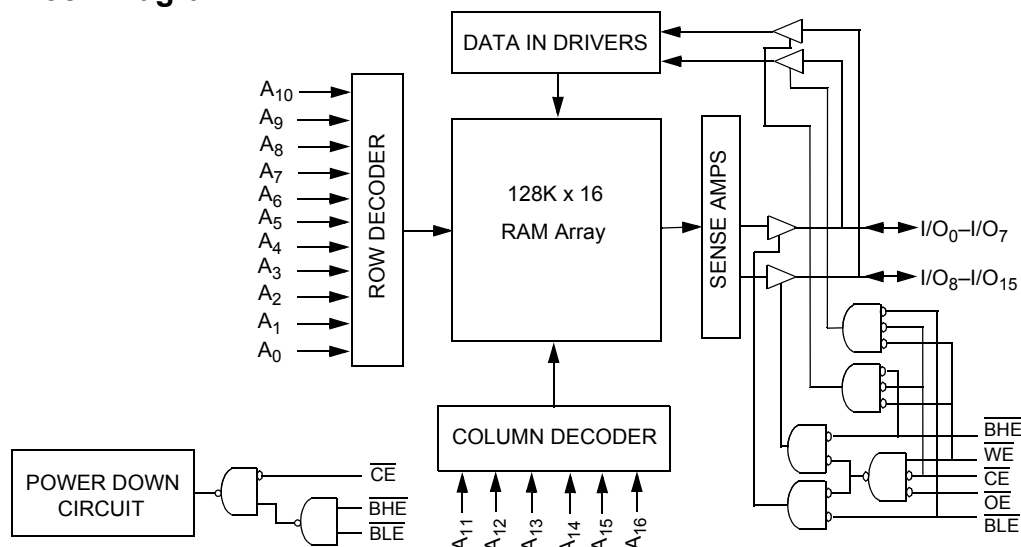
The CY62137FV30 is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features

advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (\overline{CE} HIGH or both \overline{BLE} and \overline{BHE} are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state in the following conditions when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), both the Byte High Enable and the Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during an active write operation (\overline{CE} LOW and \overline{WE} LOW).

Write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇) is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Read from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW, while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See the Truth Table on page 11 for a complete description of read and write modes.

Logic Block Diagram



Contents

Product Portfolio	3	Truth Table	11
Pin Configuration	3	Ordering Information	12
Maximum Ratings	4	Ordering Code Definitions	12
Operating Range	4	Package Diagrams	13
Electrical Characteristics	4	Acronyms	14
Capacitance	5	Document Conventions	14
Thermal Resistance	5	Units of Measure	14
AC Test Loads and Waveforms	5	Document History Page	15
Data Retention Characteristics	6	Sales, Solutions, and Legal Information	16
Data Retention Waveform	6	Worldwide Sales and Design Support	16
Switching Characteristics	7	Products	16
Switching Waveforms	8	PSoC Solutions	16

Product Portfolio

Product	Range	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
		f = 1MHz		f = f _{max}							
		Min	Typ ^[1]	Max		Typ ^[1]	Max	Typ ^[1]	Max		
CY62137FV30LL	Industrial	2.2 V	3.0 V	3.6 V	45	1.6	2.5	13	18	1	5

Pin Configuration

Figure 1. 48-Ball VFBGA Pinout^[2, 3]

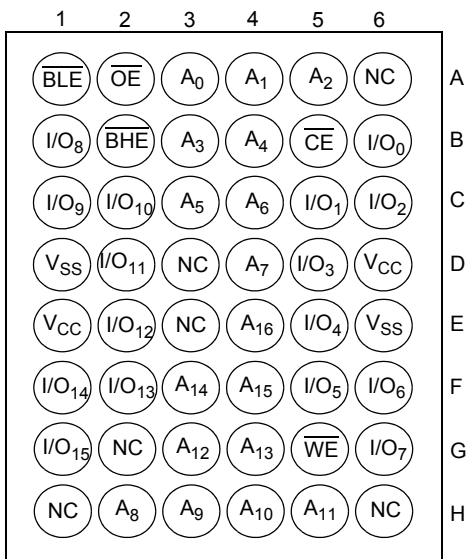
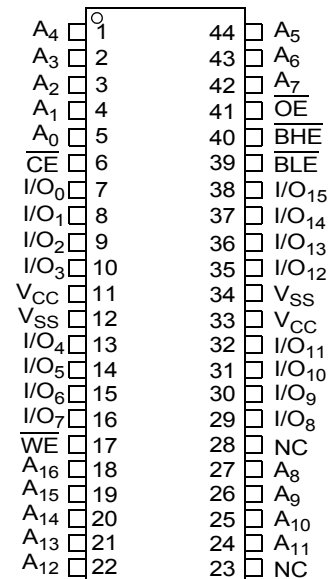


Figure 2. 44-Pin TSOP II^[2]



Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
2. NC pins are not connected on the die.
3. Pins D3, H1, G2, H6 and H3 in the VFBGA package are address expansion pins for 4 Mb, 8 Mb, 16 Mb, and 32 Mb and 64 Mb respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	-65 °C to + 150 °C
Ambient temperature with power applied	-55 °C to + 125 °C
Supply voltage to ground potential	-0.3 V to 3.9 V
DC voltage applied to outputs in High Z state ^[4, 5]	-0.3 V to 3.9 V

DC input voltage ^[5]	-0.3 V to 3.9 V
Output current into outputs (LOW)	20 mA
Static discharge voltage	> 2001 V (MIL-STD-883, method 3015)
Latch up current	> 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62137FV30LL	Industrial	-40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial)			Unit	
			Min	Typ ^[7]	Max		
V _{OH}	Output high voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OH} = -0.1 mA	2.0	-	-	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OH} = -1.0 mA	2.4	-	-	V
V _{OL}	Output low voltage	2.2 ≤ V _{CC} ≤ 2.7	I _{OL} = 0.1 mA	-	-	0.4	V
		2.7 ≤ V _{CC} ≤ 3.6	I _{OL} = 2.1 mA	-	-	0.4	V
V _{IH}	Input high voltage	2.2 ≤ V _{CC} ≤ 2.7		1.8	-	V _{CC} + 0.3	V
		2.7 ≤ V _{CC} ≤ 3.6		2.2	-	V _{CC} + 0.3	V
V _{IL}	Input low voltage	2.2 ≤ V _{CC} ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V _{CC} ≤ 3.6		-0.3	-	0.8	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}		-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , Output disabled		-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{max} = 1/t _{RC}	V _{CC} = V _{CC(max)}	-	13	18	mA
		f = 1 MHz	I _{OUT} = 0 mA CMOS levels	-	1.6	2.5	
I _{SB1} ^[8]	Automatic power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V, or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (address and data only), f = 0 (OE and WE), V _{CC} = V _{CC(max)}		-	1	5	μA
I _{SB2} ^[8]	Automatic power-down current – CMOS inputs	CE ≥ V _{CC} - 0.2 V or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)}		-	1	5	μA

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a minimum of 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.

Capacitance

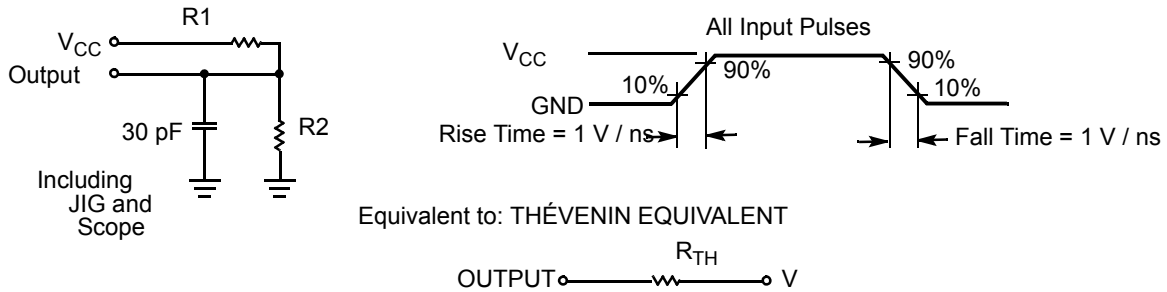
Parameter ^[9]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[9]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ _{JA}	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two layer printed circuit board	75	77	°C/W
Θ _{JC}	Thermal resistance (Junction to case)		10	13	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R ₁	16667	1103	Ω
R ₂	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Notes

9. Tested initially and after any design or process changes that may affect these parameters.

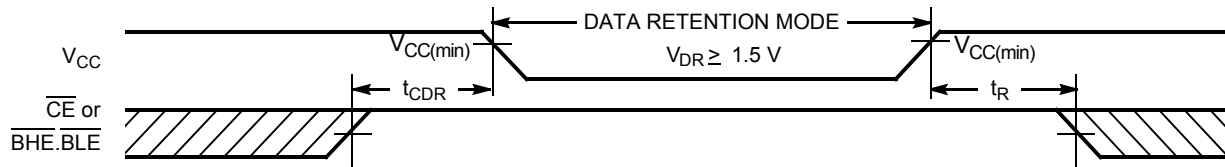
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR} ^[11]	Data retention current	$V_{CC} = 1.5\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, or (\overline{BHE} and \overline{BLE}) $\geq V_{CC} - 0.2\text{ V}$ $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	4	μA
t_{CDR} ^[12]	Chip deselect to data retention time		0	–	–	ns
t_R ^[13]	Operation recovery time	CY62137FV30LL-45	45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform^[14]



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(\text{typ})}$, $T_A = 25\text{ }^\circ\text{C}$.
11. Chip enable (\overline{CE}) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} specification. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
14. $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Parameter ^[15, 16]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[17]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[17, 18]	–	18	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[17]	10	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[17, 18]	–	18	ns
t_{PU}	\overline{CE} LOW to power up	0	–	ns
t_{PD}	\overline{CE} HIGH to power down	–	45	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[17, 19]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[17, 18]	–	18	ns
Write Cycle ^[20]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE} LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[17, 18]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[17]	10	–	ns

Notes

15. Test conditions for all parameters, other than tristate parameters, assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in [AC Test Loads and Waveforms on page 5](#).
16. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. Please see [application note AN13842](#) for further clarification.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. If both byte enables are toggled together, this value is 10 ns.
20. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5. Read Cycle 1: Address Transition Controlled [21, 22]

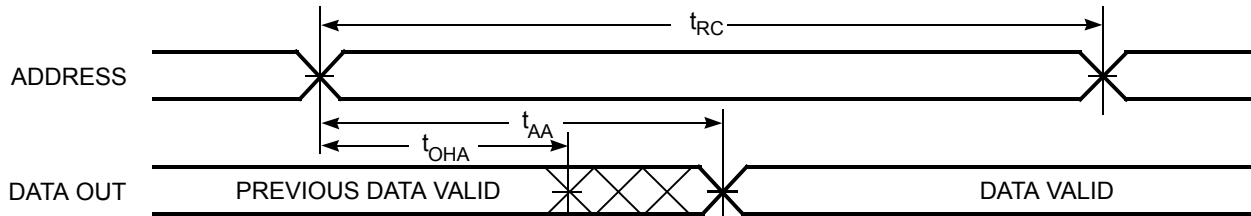
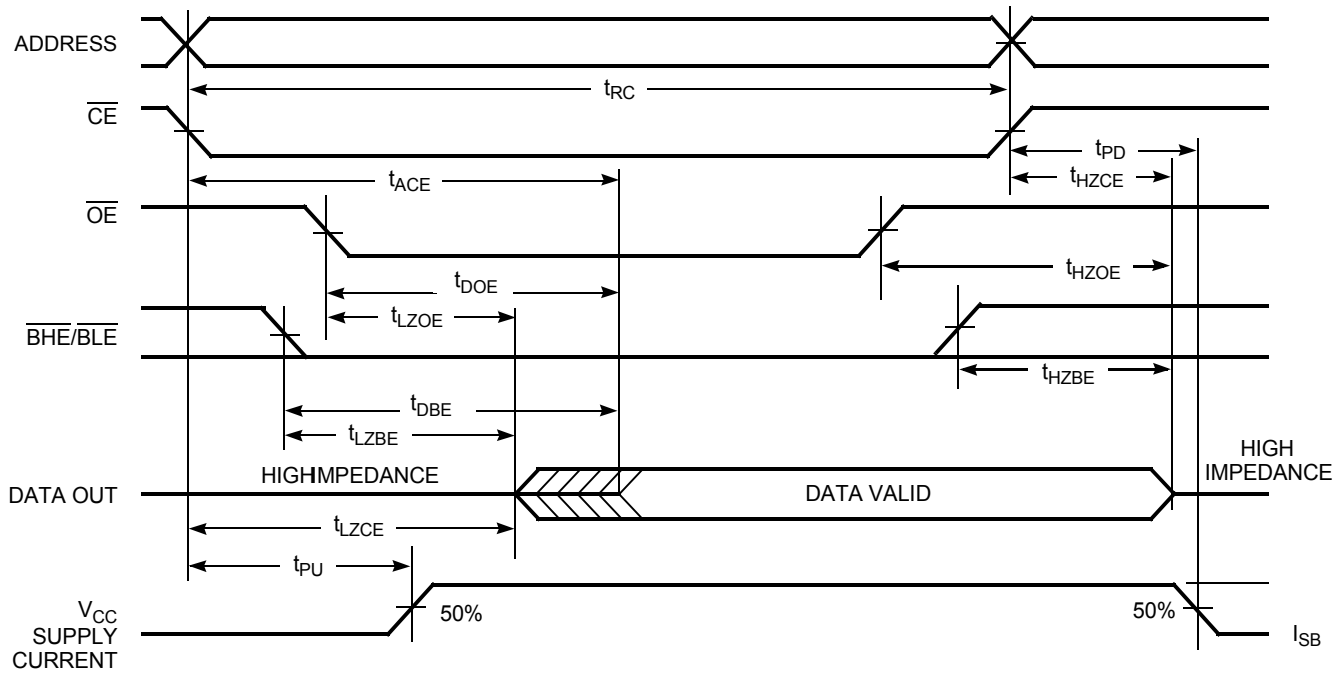


Figure 6. Read Cycle 2: \overline{OE} Controlled [22, 23]



Notes

21. The device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
22. \overline{WE} is HIGH for read cycle.
23. Address valid before or similar to \overline{CE} and \overline{BHE} , \overline{BLE} transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle 1: $\overline{\text{WE}}$ Controlled [24, 25, 26]

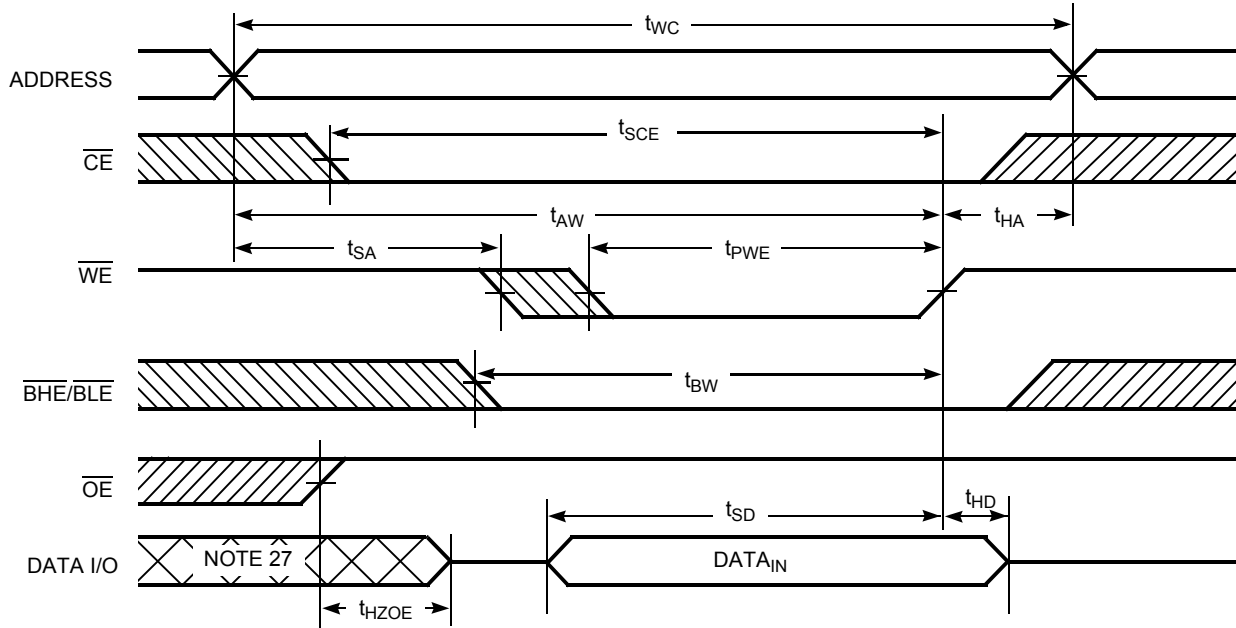
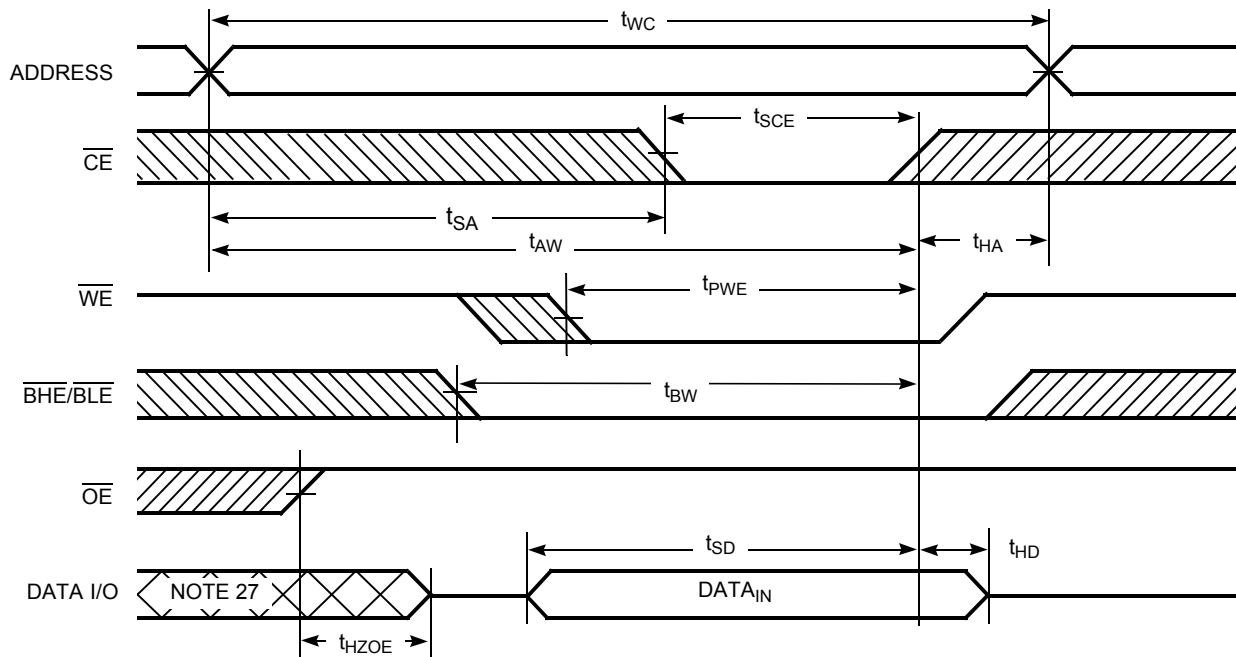


Figure 8. Write Cycle 2: $\overline{\text{CE}}$ Controlled [24, 25, 26]



Notes

- 24. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, $\overline{\text{CE}} = V_{IL}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IL}$. All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.
- 25. Data I/O is high impedance if $\overline{\text{OE}} = V_{IH}$.
- 26. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle 3: \overline{WE} Controlled, \overline{OE} LOW [28]

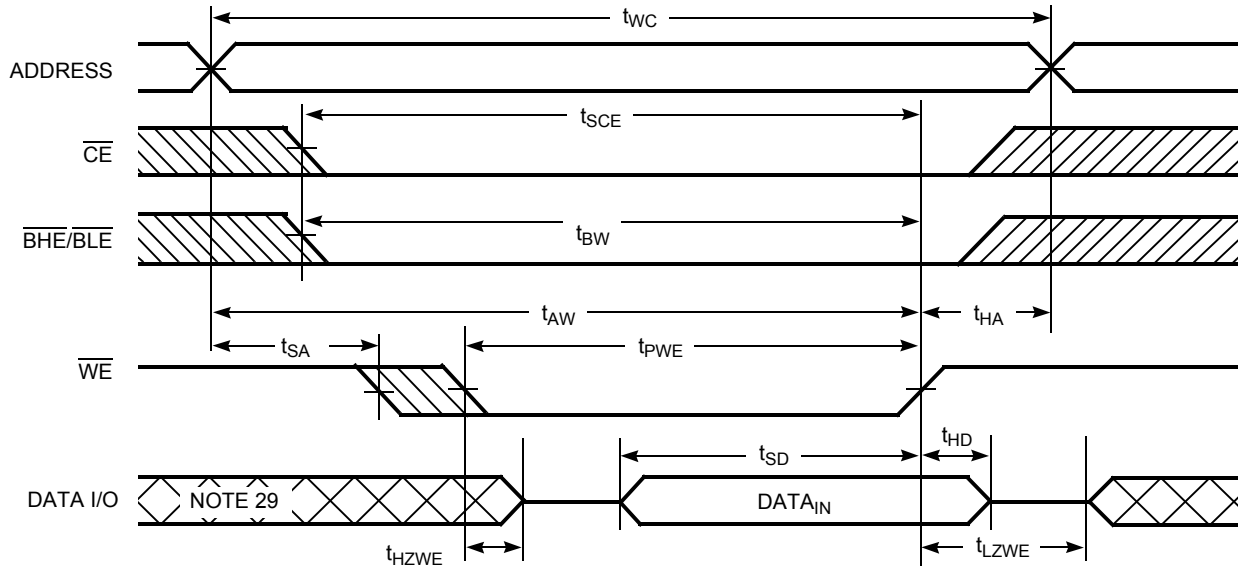
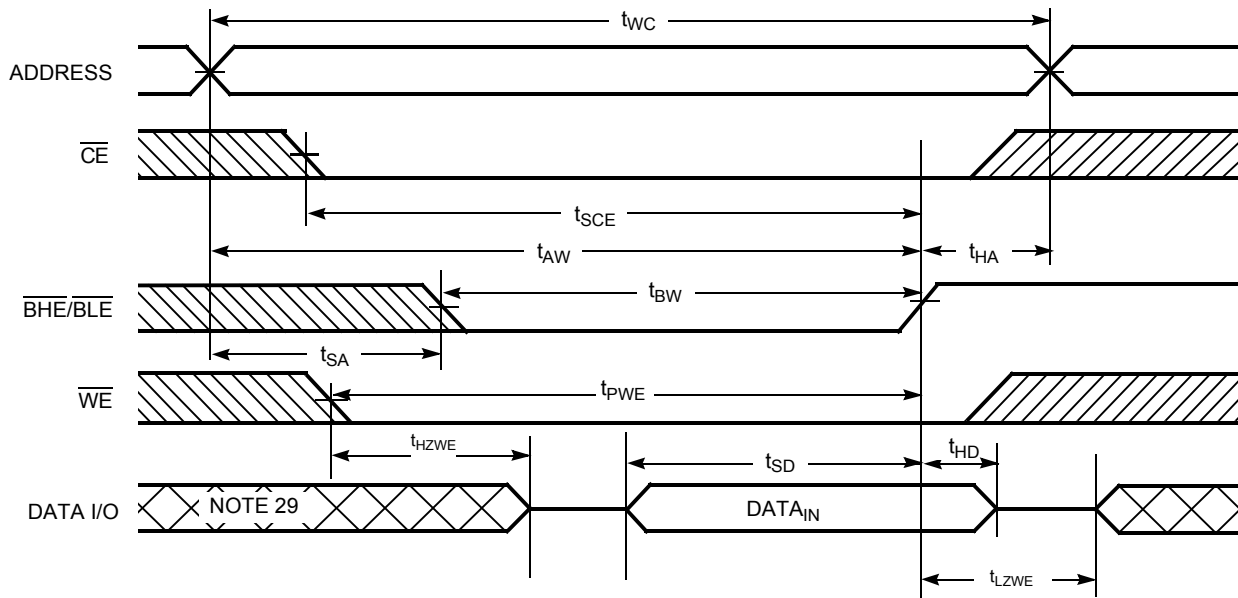


Figure 10. Write Cycle 4: $\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW [28]



Notes

- 28. If \overline{CE} goes HIGH simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 29. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs or Outputs	Mode	Power
H	X	X	X ^[30]	X ^[30]	High Z	Deselect or power-down	Standby (I_{SB})
X ^[30]	X	X	H	H	High Z	Deselect or power-down	Standby (I_{SB})
L	H	L	L	L	Data out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})

Note

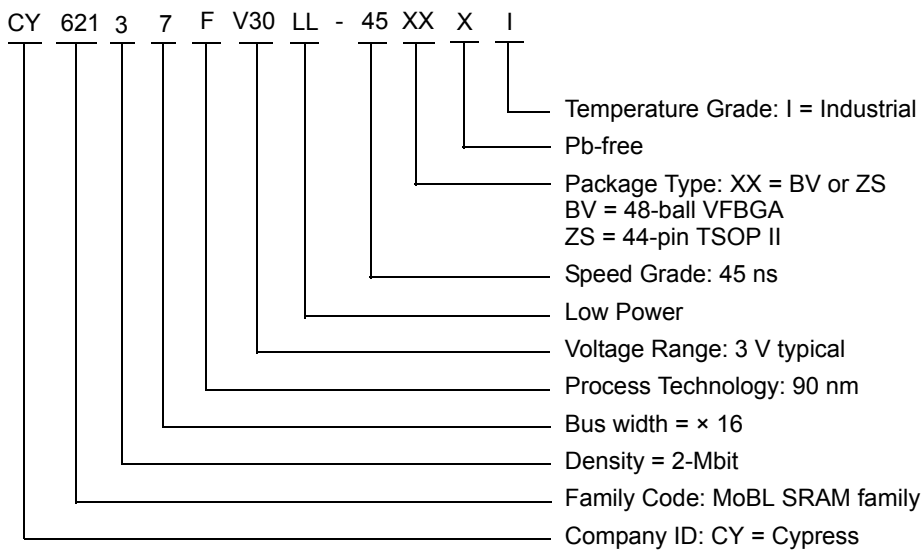
30. The 'X' (Don't care) state for the Chip enable ($\overline{\text{CE}}$) and Byte enables ($\overline{\text{BHE}}$ and $\overline{\text{BLE}}$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62137FV30LL-45BVI	51-85150	48-ball VFBGA	Industrial
	CY62137FV30LL-45BVXI		48-ball VFBGA (Pb-free)	
	CY62137FV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

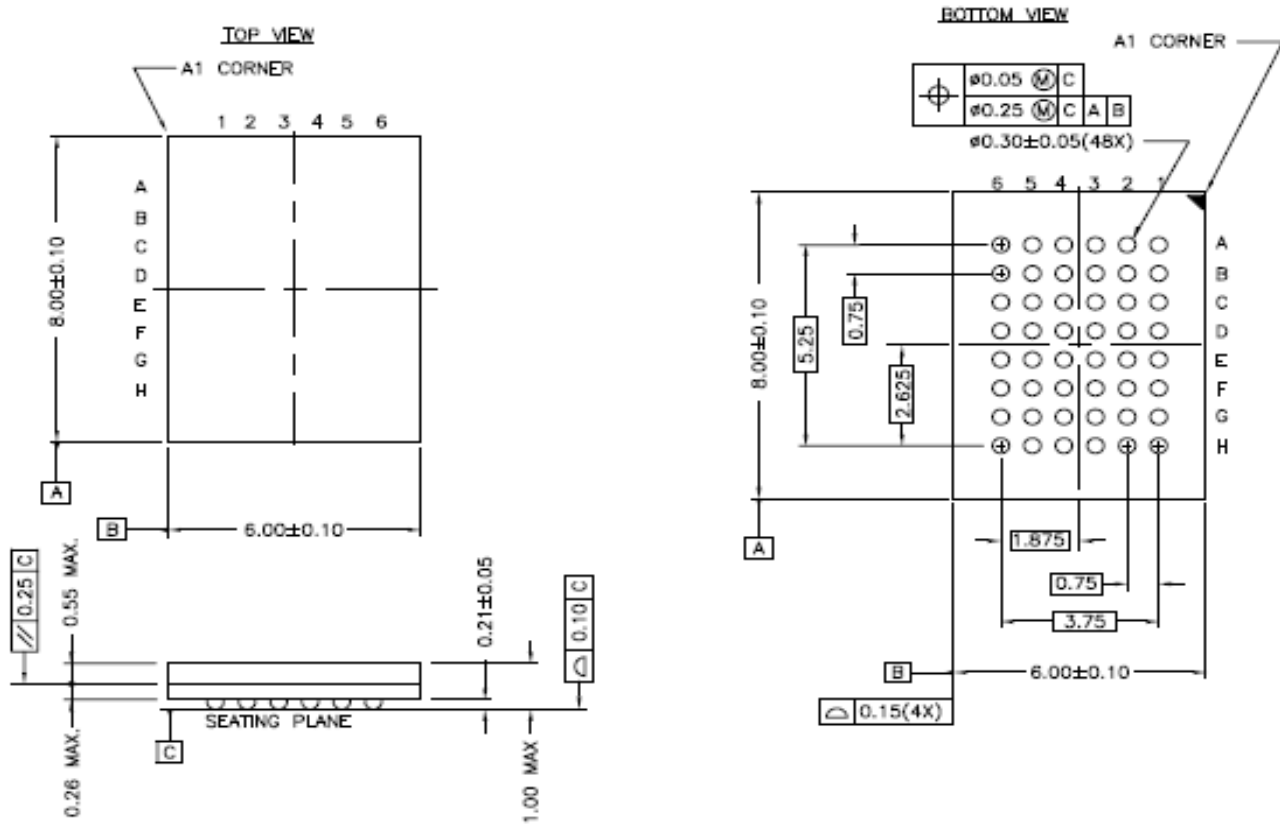
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

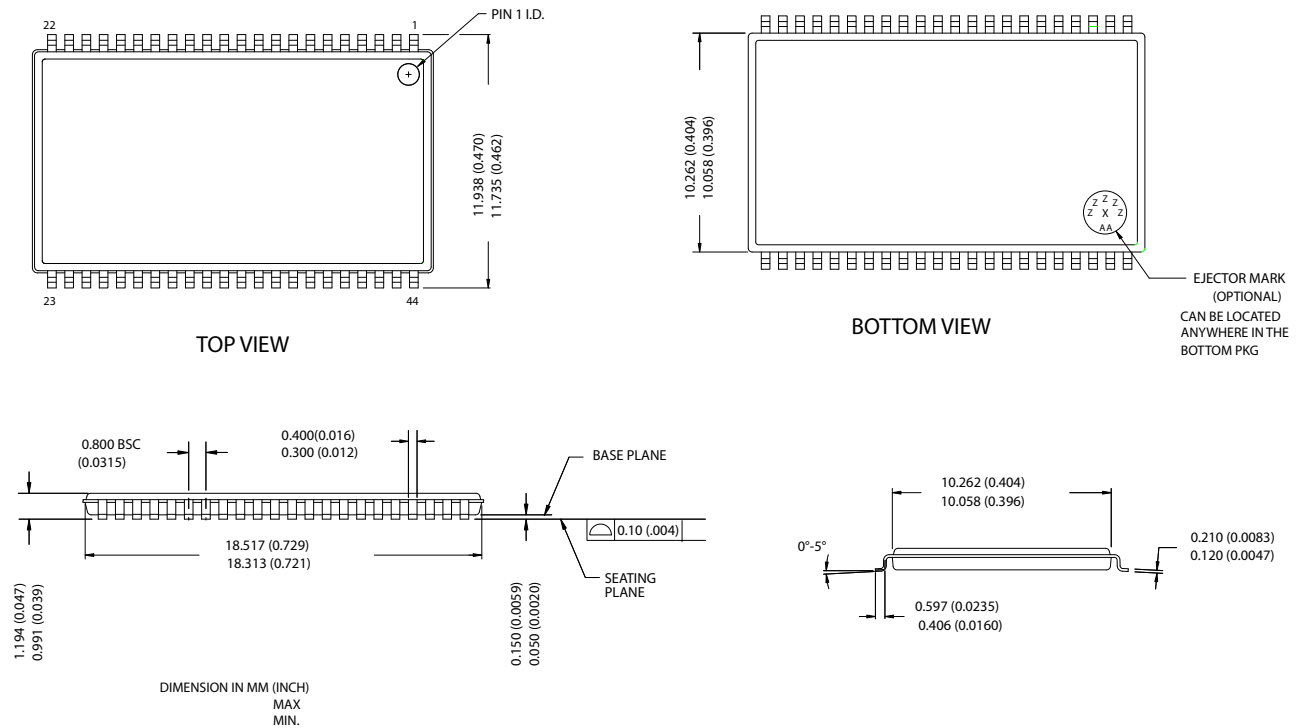
Figure 11. 48-ball VFBGA (6 x 8 x 1.0 mm) BV48/BZ48, 51-85150



51-85150 *F

Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II, 51-85087



Acronyms

Acronym	Description
BLE	byte low enable
BHE	byte high enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
μs	micro seconds
mA	milli Amperes
mm	milli meter
ns	nano seconds
%	percent
pF	pico Farads
Ω	ohms
V	Volts
W	Watts

Document History Page

Document Title: CY62137FV30 MoBL [®] , 2-Mbit (128 K × 16) Static RAM				
Document Number: 001-07141				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	449438	See ECN	NXR	New datasheet
*A	464509	See ECN	NXR	Changed the I _{SB2(typ)} value from 1.0 μA to 0.5 μA Changed the I _{SB2(max)} value from 4 μA to 2.5 μA Changed the I _{CC(typ)} value from 2 mA to 1.6 mA and I _{CC(max)} value from 2.5 mA to 2.25 mA for f=1 MHz test condition Changed the I _{CC(typ)} value from 15 mA to 13 mA and I _{CC(max)} value from 20 mA to 18 mA for f=1 MHz test condition Changed the I _{CDDR(typ)} value from 0.7 μA to 0.5 μA and I _{CDDR(max)} value from 3 μA to 2.5 μA
*B	566724	See ECN	NXR	Converted from preliminary to final Changed the I _{CC(max)} value from 2.25 mA to 2.5 mA for test condition f=1 MHz Changed the I _{SB2(typ)} value from 0.5 μA to 1 μA Changed the I _{SB2(max)} value from 2.5 μA to 5 μA Changed the I _{CDDR(typ)} value from 0.5 μA to 1 μA and I _{CDDR(max)} value from 2.5 μA to 4 μA
*C	869500	See ECN	VKN	Added Automotive-A and Automotive-E information Updated Ordering Information Table Added footnote 13 related to t _{ACE}
*D	901800	See ECN	VKN	Added footnote 9 related to I _{SB2} and I _{CDDR} Made footnote 14 applicable to AC parameters from t _{ACE}
*E	1371124	See ECN	VKN/AESA	Converted Automotive information from preliminary to final Changed I _{Ix} min spec from -1 μA to -4 μA and I _{Ix} max spec from +1 μA to +4 μA Changed I _{OZ} min spec from -1 μA to -4 μA and I _{OZ} max spec from +1 μA to +4 μA
*F	1875374	See ECN	VKN/AESA	Added -45BVI part in the Ordering Information table
*G	2943752	06/03/2010	VKN	Added Contents Added footnote related to Chip enable and Byte enables in Truth Table Updated Package Diagrams Updated links in Sales, Solutions, and Legal Information
*H	3055031	10/12/10	RAME	Added Acronyms and Units of Measure Table Converted all table notes into footnotes. Updated Electrical Characteristics , Switching Characteristics table, and Data Retention Characteristics table Updated Package Diagrams from 51-85150 *E to *F Changed I _{SB1} /I _{SB2} /I _{CDDR} test conditions to reflect byte power down feature
*I	3123998	01/03/2011	RAME	Separated Automotive and Industrial parts from datasheet Removed Automotive info
*J	3285093	06/16/2011	RAME	Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated in new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.