National Semiconductor

MICROCIRCUIT DATA SHEET

MJ54AC125-X-RH REV 0B0

Original Creation Date: 06/17/03
Last Update Date: 07/15/03
Last Major Revision Date:

Quad Buffer With TRI-STATE Outputs (ALSO AVAILABLE GUARANTEED TO 100 krd(Si) TESTED TO MIL-STD-883, METHOD 1019)

General Description

The 54AC125 contains four independent non-inverting buffers with TRI-STATE outputs.

Industry Part Number

54AC125

Prime Die

Z125

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

JM54AC125B2A
JM54AC125B2A-RH
JM54AC125BCA
JM54AC125BCA-RH
JM54AC125BDA
JM54AC125BDA-RH
JM54AC125S2A-RH
JM54AC125SCA-RH
JM54AC125SDA-RH

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

CONTROLLING DOCUMENT:	
JM54AC125B2A	5962-9325301B2A
JM54AC125B2A-RH	5962R9325301B2A
JM54AC125BCA	5962-9325301BCA
JM54AC125BCA-RH	5962R9325301BCA
JM54AC125BDA	5962-9325301BDA
JM54AC125BDA-RH	5962R9325301BDA
JM54AC125SCA-RH	5962R9325301SCA
JM54AC125SDA-RH	5962R9325301SDA
JM54AC125S2A-RH	5962R9325301S2A

(Absolute Maximum Ratings)

(Note 1, 2, 3)

DC Supply Voltage (Vcc)	-0.5V to +6.0V
DC Input Diode Current (Iik)	
Vi = -0.5V	-20 mA
Vi = Vcc +0.5V	+20 mA
DC Input Voltage (Vi)	-0.5V to Vcc +0.5V
DC Output Diode Current (Iok)	
Vo = -0.5V	-20 mA
Vo = Vcc +0.5V	+20 mA
DC Output Voltage (Vo)	-0.5V to Vcc +0.5V
DC Output Source or Sink Current (Io)	±50 mA
DC Vcc or Ground Current per Output Pin (Icc or Ignd) (times the number of outputs)	±50 mA
Storage Temperature (Tstg)	-65 C to +150 C
Junction Temperature (Tj)	+175 C
Maximum Power Dissipation (Pd)	500 mW
Lead Temperature (Soldering, 10 seconds)	+300 C
Thermal Resistance Junction-to-case (ThetaJC)	See MIL-M-1835

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specification should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation FACT TM circuits outside databook specifications.
Note 2: Unless otherwise noted, all voltages are referenced to Gnd.
Note 3: The limits for the parameters specified herein shall apply over the full specified Vcc range and case temperature range of -55 C to +125 C.

Recommended Operating Conditions

(Note 1, 2, 3)

DC Supply Voltage (Vcc)	3.0V to 5.5V
DC Input Voltage (Vi)	0V to Vcc
DC Output Voltage (Vo)	0V to Vcc
DC Maximum Low Level Input Voltage (Vil)	0.90V at Vcc = 3.0V 1.08V at Vcc = 3.6V 1.35V at Vcc = 4.5V 1.65V at Vcc = 5.5V
DC Minimum High Level Input Voltage (Vih)	2.10V at Vcc = 3.0V 2.52V at Vcc = 3.6V 3.15V at Vcc = 4.5V 3.85V at Vcc = 5.5V
Operating Temperature (Ta)	

Recommended Operating Conditions (Continued)

(Note 1, 2, 3)

Operating Temperature (Ta)	-55 C to +125 C
Minimum Input Edge Rate (Delta V/Delta t) AC Devices Vin From 30% to 70% of Vcc Vcc @ 3.0V, 4.5V, 5.5V	125 mV/ns
DC Maximum Low Level Output Current (Iol)	12mA at Vcc = 3.0V and 3.6V 24mA at Vcc = 4.5V and 5.5V
DC Maximum High Level Output Current (Ioh)	-12mA at Vcc = 3.0V and 3.6V -24mA at Vcc = 4.5V and 5.5V

Note 0: The limits for the parameters specified herein shall apply over the full specified Vcc range and case temperature range of -55 C to +125 C.
Note 1: Unless otherwise noted, all voltages are referenced to Gnd.
Note 3: Operation from 2.0V to 3.0V dc is provided for compatibility with data retention and battery back up systems. Data retention implies no input transitions and no stored data loss with the following conditions: Vih $\geq$70 percent of Vcc, Vil $\leq$30 percent of Vcc, Voh $\geq$70 percent of Vcc at -20uA, Vol $\leq$30 percent of Vcc at 20uA.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 3.0V to 5.5V, Temp. Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 3 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	High Level Input Current	VCC=5.5V, VM=5.5V	1, 2	INPUT		0.1	uA	1
			1, 2	INPUT		1.0	uA	2
IIL	Low Level Input Current	VCC=5.5V, VM=0.0V	1, 2	INPUT		-0.1	uA	1
			1, 2	INPUT		-1.0	uA	2
VOL	Low Level Output Voltage	VCC=3.0V, VIH=2.1V, VIL=0.9V, IOL=50.0uA	1, 2	OUTPUT		0.10	V	1, 2, 3
		VCC=4.5V, VIH=3.15V, VIL=1.35V, IOL=50.0uA	1, 2	OUTPUT		0.10	V	1, 2, 3
		VCC=5.5V, VIH=3.85V, VIL=1.65V, IOL=50.0uA	1, 2	OUTPUT		0.10	V	1, 2, 3
		VCC=3.0V, VIH=2.1V, VIL=0.9V, IOL=12.0mA	1, 2	OUTPUT		0.40	V	1, 3
			1, 2	OUTPUT		0.50	V	2
		VCC=4.5V, VIH=3.15V, VIL=1.35V, IOL=24.0mA	1, 2	OUTPUT		0.40	V	1, 3
			1, 2	OUTPUT		0.50	V	2
		VCC=5.5V, VIH=3.85V, VIL=1.65V, IOL=24.0mA	1, 2	OUTPUT		0.40	V	1, 3
			1, 2	OUTPUT		0.50	V	2
VIOL	Dynamic Output Current LOW	VCC=5.5V, VIH=3.85V, VIL=1.65V, IOL=50.0mA	1, 2, 5	OUTPUT		1.65	V	1, 2, 3
VOH	High Level Output Voltage	VCC=3.0V, VIH=2.1V, VIL=0.9V, IOH=-50uA	1, 2	OUTPUT	2.90		V	1, 2, 3
		VCC=4.5V, VIH=3.15V, VIL=1.35V, IOH=-50.0uA	1, 2	OUTPUT	4.40		V	1, 2, 3
		VCC=5.5V, VIH=3.85V, VIL=1.65V, IOH=-50.0uA	1, 2	OUTPUT	5.40		V	1, 2, 3
		VCC=3.0V, VIH=2.1V, VIL=0.9V, IOH=-12mA	1, 2	OUTPUT	2.40		V	1, 2, 3
		VCC=4.5V, VIH=3.15V, VIL=1.35V, IOH=-24.0mA	1, 2	OUTPUT	3.70		V	1, 2, 3
		VCC=5.5V, VIH=3.85V, VIL=1.65V, IOH=-24.0mA	1, 2	OUTPUT	4.70		V	1, 2, 3
VIOH	Dynamic Output Current HIGH	VCC=5.5V, VIH=3.85V, VIL=1.65V, IOH=-50.0mA	1, 2, 5	OUTPUT	3.85		V	1, 2, 3
IOZH	Maximum TRI-STATE Leakage Current HIGH	VCC=5.5V, VM=5.5V, VINL=0.0V, VIH=3.85V	1, 2	OUTPUT		0.5	uA	1
			1, 2	OUTPUT		10.0	uA	2

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 3.0V to 5.5V, Temp. Range: -55C to 125C. NOTE: -55C TEMPERATURE, SUBGROUP 3 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IOZL	Maximum TRI-STATE Leakage Current LOW	VCC=5.5V, VM=0.0V, VINH=5.5V, VIH=3.85V	1, 2	OUT		-0.5	uA	1
			1, 2	OUT		-10.0	uA	2
ICCH	Quiescent Supply Current Output HIGH	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		90.0	nA	1
			1, 2	VCC		40	uA	2
ICCL	Quiescent Supply Current Output LOW	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		90.0	nA	1
			1, 2	VCC		40	uA	2
ICCZ	Quiescent Supply Current Output TRI-STATE	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 2	VCC		90.0	nA	1
			1, 2	VCC		40	uA	2
VIC+	Positive Input Clamp Voltage	VCC=GND, IIN=1mA		INPUT	0.4	1.5	V	1
VIC-	Negative Input Clamp Voltage	VCC=OPEN, IIN=-1mA		INPUT	-0.4	-1.5	V	1
ICC(0/V1)	Latch-Up Input/Output Over-Voltage	VCC=5.5V, tw≥100us, tcool≥tw, 5us≤tr≤5ms, 5us≤tf≤5ms, Vtest=6.0V, VCCQ=5.5V, Vover=10.5V				200	mA	2
ICC(0/I1+)	Latch-Up Input/Output Positive Over-Current	VCC=5.5V, tw≥100us, tcool≥tw, 5us≤tr≤5ms, 5us≤tf≤5ms, Vtest=6.0V, VCCQ=5.5V, Itrigger=+120mA				200	mA	2
ICC(0/I1-)	Latch-Up Input/Output Negative Over-Current	VCC=5.5V, tw≥100us, tcool≥tw, 5us≤tr≤5ms, 5us≤tf≤5ms, Vtest=6.0V, VCCQ=5.5V, Itrigger=-120mA				200	mA	2
ICC(0/V2)	Latch-Up Supply Over-Voltage	VCC=5.5V, tw≥100us, tcool≥tw, 5us≤tr≤5ms, 5us≤tf≤5ms, Vtest=6.0V, VCCQ=5.5V, Vover=9.0V				100	mA	2
	Truth Table Test Output Voltage	VCC=3.0V, VIH=2.1V, VIL=0.9V, Verify output Vo			<1.5	≥1.5	V	7, 8
		VCC=4.5V, VIH=3.15V, VIL=1.35V, Verify output Vo			<2.5	≥2.5	V	7, 8
CIN	Input Capacitance	VCC=GND, TC=+25 C		INPUT		10.0	pF	4
COUT	Output Capacitance	VCC=5.5V, TC=+25 C		OUTPUT		15.0	pF	4
CPD	Power Dissipation Capacitance	VCC=5.0V, TC=+25 C				70.0	pF	4
VGBL	Low Level Ground Bounce Noise	VCC=4.5V, VLD=2.5V, IOL=+24mA				1500	mV	4
VGBH	High Level Ground Bounce Noise	VCC=4.5V, VLD=2.5V, IOL=-24mA				1500	mV	4

Electrical Characteristics

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS TRISE=3ns & TFALL=3ns. NOTE: -55C TEMPERATURE, SUBGROUP 11 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH(1)	Propagation Delay	VCC=4.5V	3, 4, 6	Bn to On	1.5	7.0	ns	9, 11
			3, 4, 6	Bn to On	1.5	8.5	ns	10
tpHL(1)	Propagation Delay	VCC=4.5V	3, 4, 6	Bn to On	1.5	7.0	ns	9, 11
			3, 4, 6	Bn to On	1.5	8.5	ns	10
tpZH(1)	Output Enable Time	VCC=4.5V	3, 4, 6	$\overline{An}$ to On	1.5	8.0	ns	9, 11
			3, 4, 6	$\overline{An}$ to On	1.5	8.5	ns	10
tpZL(1)	Output Enable Time	VCC=4.5V	3, 4, 6	$\overline{An}$ to On	1.5	8.0	ns	9, 11
			3, 4, 6	$\overline{An}$ to On	1.5	8.5	ns	10
tpHZ(1)	Output Disable Time	VCC=4.5V	3, 4, 6	$\overline{An}$ to On	1.5	9.0	ns	9, 11
			3, 4, 6	$\overline{An}$ to On	1.5	9.5	ns	10
tpLZ(1)	Output Disable Time	VCC=4.5V	3, 4, 6	$\overline{An}$ to On	1.5	9.0	ns	9, 11
			3, 4, 6	$\overline{An}$ to On	1.5	9.5	ns	10
tpLH(2)	Propagation Delay	VCC=3.0V	3, 4	Bn to On	1.0	9.0	ns	9, 11
			3, 4	Bn to On	1.0	10.0	ns	10
tpHL(2)	Propagation Delay	VCC=3.0V	3, 4	Bn to On	1.0	9.0	ns	9, 11
			3, 4	Bn to On	1.0	10.0	ns	10
tpZH(2)	Output Enable Time	VCC=3.0V	3, 4	$\overline{An}$ to On	1.0	10.0	ns	9, 11
			3, 4	$\overline{An}$ to On	1.0	11.0	ns	10
tpZL(2)	Output Enable Time	VCC=3.0V	3, 4	$\overline{An}$ to On	1.0	10.0	ns	9, 11
			3, 4	$\overline{An}$ to On	1.0	11.0	ns	10

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pf, RL=500 OHMS TRISE=3ns & TFALL=3ns. NOTE: -55C TEMPERATURE, SUBGROUP 11 IS GUARANTEED BUT NOT TESTED.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpHZ(2)	Output Disable Time	VCC=3.0V	3, 4	$\overline{An}$ to On	1.0	10.0	ns	9, 11
			3, 4	$\overline{An}$ to On	1.0	11.0	ns	10
tpLZ(2)	Output Disable Time	VCC=3.0V	3, 4	$\overline{An}$ to On	1.0	10.0	ns	9, 11
			3, 4	$\overline{An}$ to On	1.0	11.0	ns	10

Electrical Characteristics

AC/DC PARAMETERS: POST RADIATION LIMITS (SEE NOTE 7)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: The 100 krd(Si) DOSE LEVEL INCLUDES A POST IRRADIATION 168 HOUR, 25 Deg C BIASED ANNEAL

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ICCH	Quiescent Supply Current Output HIGH	VCC=5.5V, VINH=5.5V, VINL=0.0V (M = 3k RAD)	7	VCC		15.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (D = 10k RAD)	7	VCC		100.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (R = 100k RAD)	7	VCC		700.0	uA	1
ICCL	Quiescent Supply Current Output LOW	VCC=5.5V, VINH=5.5V, VINL=0.0V (M = 3k RAD)	7	VCC		15.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (D = 10k RAD)	7	VCC		100.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (R = 100k RAD)	7	VCC		700.0	uA	1
ICCZ	Quiescent Supply Current Output TRI-STATE	VCC=5.5V, VINH=5.5V, VINL=0.0V (M = 3k RAD)	7	VCC		15.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (D = 10k RAD)	7	VCC		100.0	uA	1
		VCC=5.5V, VINH=5.5V, VINL=0.0V (R = 100k RAD)	7	VCC		700.0	uA	1
IOZH	Maximum TRI-STATE Leakage Current HIGH	VCC=5.5V, VM=5.5V, VINL=0.0V, VIH-3.85V (M = 3k RAD)	7	OUTPUT		25.0	uA	1
		VCC=5.5V, VM=5.5V, VINL=0.0V, VIH-3.85V (D = 10k RAD)	7	OUTPUT		25.0	uA	1
		VCC=5.5V, VM=5.5V, VINL=0.0V, VIH-3.85V (R = 100k RAD)	7	OUTPUT		25.0	uA	1
IOZL	Maximum TRI-STATE Leakage Current LOW	VCC=5.5V, VM=0.0V, VINH=5.5V, VIH=3.85V (M = 3k RAD)	7	OUTPUT		-25.0	uA	1
		VCC=5.5V, VM=0.0V, VINH=5.5V, VIH=3.85V (D = 10k RAD)	7	OUTPUT		-25.0	uA	1
		VCC=5.5V, VM=0.0V, VINH=5.5V, VIH=3.85V (R = 100k RAD)	7	OUTPUT		-25.0	uA	1

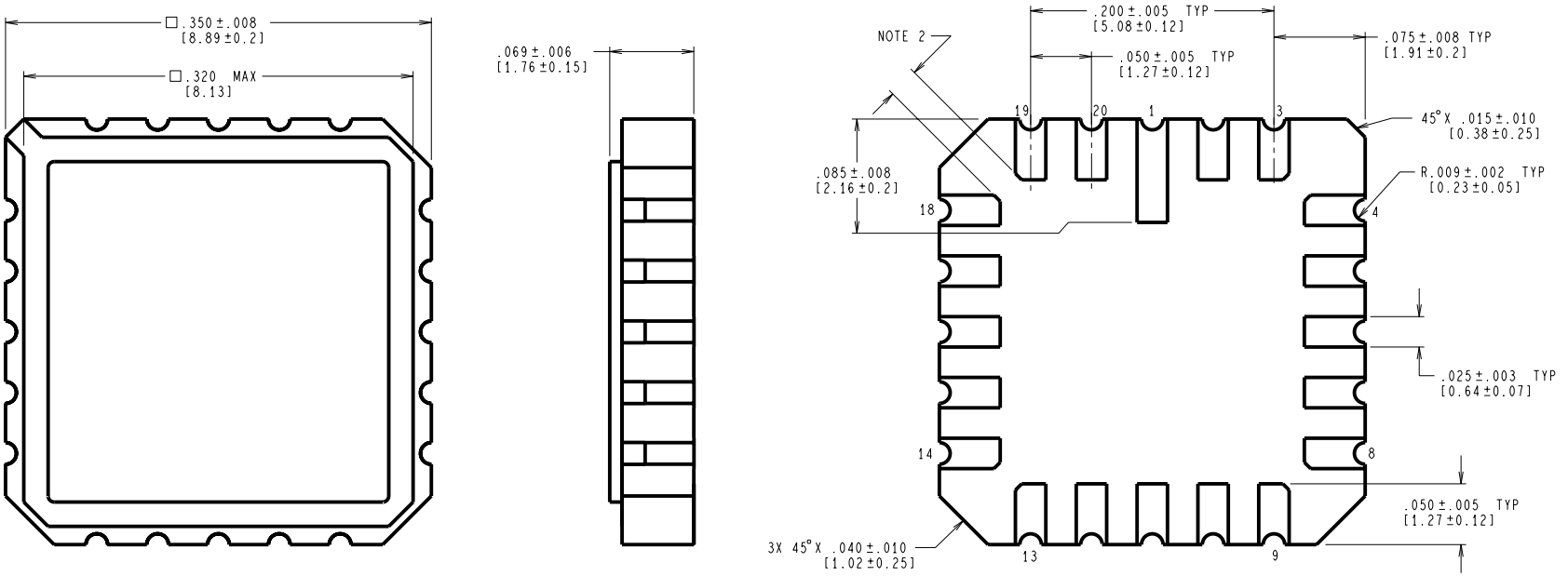
Note 1: SCREEN TESTED 100% ON EACH DEVICE AT +25C & +125C TEMPERATURE, SUBGROUPS 1, 2, 7, & 8.
Note 2: SAMPLE TESTED (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A1, 2, 7, & 8.
Note 3: SCREEN TESTED 100% ON EACH DEVICE AT +25C TEMPERATURE ONLY, SUBGROUP A9.
Note 4: SAMPLE TEST (METHOD 5005, TABLE 1) ON EACH MFG. LOT AT +25C & +125C TEMPERATURE, SUBGROUPS A9 & 10.
Note 5: TRANSMISSION LINE DRIVING TEST, GUARDBAND LIMITS SET FOR +25C, 2 MSEC DURATION MAX.
Note 6: +25C & +125C MIN LIMITS GUARANTEED FOR 5.5V BY GUARDBANDING 4.5V MIN. LIMITS.
Note 7: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics subgroups 1, 7, 9 except if listed in the Post Radiation Limits Table (IF APPLICABLE). Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
W14BRN	CERPACK (W), 14 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

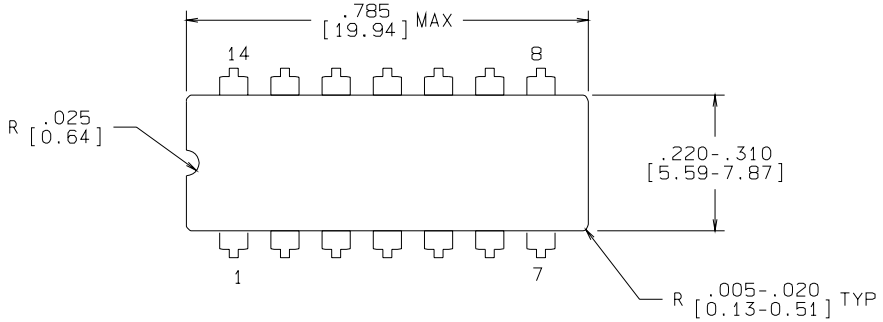
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

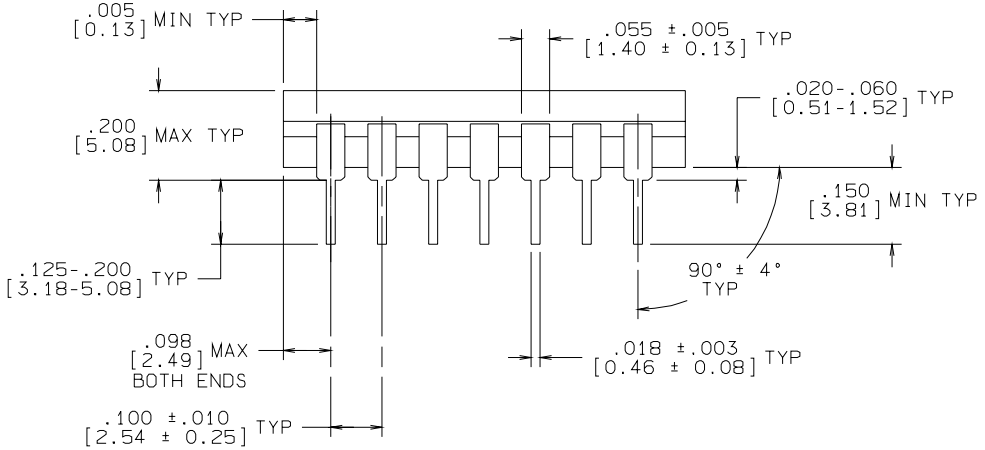
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

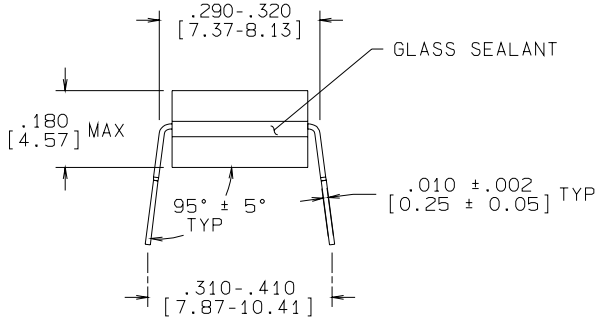
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

INCH
[MM]

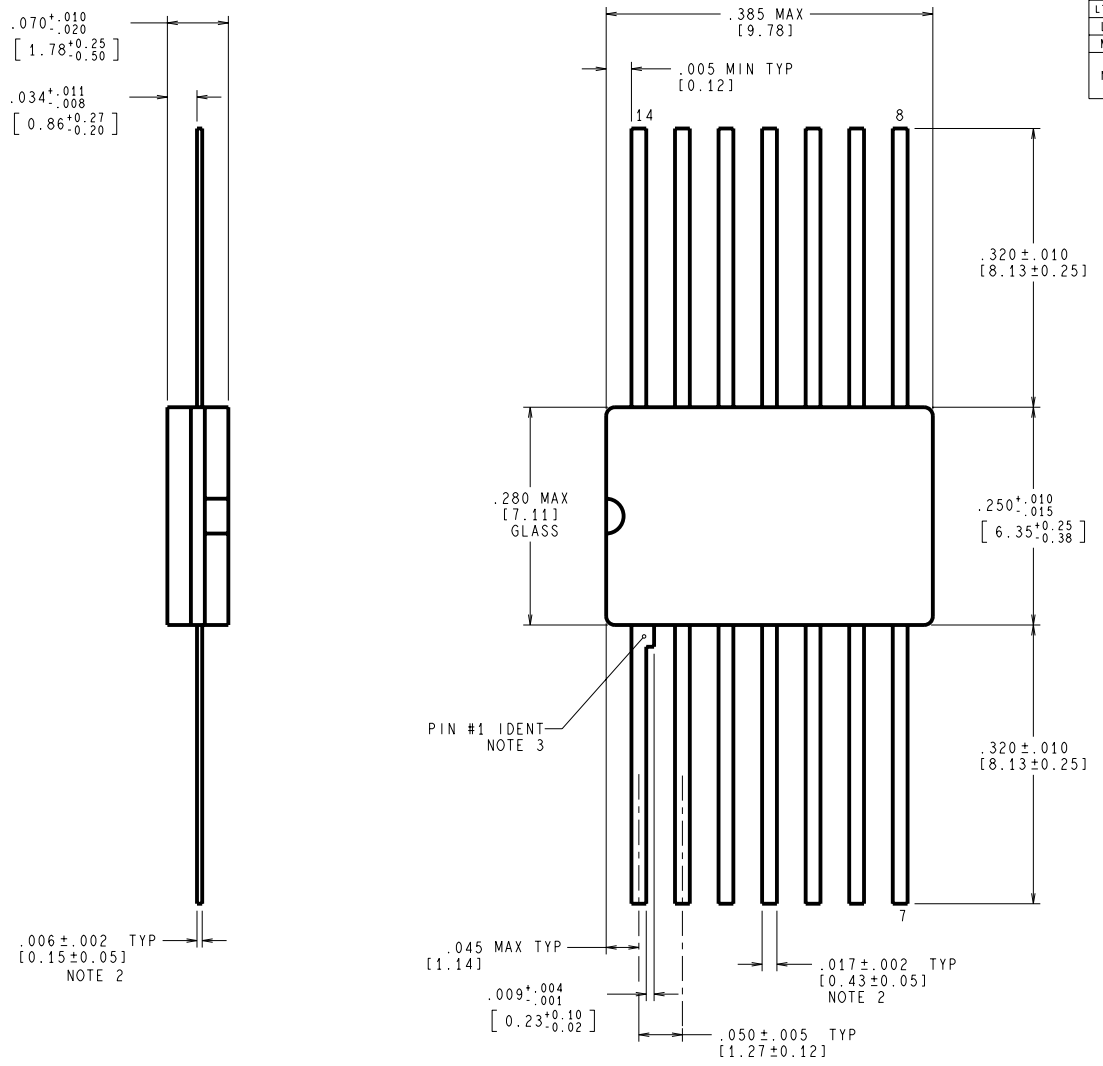
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE AND REDRAW PER NEW STANDARD.	10513	07/26/94	DEG/AEP
M	.017±.002 WAS .017±.020.	10655	10/21/94	DEG/CD
N	L/F THKS .006±.002 WAS .005±.001; UPDATE NOTES 1 & 2; REMOVE NOTE 4; UPDATE MILAERO STAMP; DUAL DIM'S WERE INCHES ONLY.	11005	06/08/95	MS/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-I-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES/ 0.08 MILLIMETERS AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN D.E.Grady	07/26/94
DFTG. CHK.	
ENGR. CHK.	

PROJECTION INCH [MM]

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W14B	N

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0001759	07/15/03	Rose Malone	Initial MDS Release: MJ54AC125-X-RH, Rev. 0A0
0B0	M0004176	07/15/03	Rose Malone	Update MDS: MJ54AC125-X-RH, Rev. 0A0 to MJ54AC125-X-RH, Rev. 0B0. Corrected typo in Features Section, correction to SMD number.