

54ABT374

Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 54ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 48 mA, source capability of 24 mA

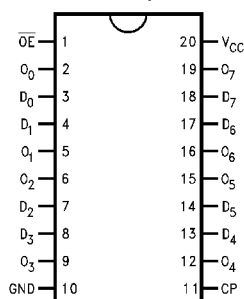
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9314901

Ordering Code

Military	Package Number	Package Description
54ABT374J/883	J20A	20-Lead Ceramic Dual-In-Line
54ABT374W/883	W20A	20-Lead Cerpack
54ABT374E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

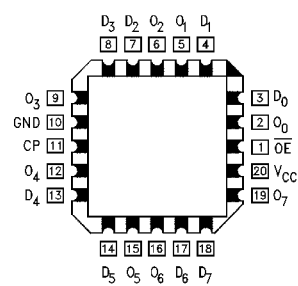
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100207-1

Pin Assignment for LCC



DS100207-2

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54ABT374 Octal D-Type Flip-Flop with TRI-STATE Outputs

Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)
O ₀ –O ₇	TRI-STATE Outputs

Functional Description

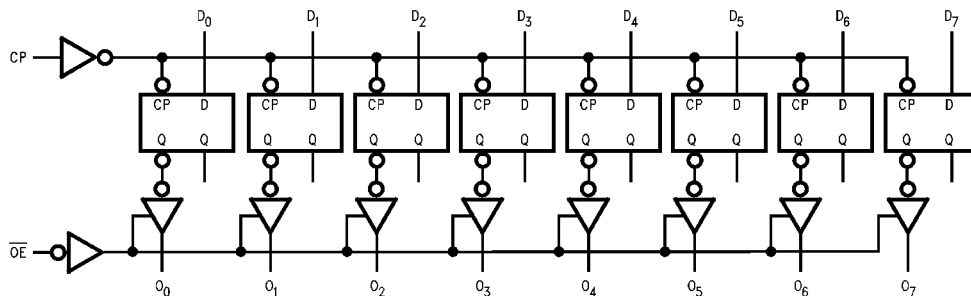
The ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs are in a high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
\overline{OE}	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



DS100207-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current:

\overline{OE} Pin (Across Comm Operating Range)	-150 mA
Other Pins	-500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	ABT374			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA
		54ABT	2.0		V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = 2.7V (Note 4)
			5		μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current		-5		μA	Max	V _{IN} = 0.5V (Note 4)
			-5		μA	Max	V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current		50		μA	0 - 5.5V	V _{OUT} = 2.7V; \overline{OE} = 2.0V
I _{OZL}	Output Leakage Current		-50		μA	0 - 5.5V	V _{OUT} = 0.5V; \overline{OE} = 2.0V
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V; All Others V _{CC} or GND
I _{OCH}	Power Supply Current		50		μA	Max	All Outputs HIGH
I _{OCL}	Power Supply Current		30		mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current		50		μA	Max	\overline{OE} = V _{CC} ; All Others at V _{CC} or GND
I _{OCT}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA		V _I = V _{CC} - 2.1V
		Outputs TRI-STATE	2.5		mA	Max	Enable Input V _I = V _{CC} - 2.1V
		Outputs TRI-STATE	2.5		mA	Max	Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter	ABT374			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{CCD}	Dynamic I _{CC} (Note 4) No Load	0.30			mA/ MHz	Max	Outputs Open OE = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		
		Min	Max	
f _{max}	Max Clock Frequency	150		MHz
t _{PLH}	Propagation Delay	1.4	6.6	ns
t _{PHL}	CP to O _n	2.0	7.6	
t _{PZH}	Output Enable Time	0.8	5.7	ns
t _{PZL}		1.5	7.2	
t _{PHZ}	Output Disable Time	1.3	7.2	ns
t _{PLZ}		1.0	7.0	

AC Operating Requirements

Symbol	Parameter	54ABT		Units
		T _A = -55°C to +125°C V _{CC} = 4.5V to 5.5V C _L = 50 pF		
		Min	Max	
t _s (H)	Setup Time, HIGH	2.5		ns
t _s (L)	or LOW D _n to CP	2.5		
t _h (H)	Hold Time, HIGH	2.5		ns
t _h (L)	or LOW D _n to CP	2.5		
t _w (H)	Pulse Width, CP	3.3		ns
t _w (L)	HIGH or LOW	3.3		

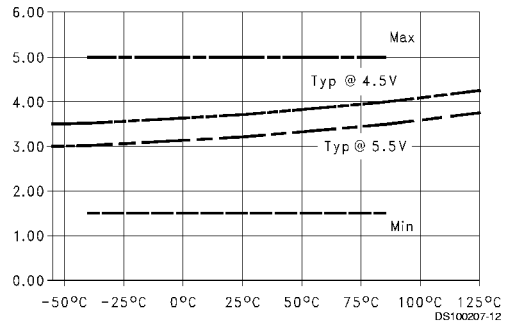
Capacitance

Symbol	Parameter	Typ	Units	Conditions (T _A = 25°C)
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0V
C _{OUT} (Note 5)	Output Capacitance	9.0	pF	V _{CC} = 5.0V

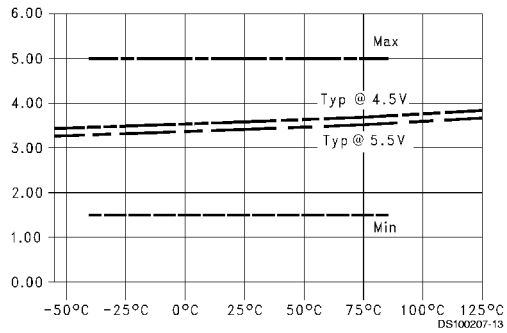
Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Capacitance (Continued)

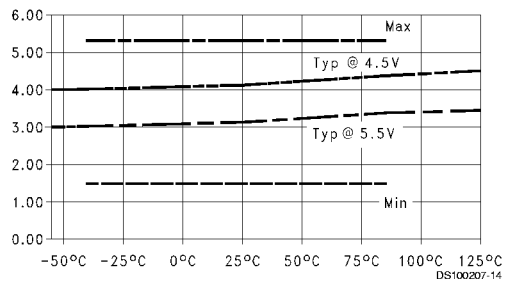
**t_{PLH} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Clock to Output**



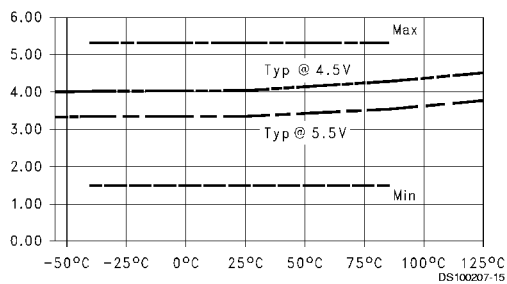
**t_{PHL} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Clock to Output**



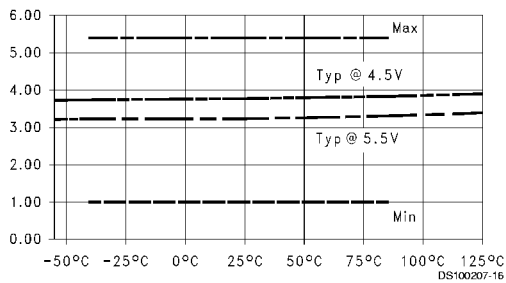
**t_{PZH} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching OE to Output**



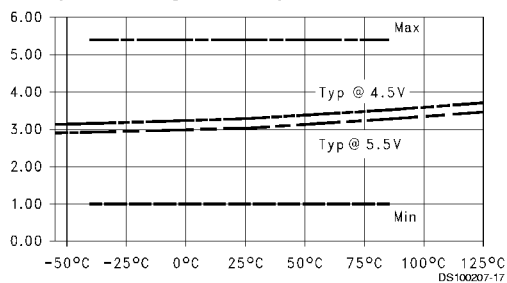
**t_{PZL} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching OE to Output**



**t_{PHZ} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching OE to Output**



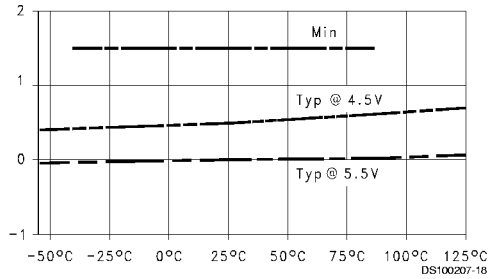
**t_{PLZ} vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching OE to Output**



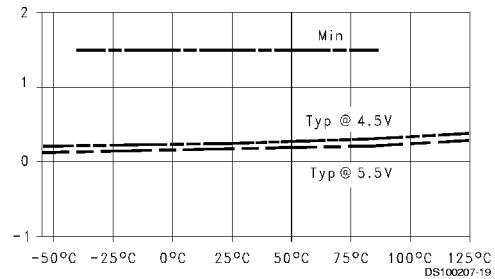
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

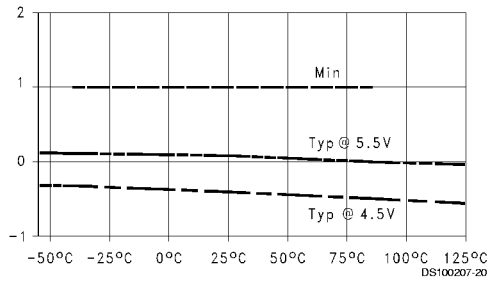
**t_{SET} LOW vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Data to Clock**



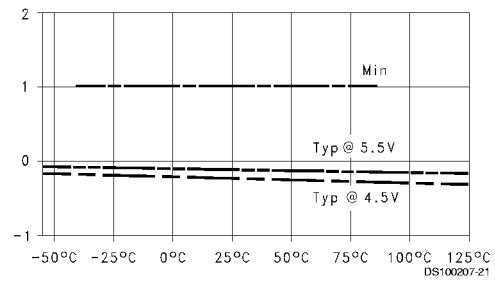
**t_{SET} HIGH vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Data to Clock**



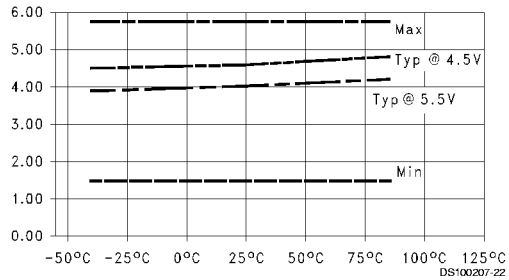
**t_{HOLD} HIGH vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Data to Clock**



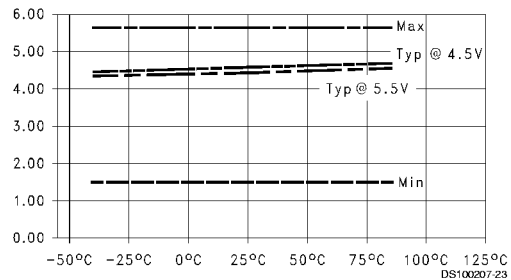
**t_{HOLD} LOW vs Temperature (T_A) $C_L = 50$ pF,
1 Output Switching Data to Clock**



**t_{PLH} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching Clock to Output**



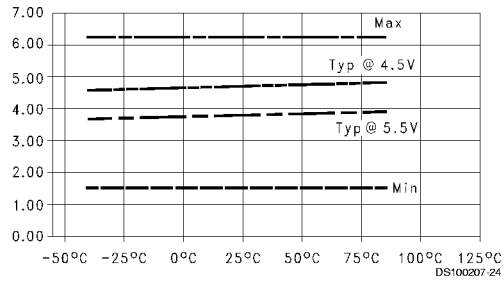
**t_{PHL} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching Clock to Output**



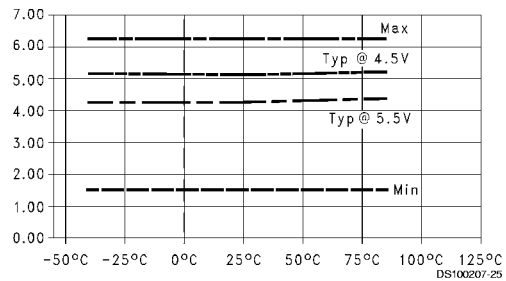
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Capacitance (Continued)

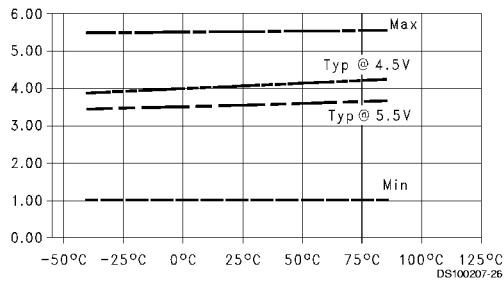
**t_{PZH} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching OE to Output**



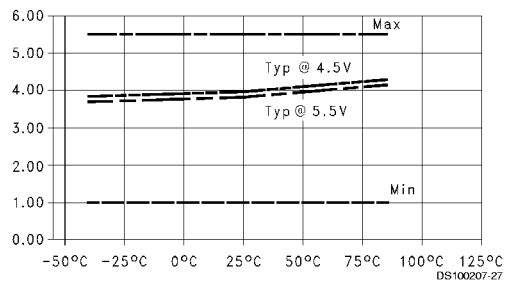
**t_{PZL} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching OE to Output**



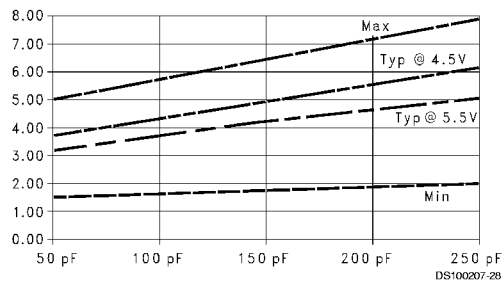
**t_{PHZ} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching OE to Output**



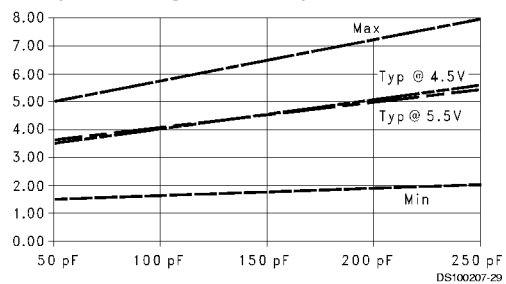
**t_{PLZ} vs Temperature (T_A) $C_L = 50$ pF,
8 Outputs Switching OE to Output**



**t_{PLH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
1 Output Switching Clock to Output**



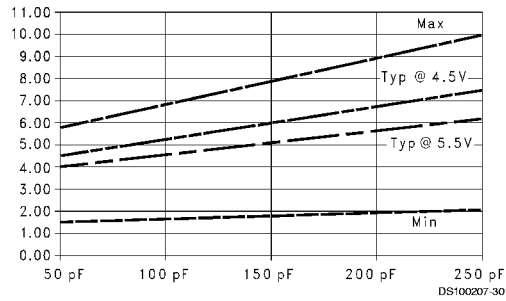
**t_{PHL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
1 Output Switching Clock to Output**



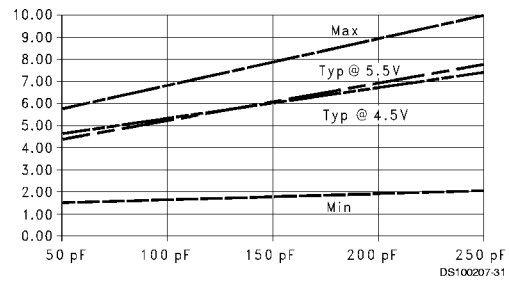
Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

Capacitance (Continued)

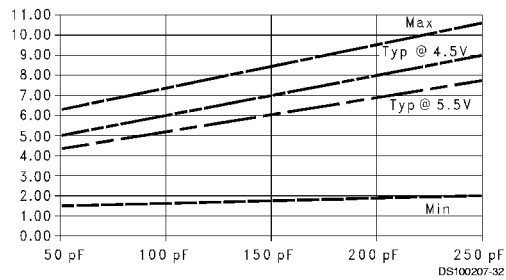
**t_{PLH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching Clock to Output**



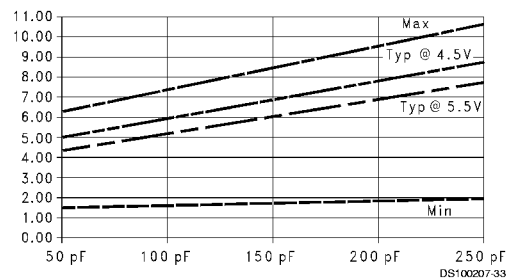
**t_{PHL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching Clock to Output**



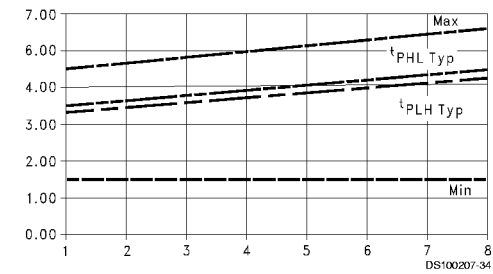
**t_{PZH} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching OE to Output**



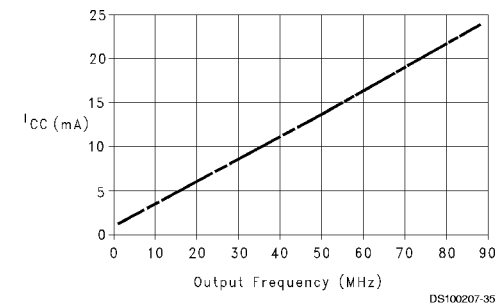
**t_{PZL} vs Load Capacitance $T_A = 25^\circ\text{C}$,
8 Outputs Switching OE to Output**



**t_{PLH} and t_{PHL} vs Number Outputs Switching
 $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$,
Outputs in Phase Clock to Output**

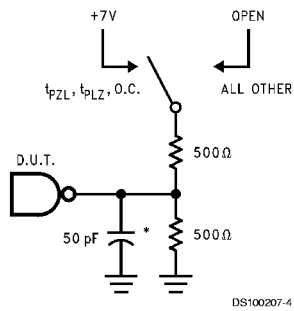


**Typical I_{CC} vs Output Switching Frequency
 $C_L = 0\text{ pF}$, $V_{CC} = V_{IH} = 5.5\text{V}$, 1 Output
Switching at 50% Duty Cycle Clock to Output**



Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

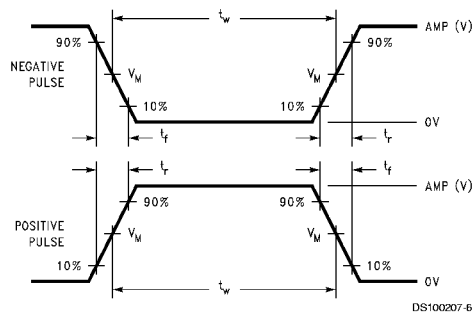


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

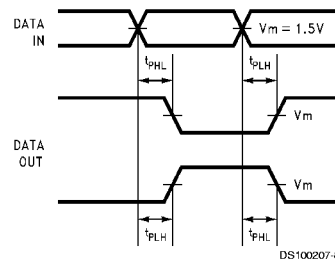


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

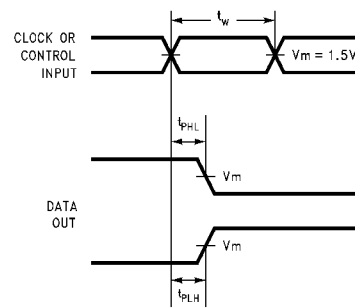


FIGURE 5. Propagation Delay, Pulse Width Waveforms

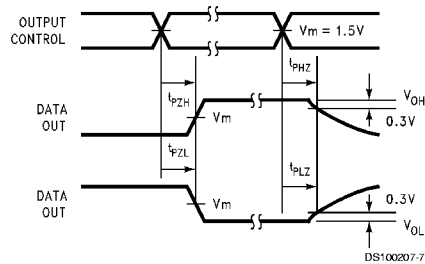


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

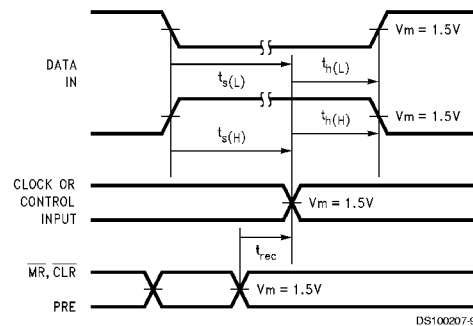
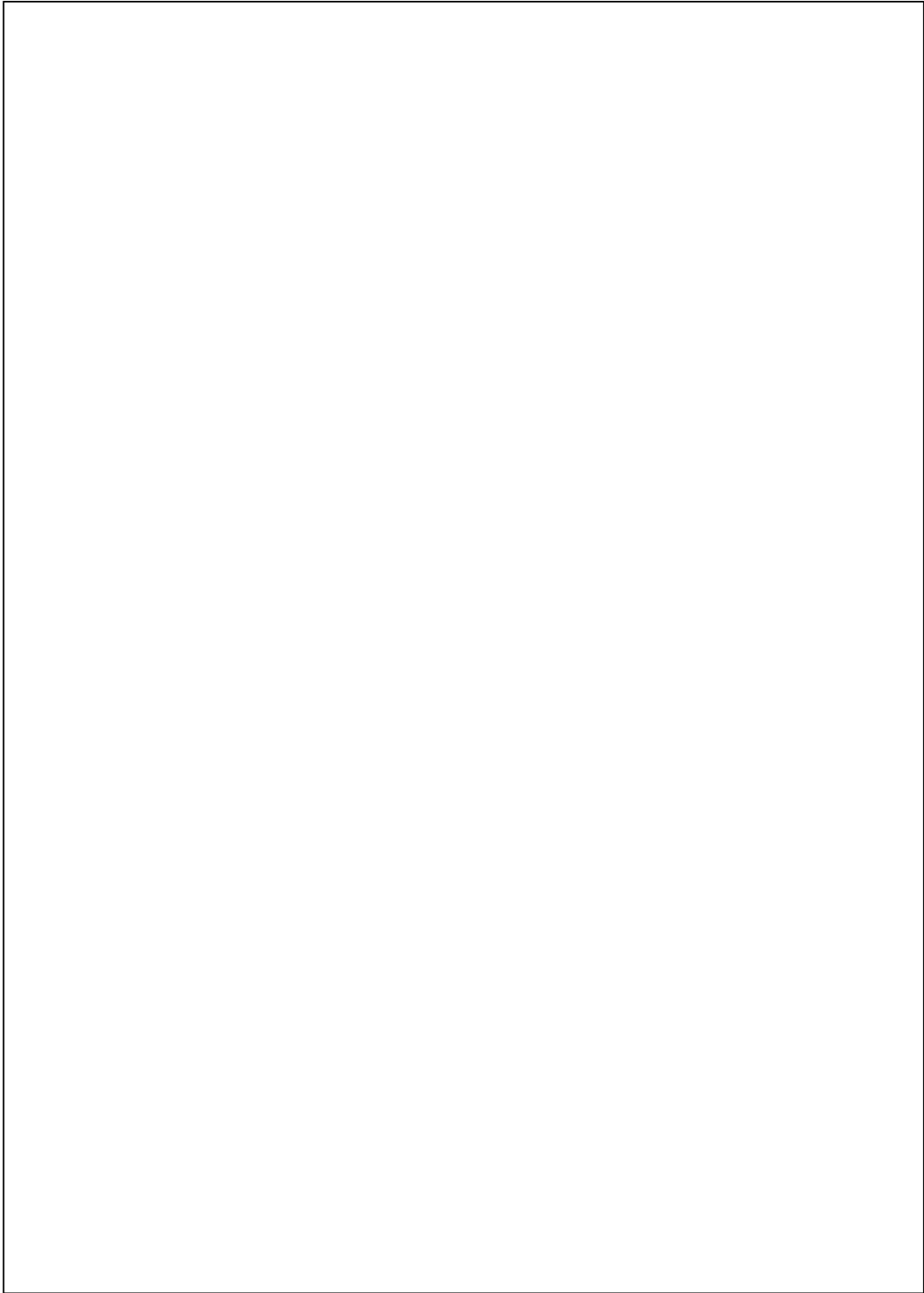
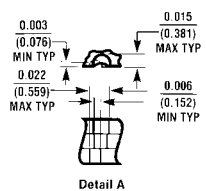
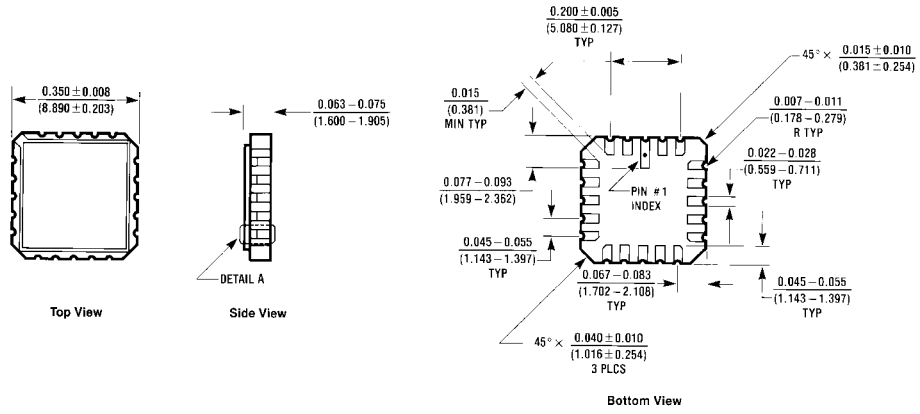


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

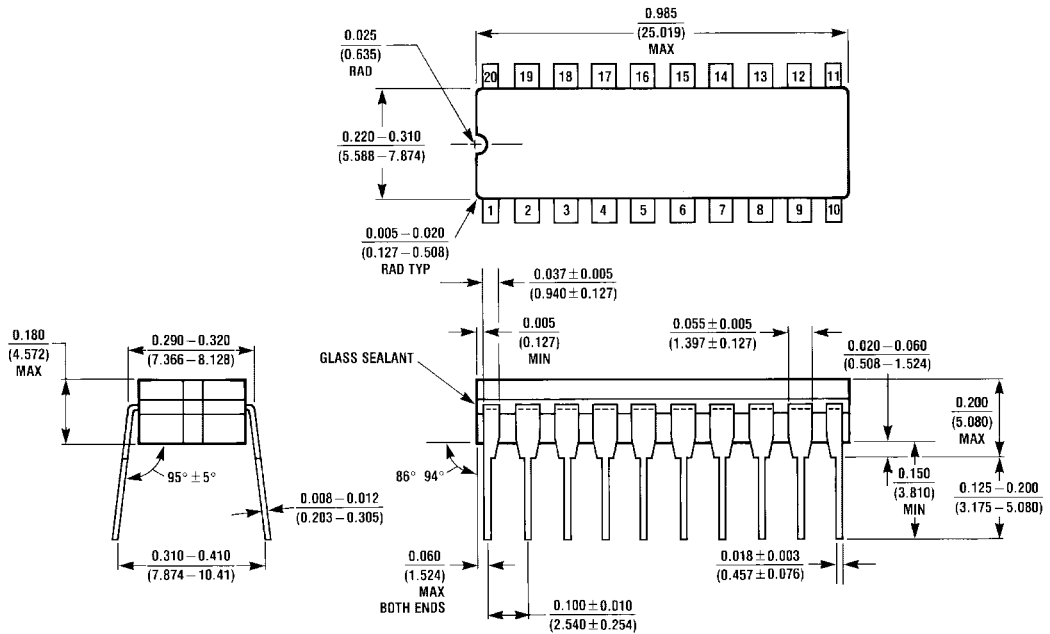


Physical Dimensions inches (millimeters) unless otherwise noted



L20A (REV D)

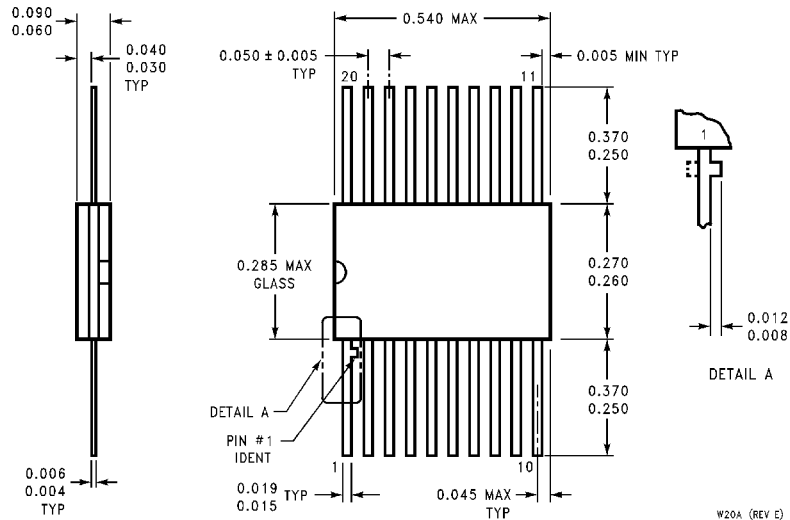
**20-Terminal Ceramic Chip Carrier (L)
 NS Package Number E20A**



J20A (REV M)

**20-Lead Ceramic Dual-In-Line (D)
 NS Package Number J20A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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