

## Dual Power Distribution Controller

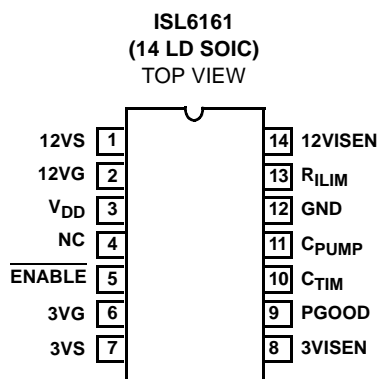
The ISL6161 is a HOT SWAP dual supply power distribution controller that can be used in PCI-Express applications.

Two external N-Channel MOSFETs are driven to distribute and control power while providing load fault isolation. At turn-on, the gate of each external N-Channel MOSFET is charged with a 10 $\mu$ A current source. Capacitors on each gate (see the "Typical Application Diagram" on page 1), create a programmable ramp (soft turn-on) to control in-rush currents. A built-in charge pump supplies the gate drive for the 12V supply N-Channel MOSFET switch.

Overcurrent protection is facilitated by two external current sense resistors and FETs. When the current through either resistor exceeds the user programmed value, the controller enters the current regulation mode. The time-out capacitor, C<sub>TIM</sub>, starts charging as the controller enters the time-out period. Once C<sub>TIM</sub> charges to a 2V threshold, both the N-Channel MOSFETs are latched off. In the event of a hard and fast fault of at least 3x the programmed current limit level, the N-Channel MOSFET gates are pulled low immediately before entering the time-out period. The controller is reset by a rising edge on the ENABLE pin.

The ISL6161 constantly monitors both output voltages and reports either one being low on the PGOOD output as a low. The 12V PGOOD V<sub>th</sub> is ~10.8V and the 3.3V V<sub>th</sub> is ~2.8V nominally.

## Pinout



## Features

- HOT SWAP Dual Power Distribution and Control for +12V and +3.3V
- Provides Fault Isolation
- Programmable Current Regulation Level
- Programmable Time-Out
- Charge Pump Allows the Use of N-Channel MOSFETs
- Power-Good and Overcurrent Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Two Levels of Current Limit Detection Provide Fast Response to Varying Fault Conditions
- 1 $\mu$ s Response Time to Dead Short
- 3 $\mu$ s Response Time to 200% Current Overshoot
- Pb-Free Available (RoHS compliant)

## Applications

- PCI-Express Applications
- Power Distribution and Control
- Hot Plug, Hot Swap Components

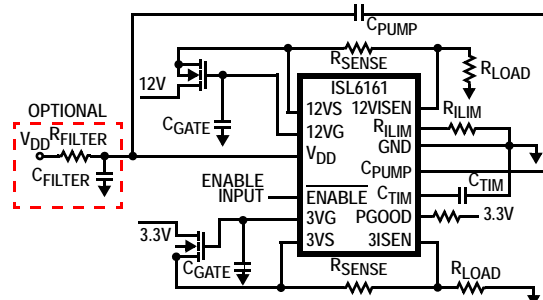
## Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6161IBZA* (Note)	ISL6161 IBZ	-40 to +85	14 Ld SOIC (Pb-free)	M14.15
ISL6161CB*	ISL6161CB	0 to +70	14 Ld SOIC	M14.15
ISL6161CBZA* (Note)	6161CBZ	0 to +70	14 Ld SOIC (Pb-free)	M14.15

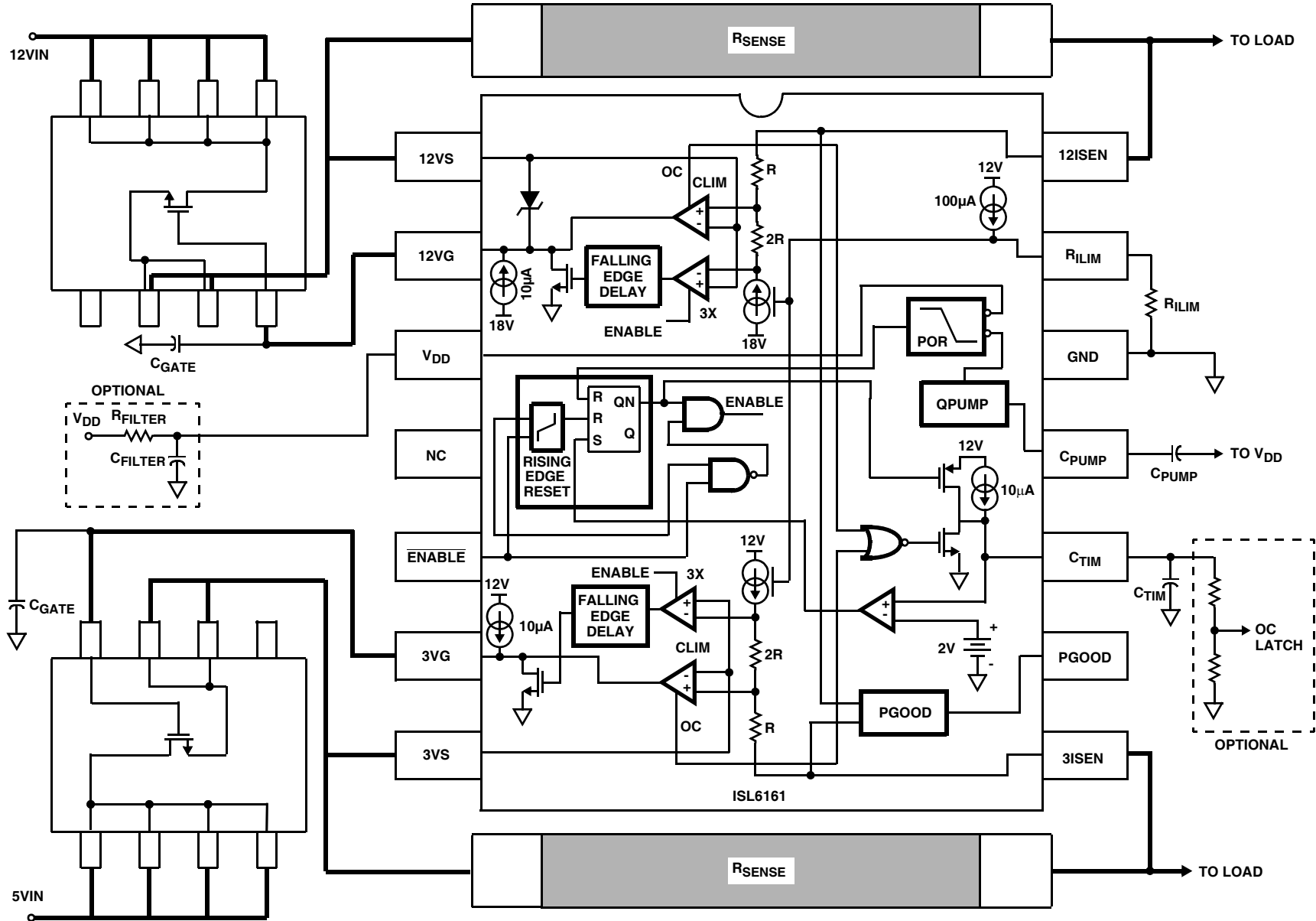
\*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

## Typical Application Diagram



# Simplified Schematic



ISL6161

# ISL6161

## Pin Descriptions

PIN NUMBER	SYMBOL	FUNCTION	DESCRIPTION
1	12VS	12V Source	Connect to source of associated external N-Channel MOSFET switch to sense output voltage.
2	12VG	12V Gate	Connect to the gate of associated N-Channel MOSFET switch. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to ~17.4V by a 10 $\mu$ A current source.
3	V <sub>DD</sub>	Chip Supply	Connect to 12V supply. This can be either connected directly to the +12V rail supplying the load voltage or to a dedicated V <sub>DD</sub> +12V supply. If the former is chosen, special attention to V <sub>DD</sub> decoupling must be paid to prevent sagging as heavy loads are switched on.
4	NC	Not Connected	
5	$\overline{\text{ENABLE}}$	Enable/Reset	$\overline{\text{ENABLE}}$ is used to turn-on and reset the chip. Both outputs turn-on when this pin is driven low. After a current limit time-out, the chip is reset by the rising edge of a reset signal applied to the ENABLE pin. This input has 100 $\mu$ A pull-up capability, which is compatible with 3V and 5V open drain and standard logic.
6	3VG	3V Gate	Connect to the gate of the external 3V N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on, this capacitor will be charged to ~11.4V by a 10 $\mu$ A current source.
7	3VS	3 Source	Connect to the source side of 3V external N-Channel MOSFET switch to sense output voltage.
8	3VISEN	3V Current Sense	Connect to the load side of the 3V sense resistor to measure the voltage drop across this resistor between 3VS and 3VISEN pins.
9	PGOOD	Power-Good indicator	Indicates that all output voltages are within specification. PGOOD is driven by an open drain N-Channel MOSFET. It is pulled low when any output is not within specification.
10	C <sub>TIM</sub>	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor controls the time between the onset of current limit and chip shutdown (current limit time-out). The duration of current limit time-out (in seconds) = 200k $\Omega$ x C <sub>TIM</sub> (Farads).
11	C <sub>PUMP</sub>	Charge Pump Capacitor	Connect a 0.1 $\mu$ F capacitor between this pin and V <sub>DD</sub> (pin 3). Provides charge storage for 12VG drive.
12	GND	Chip Ground	
13	R <sub>ILIM</sub>	Current Limit Set Resistor	A resistor connected between this pin and ground determines the current level at which current limit is activated. This current is determined by the ratio of the R <sub>ILIM</sub> resistor to the sense resistor (R <sub>SENSE</sub> ). The current at current limit onset is equal to 10 $\mu$ A x (R <sub>ILIM</sub> /R <sub>SENSE</sub> ). The ISL6161 is limited to a 10k $\Omega$ min. value (OC V <sub>th</sub> = 100mV) resistor whereas the ISL6161 can accommodate a 5k $\Omega$ resistor for a lower OC V <sub>th</sub> (50mV).
14	12VISEN	12V Current Sense	Connect to the load side of sense resistor to measure the voltage drop across this resistor.

# ISL6161

## Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

$V_{DD}$ .....	-0.3V to +16V
12VG, $C_{PUMP}$ .....	-0.3V to 21V
12VISEN, 12VS .....	-5V to $V_{DD} + 0.3\text{V}$
3VISEN, 3VS .....	-5V to 7.5V
PGOOD, $R_{ILIM}$ .....	-0.3V to 7.5V
ENABLE, $C_{TIM}$ , 3VG .....	-0.3V to $V_{DD} + 0.3\text{V}$
ESD Classification .....	2kV (Class 2)

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )
SOIC Package .....	67
Maximum Junction Temperature (Plastic Package) .....	+150 $^\circ\text{C}$
Maximum Storage Temperature Range .....	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Pb-Free Reflow Profile .....	see link below
<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

## Operating Conditions

$V_{DD}$ Supply Voltage Range .....	+10.5V to +13.2V
Temperature Range ( $T_A$ )	
ISL6161B .....	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$
ISL6161CB .....	0 $^\circ\text{C}$ to +70 $^\circ\text{C}$

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- All voltages are relative to GND, unless otherwise specified.

**Electrical Specifications**  $V_{DD} = 12\text{V}$ ,  $C_{VG} = 0.01\mu\text{F}$ ,  $C_{TIM} = 0.1\mu\text{F}$ ,  $R_{SENSE} = 0.1\Omega$ ,  $C_{BULK} = 220\mu\text{F}$ ,  $ESR = 0.5\Omega$ ,  $T_A = T_J = -40^\circ\text{C}$  to +85 $^\circ\text{C}$ , Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25 $^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>12V CONTROL SECTION</b>						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	$V_{IL12V}$	$R_{ILIM} = 10\text{k}\Omega$	92	100	108	mV
		$R_{ILIM} = 5\text{k}\Omega$	47	53	59	mV
3x Current Limit Threshold Voltage (Voltage Across Sense Resistor)	3 x $V_{IL12V}$	$R_{ILIM} = 10\text{k}\Omega$	250	300	350	mV
		$R_{ILIM} = 5\text{k}\Omega$	100	165	210	mV
$\pm 20\%$ Current Limit Response Time (Current within 20% of Regulated Value)	20% $i_{Lrt}$	200% Current Overload, $R_{ILIM} = 10\text{k}\Omega$ , $R_{SHORT} = 6.0\Omega$	-	2	-	$\mu\text{s}$
$\pm 10\%$ Current Limit Response Time (Current within 10% of Regulated Value)	10% $i_{Lrt}$	200% Current Overload, $R_{ILIM} = 10\text{k}\Omega$ , $R_{SHORT} = 6.0\Omega$	-	4	-	$\mu\text{s}$
$\pm 1\%$ Current Limit Response Time (Current within 1% of Regulated Value)	1% $i_{Lrt}$	200% Current Overload, $R_{ILIM} = 10\text{k}\Omega$ , $R_{SHORT} = 6.0\Omega$	-	10	-	$\mu\text{s}$
Response Time to Dead Short	$R_{TSHORT}$	$C_{12VG} = 0.01\mu\text{F}$	-	500	-	ns
Gate Turn-On Time	$t_{ON12V}$	$C_{12VG} = 0.01\mu\text{F}$	-	12	-	ms
Gate Turn-On Current	$I_{ON12V}$	$C_{12VG} = 0.01\mu\text{F}$	8	10	12	$\mu\text{A}$
3x Gate Discharge Current	3Xdisl	12VG = 18V	-	0.75	-	A
12V Undervoltage Threshold	12V $V_{UV}$		10.5	10.8	11.0	V
Charge Pumped 12VG Voltage	V12VG	$C_{PUMP} = 0.1\mu\text{F}$	16.8	17.3	17.9	V
<b>3.3V CONTROL SECTION</b>						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	$V_{IL3V}$	$R_{ILIM} = 10\text{k}\Omega$	92	100	108	mV
		$R_{ILIM} = 5\text{k}\Omega$	47	53	59	mV
3x Current Limit Threshold Voltage (Voltage Across Sense Resistor)	3 x $V_{IL3V}$	$R_{ILIM} = 10\text{k}\Omega$	250	300	350	mV
		$R_{ILIM} = 5\text{k}\Omega$	100	155	210	mV
$\pm 20\%$ Current Limit Response Time (Current within 20% of Regulated Value)		200% Current Overload, $R_{ILIM} = 10\text{k}\Omega$ , $R_{SHORT} = 2.5\Omega$	-	2	-	$\mu\text{s}$
$\pm 10\%$ Current Limit Response Time (Current within 10% of Regulated Value)		200% Current Overload, $R_{ILIM} = 10\text{k}\Omega$ , $R_{SHORT} = 2.5\Omega$	-	4	-	$\mu\text{s}$

**Electrical Specifications**  $V_{DD} = 12V$ ,  $C_{VG} = 0.01\mu F$ ,  $C_{TIM} = 0.1\mu F$ ,  $R_{SENSE} = 0.1\Omega$ ,  $C_{BULK} = 220\mu F$ ,  $ESR = 0.5\Omega$ ,  $T_A = T_J = -40^\circ C$  to  $+85^\circ C$ , Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ C$ , unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\pm 1\%$ Current Limit Response Time (Current within 1% of Regulated Value)		200% Current Overload, $R_{LIM} = 10k\Omega$ , $R_{SHORT} = 2.5\Omega$	-	10	-	$\mu s$
Response Time To Dead Short	$RT_{SHORT}$	$C_{VG} = 0.01\mu F$	-	500		ns
Gate Turn-On Time	$t_{ON3V}$	$C_{VG} = 0.01\mu F$	-	5	-	ms
Gate Turn-On Current	$I_{ON3V}$	$C_{VG} = 0.01\mu F$	8	10	12	$\mu A$
3x Gate Discharge Current	3xdisl	$C_{VG} = 0.01\mu F$ , ENABLE = Low		0.75	-	A
3.3V Undervoltage Threshold	3.3V <sub>VUV</sub>		2.7	2.85	3.0	V
3.3VG High Voltage	3VG		11.2	11.9	-	V
<b>SUPPLY CURRENT AND IO SPECIFICATIONS</b>						
$V_{DD}$ Supply Current	$I_{VDD}$		4	8	10	mA
$V_{DD}$ POR Rising Threshold			9.5	10.0	10.7	V
$V_{DD}$ POR Falling Threshold			9.0	9.4	9.8	V
Current Limit Time-Out	$t_{LIM}$	$C_{TIM} = 0.1\mu F$	-	20	-	ms
$\overline{ENABLE}$ Pull-up Voltage	PWRN_V	$\overline{ENABLE}$ pin open	1.8	2.4	3.2	V
$\overline{ENABLE}$ Rising Threshold	PWR_Vth		1.1	1.5	2	V
$\overline{ENABLE}$ Hysteresis	PWR_hys		0.1	0.2	0.3	V
$\overline{ENABLE}$ Pull-Up Current	PWRN_I		60	80	100	$\mu A$
Current Limit Time-Out Threshold ( $C_{TIM}$ )	$C_{TIM\_Vth}$		1.8	2	2.2	V
$C_{TIM}$ Charging Current	$C_{TIM\_I}$		8	10	12	$\mu A$
$C_{TIM}$ Discharge Current	$C_{TIM\_disl}$		1.7	2.6	3.5	mA
$C_{TIM}$ Pull-Up Current	$C_{TIM\_disl}$	$V_{CTIM} = 8V$	3.5	5	6.5	mA
$R_{LIM}$ Pin Current Source Output	$R_{LIM\_Io}$		90	100	110	$\mu A$
Charge Pump Output Current	Qpmp_Io	$C_{PUMP} = 0.1\mu F$ , $C_{PUMP} = 16V$	320	560	900	$\mu A$
Charge Pump Output Voltage	Qpmp_Vo	No load	17.2	17.4	-	V
Charge Pump Output Voltage - Loaded	Qpmp_Vlo	Load current = 100 $\mu A$	16.2	16.7	-	V
Charge Pump POR Rising Threshold	Qpmp + Vth		15.6	16	16.5	V
Charge Pump POR Falling Threshold	Qpmp - Vth		15.2	15.7	16.2	V

**ISL6161 Description and Operation**

The ISL6161 is a multi-featured +12V and +3.3V dual power supply distribution controller. Its features include programmable current regulation (CR) limiting and time to latch off.

At turn-on, the gate capacitor of each external N-Channel MOSFET is charged with a 10 $\mu A$  current source. These capacitors create a programmable ramp (soft turn-on). A charge pump supplies the gate drive for the 12V supply control FET switch driving that gate to 17V.

The load currents pass through two external current sense resistors. When the voltage across either resistor quickly exceeds the user programmed Current Regulation voltage threshold (CRVth) level, the controller enters current regulation. The CRVth is set by the external resistor value on  $R_{LIM}$  pin. At

this time, the time-out capacitor,  $C_{TIM}$ , starts charging with a 10 $\mu A$  current source and the controller enters the time-out period. The length of the time-out period is set by the single external capacitor (see Table 2) placed from the  $C_{TIM}$  pin (pin 10) to ground and is characterized by a lowered gate drive voltage to the appropriate external N-Channel MOSFET. Once  $C_{TIM}$  charges to 2V, an internal comparator is tripped resulting in both N-Channel MOSFETs being latched off. If the voltage across the sense resistors rises slowly in response to an OC condition, then the CR mode is entered at ~95% of the programmed CR level. This difference is due to the necessary hysteresis and response time in the CR control circuitry.

Table 1 shows  $R_{SENSE}$  and  $R_{LIM}$  recommendations and resulting CR level for the PCI-Express add-in card connector sizes specified.

TABLE 1. R<sub>SENSE</sub> AND R<sub>LIM</sub> RECOMMENDATIONS

PCI-EXPRESS ADD-IN CARD CONNECTOR	R <sub>LIM</sub> (kΩ)	3.3V R <sub>SENSE</sub> (mΩ), NOMINAL CR (A)	12V R <sub>SENSE</sub> (mΩ), NOMINAL CR (A)	NOMINAL CRV <sub>th</sub> (mV)
X1	10	30, 3.3	150, 0.7	100
	4.99	15, 3.5	90, 0.6	53
X4/X8	10	30, 3.3	40, 2.5	100
	4.99	15, 3.5	20, 2.6	53
X16	10	30, 3.3	16, 6.3	100
	4.99	15, 3.5	8, 6.6	53

NOTE: Nominal CR V<sub>th</sub> = R<sub>LIM</sub> × 10μA.

TABLE 2.

C <sub>TIM</sub> CAPACITOR (μF)	NOMINAL TIME-OUT PERIOD (ms)
0.022	4.4
0.047	9.4
0.1	20

NOTE: Nominal time-out period in seconds = C<sub>TIM</sub> × 200kΩ.

The ISL6161 responds to a load short (defined as a current level 3x the OC set point with a fast transition) by immediately driving the relevant N-Channel MOSFET gate to 0V in ~3μs. The gate voltage is then slowly ramped up, soft-starting the N-Channel MOSFET to the programmed current regulation limit level. This is the start of the time-out period if the abnormal load condition still exists. The programmed current regulation level is held until either the OC event passes or the time-out period expires. If the former is the case, then the N-Channel MOSFET is fully enhanced and the C<sub>TIM</sub> charging current is diverted away from the capacitor. If the time-out period expires prior to OC resolution, then both gates are quickly pulled to 0V turning off both N-Channel MOSFETs simultaneously.

Upon any UV condition, the PGOOD signal will pull low when tied high through a resistor to the logic supply. This pin is a fault indicator but not the OC latch-off indicator. For an OC latch-off indication, monitor CTIM, pin 10. This pin will rise rapidly to 12V once the time-out period expires. See "Simplified Schematic" on page 2 for OC latch-off circuit suggestion.

The ISL6161 is reset by a rising edge on the ENABLE pin and is turned on by the ENABLE pin being driven low.

## ISL6161 Application Considerations

In a non PCI-Express, motor drive application, **Current loop stabilization** is facilitated through a small value resistor in series with the gate timing capacitor. As the ISL6161 drives a highly inductive current load, instability characterized by the gate voltage repeatedly ramping up and down may appear. A simple method to enhance stability is provided by the substitution of a larger value gate resistor. Typically, this situation can be avoided by eliminating long point-to-point wiring to the load.

With the ENABLE internal pull-up, the ISL6161 is well suited for implementation on either side of the connector where a motherboard prebiased condition or a load board staggered connection is present. In either case, the ISL6161 turns on in a soft-start mode protecting the supply rail from sudden current loading.

During the **Time-Out delay period** with the ISL6161 in current limit mode, the V<sub>GS</sub> of the external N-Channel MOSFETs is reduced driving the N-Channel MOSFET switch into a high r<sub>DS(ON)</sub> state. Thus, avoid extended time-out periods as the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the MOSFET manufacturers data sheet for SOA information.

With the high levels of in-rush current e.g., highly capacitive loads and motor start-up currents, **choosing the current regulation (CR) level** is crucial to provide both protection and still allow for this in-rush current without latching off. Consider this in addition to the time-out delay when choosing MOSFETs for your design.

**Physical layout of R<sub>SENSE</sub> resistors** is critical to avoid inadvertently lowering the CR and trip levels. Ideally, trace routing between the R<sub>SENSE</sub> resistors and the ISL6161 should be as direct and as short as possible with zero current in the sense lines.

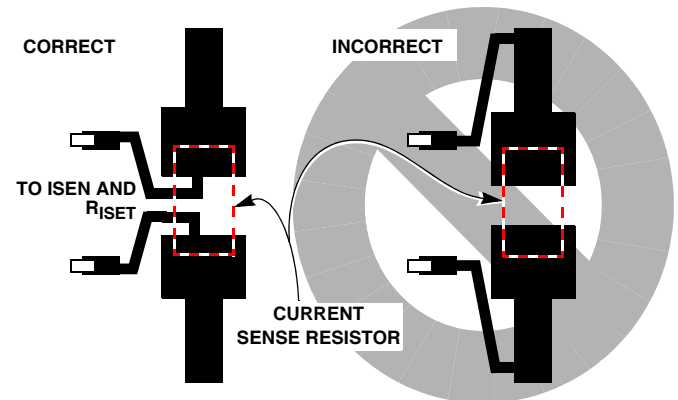


FIGURE 1. SENSE RESISTOR PCB LAYOUT

**Open load detection** can be accomplished by monitoring the ISEN pins. Although gated off, the external FET  $I_{DSS}$  will cause the ISEN pin to float above ground to some voltage when there is no attached load. If this is not desired, 5k resistors from the xISEN pins to ground will prevent the outputs from floating when the external switch FETs are disabled and the outputs are open.

For **PCI-Express applications**, the ISL6161 and the ISL6118 provide the fundamental hotswap function for the +12V and +3.3V main rails and the +3.3V aux respectively, as shown in the “PCI-Express Implementation of ISL6161 and ISL6118” on page 10.

**Typical Performance Curves**

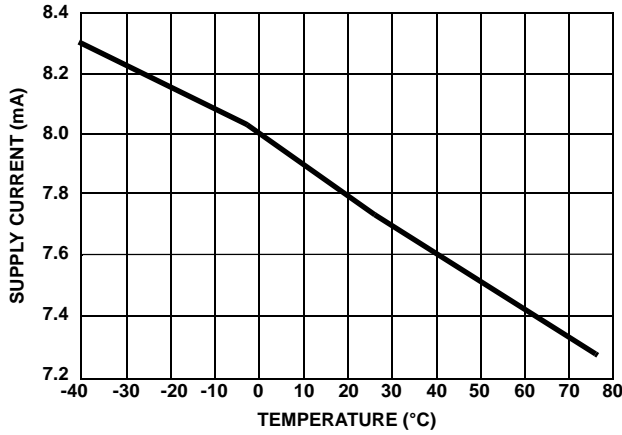


FIGURE 2. SUPPLY CURRENT

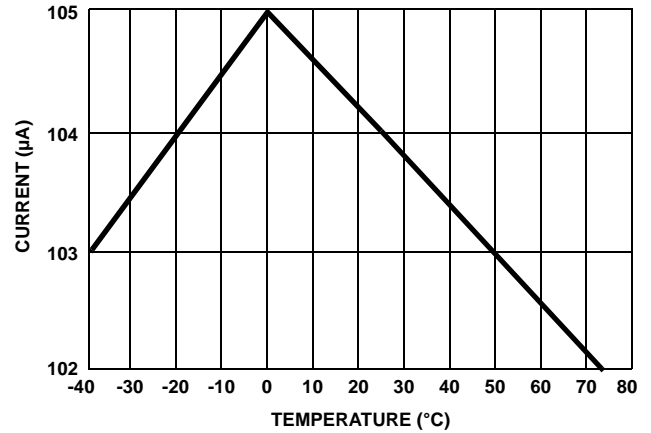


FIGURE 3. R\_ILIM SOURCE CURRENT

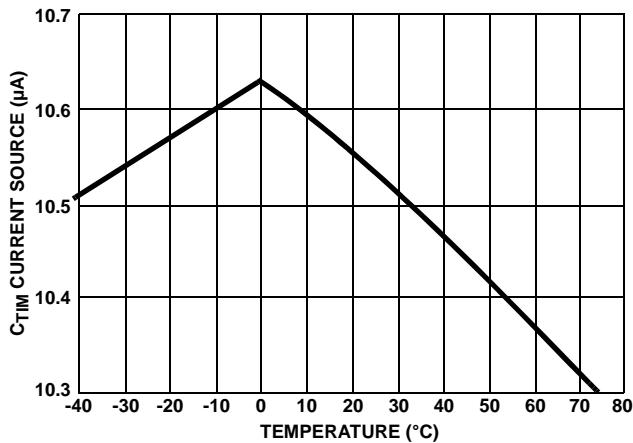


FIGURE 4. C\_TIM CURRENT SOURCE

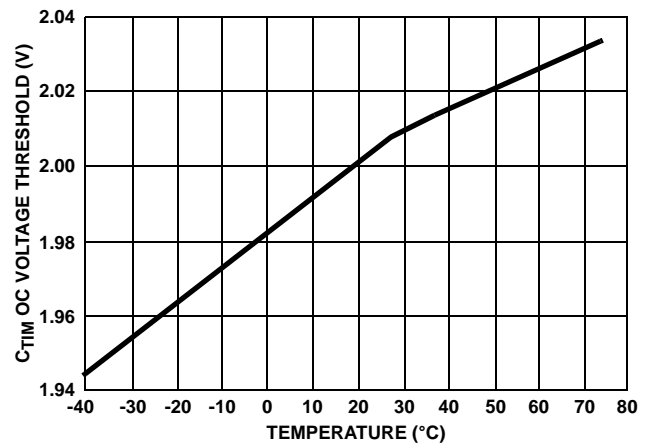


FIGURE 5. C\_TIM OC VOLTAGE THRESHOLD

Typical Performance Curves (Continued)

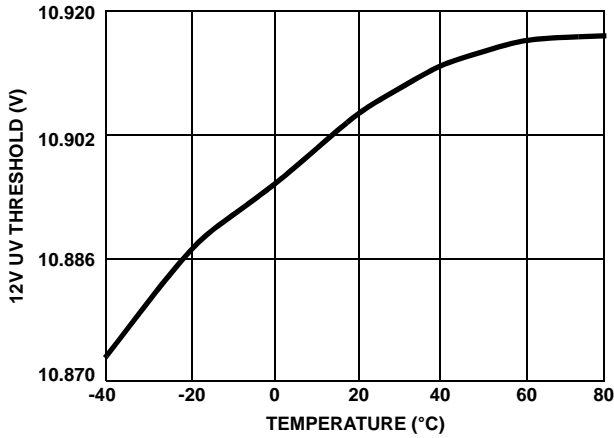


FIGURE 6. 12V UV THRESHOLD

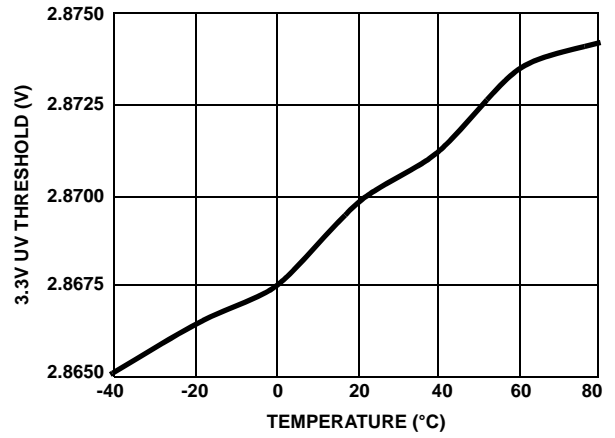


FIGURE 7. 3.3V UV THRESHOLD

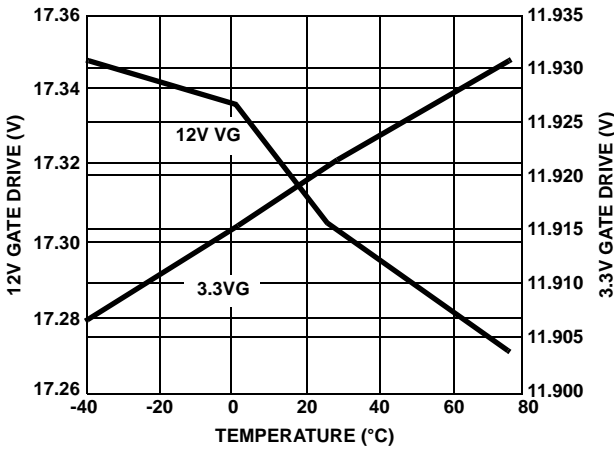


FIGURE 8. 12V, 3V GATE DRIVE

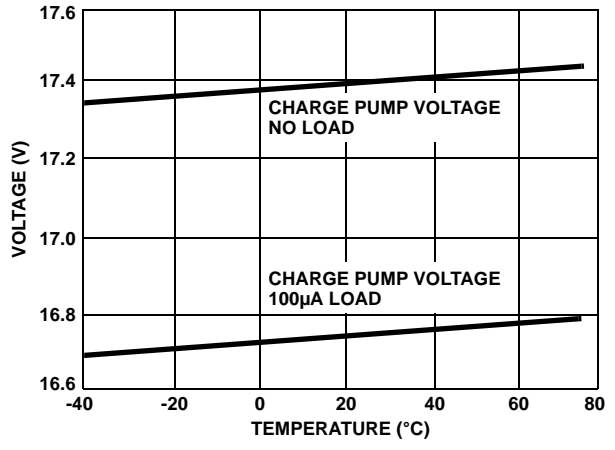


FIGURE 9. PUMP VOLTAGE

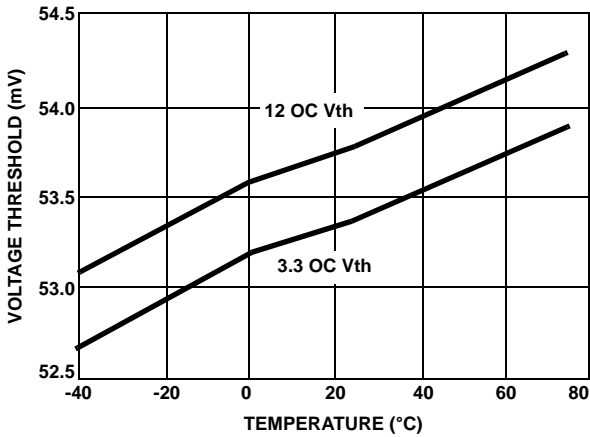


FIGURE 10. OC VOLTAGE THRESHOLD WITH  $R_{LIM} = 5k\Omega$

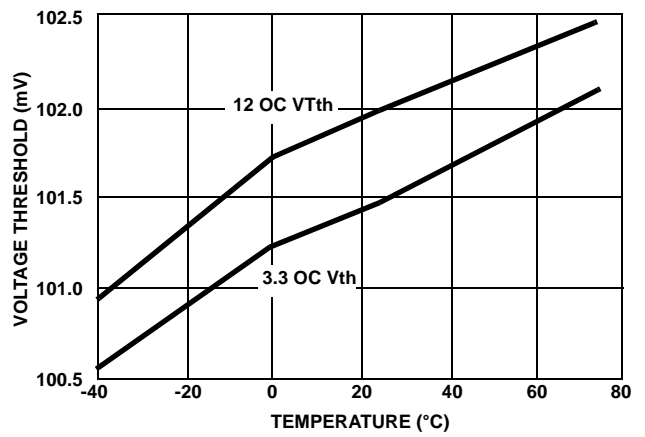


FIGURE 11. OC VOLTAGE THRESHOLD WITH  $R_{LIM} = 10k\Omega$



Typical Performance Curves (Continued)

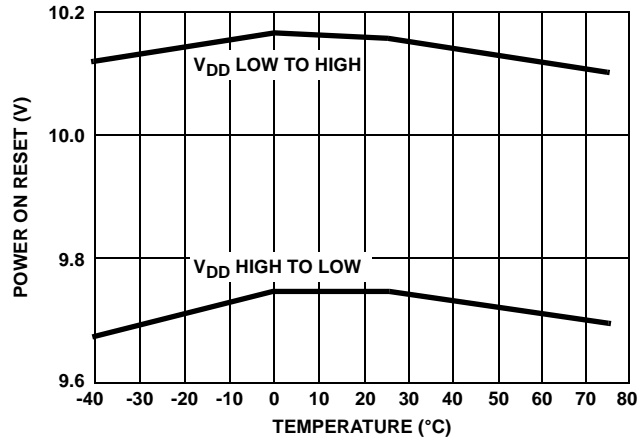
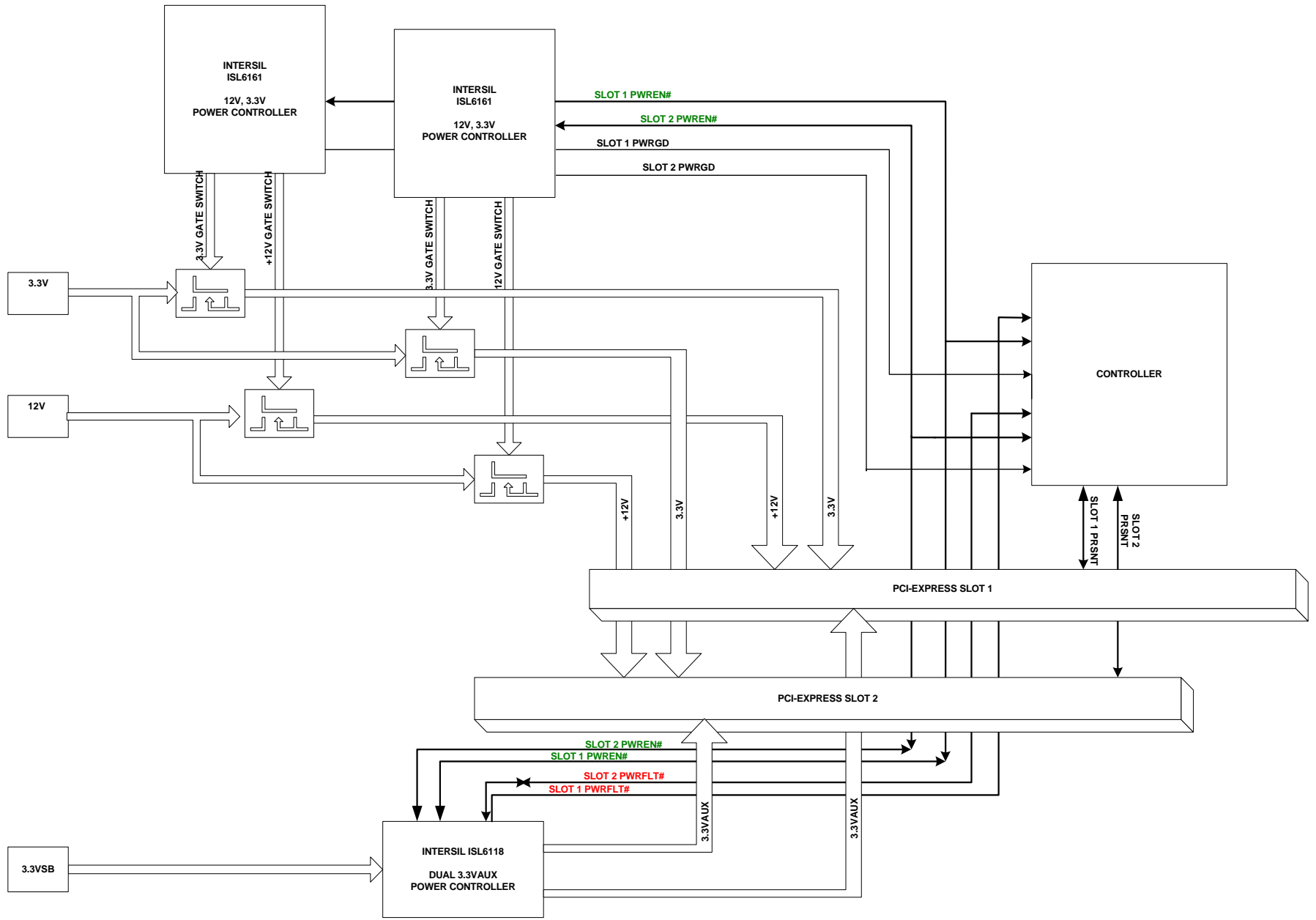
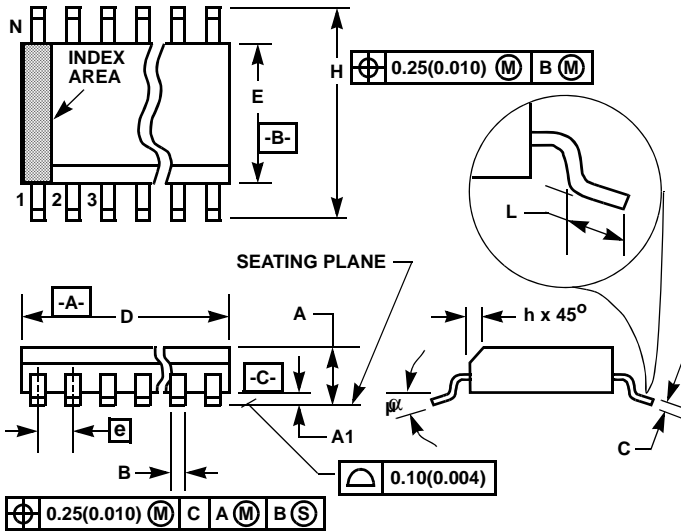


FIGURE 12. POWER-ON RESET VOLTAGE THRESHOLD

# PCI-Express Implementation of ISL6161 and ISL6118



**Small Outline Plastic Packages (SOIC)**



**M14.15 (JEDEC MS-012-AB ISSUE C)  
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

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