

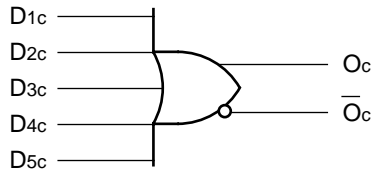
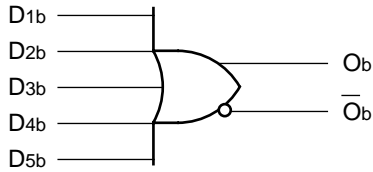
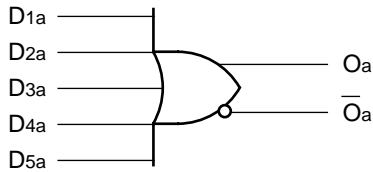
FEATURES

- Max. propagation delay of 750ps
- IEE min. of -25mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- 20% faster than Fairchild 300K at lower power
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S301 is an ultra-fast triple 5-input OR/NOR gate designed for use in high-performance ECL systems. The inputs on this device have 75KΩ pull-down resistors.

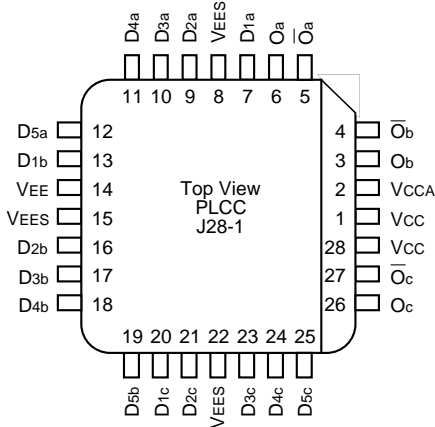
BLOCK DIAGRAM



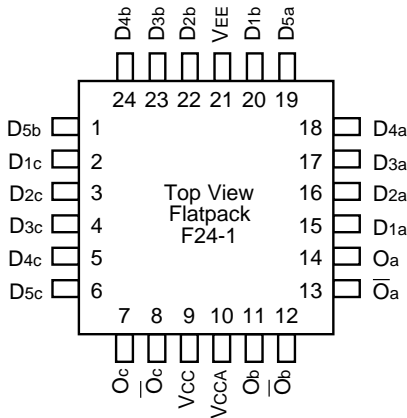
PIN NAMES

| Pin | Function |
|--------------------------------|----------------------------|
| Dna, Dnb, Dnc | Data Inputs (n-1...5) |
| $\bar{O}a, \bar{O}b, \bar{O}c$ | Data Outputs |
| Oa, Ob, Oc | Complementary Data Outputs |
| VEES | VEE Substrate |
| VCCA | Vcco for ECL Outputs |

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---------------------------------|--------------|-----------------|---|-------------|
| SY100S301FC | F24-1 | Commercial | SY100S301FC | Sn-Pb |
| SY100S301FCTR ⁽¹⁾ | F24-1 | Commercial | SY100S301FC | Sn-Pb |
| SY100S301JC | J28-1 | Commercial | SY100S301JC | Sn-Pb |
| SY100S301JCTR ⁽¹⁾ | J28-1 | Commercial | SY100S301JC | Sn-Pb |
| SY100S301JZ ⁽²⁾ | J28-1 | Commercial | SY100S301JZ with Pb-Free bar-line indicator | Matte-Sn |
| SY100S301JZTR ^(1, 2) | J28-1 | Commercial | SY100S301JZ with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

LOGIC EQUATION

$$O_a = D_{1a} + D_{2a} + D_{3a} + D_{4a} + D_{5a}$$

$$O_b = D_{1b} + D_{2b} + D_{3b} + D_{4a} + D_{5b}$$

$$O_c = D_{1c} + D_{2c} + D_{3c} + D_{4c} + D_{5c}$$

GUARANTEED OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|----------------------|------|------|------|------|
| VEE | Input HIGH Current | -5.5 | -4.5 | -4.2 | V |
| TA | Power Supply Current | 0 | 25 | 85 | °C |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Value | Unit |
|--------|--|--------------|------|
| VEE | Power Supply | -0.5 to +7.0 | V |
| VIN | Input Voltage | -0.5 to VEE | V |
| IOUT | DC Output Current | -50 | mA |
| TC | Temperature Under Bias | -55 to +125 | °C |
| TJ | Junction Temperature | +150 | °C |
| TLEAD | Lead Temperature (soldering, 20 sec.) | +260 | °C |
| Tstore | Storage Temperature | -65 to +150 | °C |

Note:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|-----------------|----------------------|------|------|------|------|-------------|
| I _{IH} | Input HIGH Current | — | — | 200 | μA | — |
| I _{EE} | Power Supply Current | -25 | -17 | -11 | mA | Inputs Open |

AC ELECTRICAL CHARACTERISTICS**CERPACK**

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

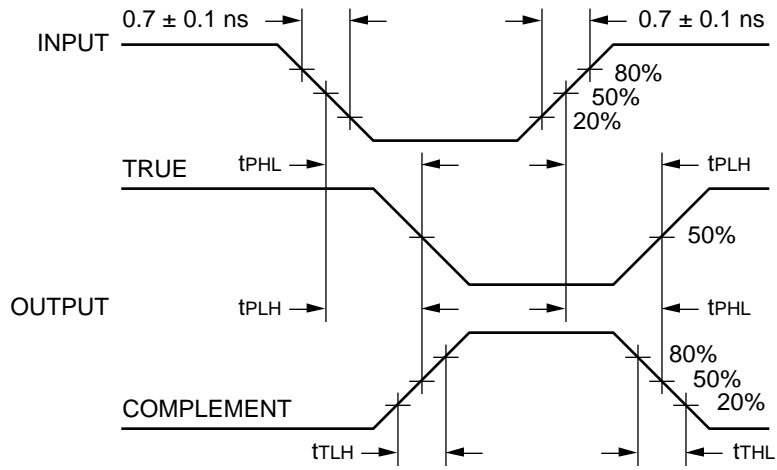
| Symbol | Parameter | TA = 0°C | | TA = +25°C | | TA = +85°C | | Unit | Condition |
|--------------------------------------|---|----------|------|------------|------|------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 300 | 800 | 300 | 800 | 300 | 800 | ps | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |

PLCC

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

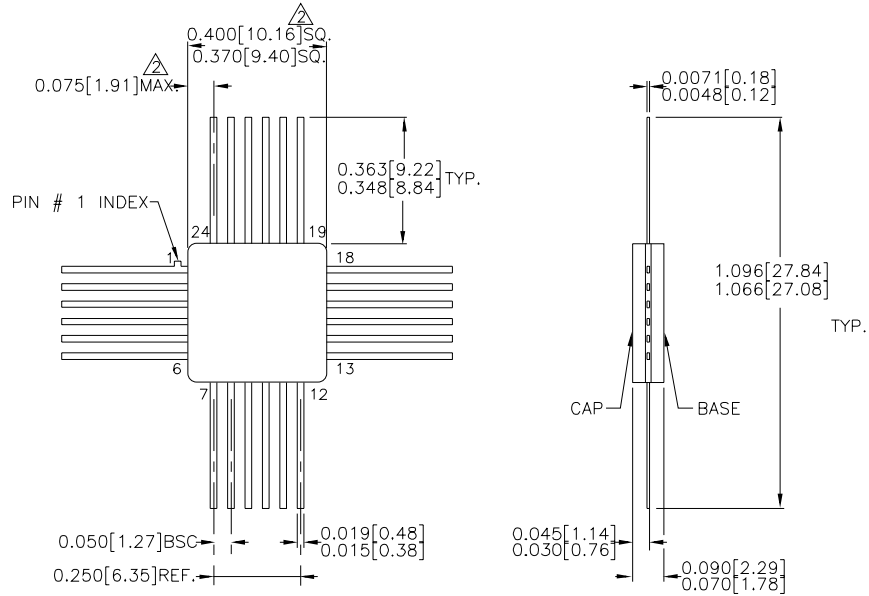
| Symbol | Parameter | TA = 0°C | | TA = +25°C | | TA = +85°C | | Unit | Condition |
|--------------------------------------|---|----------|------|------------|------|------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 300 | 750 | 300 | 750 | 300 | 750 | ps | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |

TIMING DIAGRAM



Propagation Delay and Transition Times

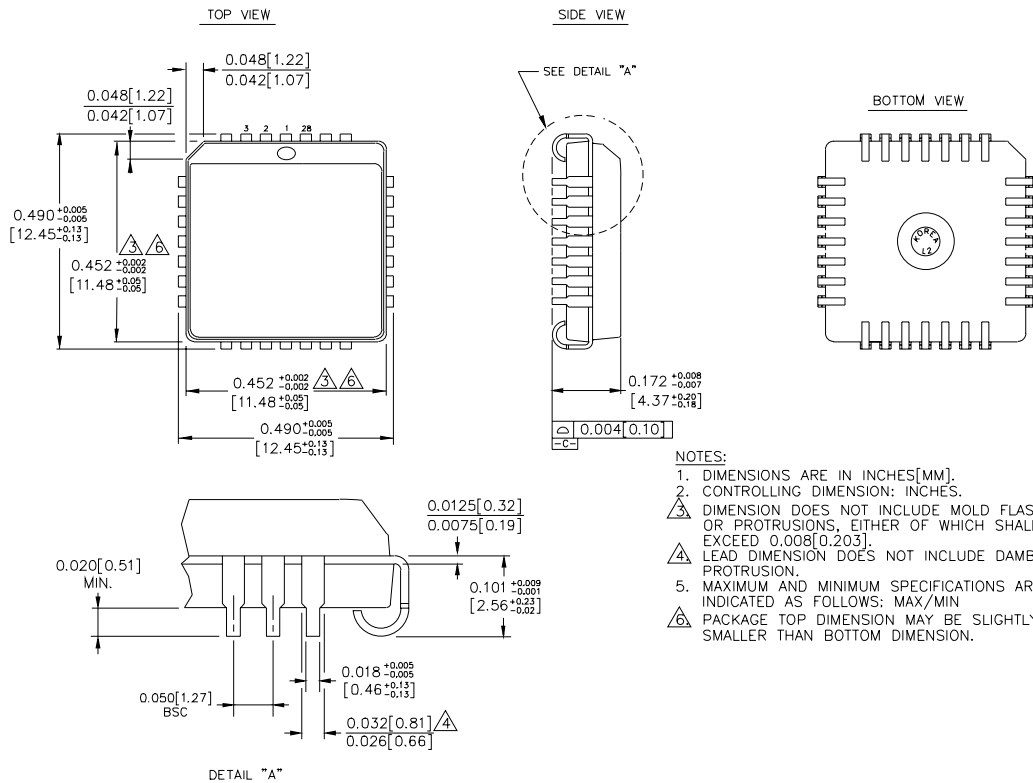
24-PIN CERPACK (F24-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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